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Optimization of Gate Oxide Screening Technology for Commercial SiC Discrete MOSFETs and Power Modules

Limeng Shi[1,a*], Michael Jin[1,b], Jiashu Qian[1,c], Monikuntala Bhattacharya[1,d], Shiva Houshmand[1,e], Hengyu Yu[1,f], Atsushi Shimbori[2,g], Marvin H. White[1,h], Anant K. Agarwal[1,i]

[1]Dept. of Electrical & Computer Eng., The Ohio State University, Columbus, OH, USA

[2]Ford Motor Company, Dearborn, MI, USA

[a]shi.1564@osu.edu, [b]jin.845@osu.edu, [c]qian.539@osu.edu, [d]bhattacharya.119@osu.edu, [e]houshmand.3@osu.edu, [f]yu.3868@osu.edu, [g]ashimbor@ford.com, [h]white.1829@osu.edu, [i]agarwal.334@osu.edu

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Abstract. This study demonstrates a negative correlation between gate leakage current (I_{gss}) and time to breakdown (t_{bd}) of gate oxide in various commercial SiC discrete MOSFETs and power modules. SiC MOSFETs with higher leakage current at the same gate voltage exhibit lower oxide failure time in the constant-voltage Time-Dependent Dielectric Breakdown (TDDB) test. The novelty lies in the discovery that I_{gss} measured under conditions of either low gate voltage (V_g) at RT or high V_g at 150°C can be utilized to identify discrete devices or power modules with non-infant failures or lower intrinsic lifetime. Aggressive screening based on I_{gss} helps to reduce non-infant extrinsic failure probability and identify devices with more uniformity of intrinsic lifetime.

Introduction

A significant challenge in the adoption of SiC MOSFETs for electric vehicle (EV) applications is the issue of gate oxide failure. In practical circuits, certain SiC MOSFETs exhibit early gate oxide breakdown, which is primarily attributed to the high extrinsic defect density inherent in these devices [1,2]. Therefore, it is essential to implement a screening process to eliminate unreliable devices prior to deployment [3–5]. The conventional screening method involves applying high-voltage pulses to the gate electrode for a specified duration, followed by the removal of failed devices. However, manufacturers tend to employ conservative screening conditions to avoid compromising the performance of SiC MOSFETs [6–8]. The conventional screening process can basically remove infant failures, but some non-infant failures close to the intrinsic failure line still survive [9].

In this study, gate leakage current (I_{gss}) and gate oxide lifetime (t_{bd}) measurements are performed on a variety of commercial SiC discrete MOSFETs and power modules. The relationship between gate leakage current and oxide lifetime is analyzed using the charge-to-breakdown mechanism. Based on the measurement results, an optimized screening method is developed to eliminate extrinsic failure tails and identify devices with more consistent intrinsic lifetime characteristics. Furthermore, the effectiveness of the enhanced screening technique is validated.

Experimental

Table 1 summarizes the relevant information for the commercial SiC discrete MOSFETs and power modules studied in this work. SiC devices with different gate structures and current ratings are selected for the investigation. Fig. 1 illustrates the test procedures for measuring gate leakage current and oxide lifetime in SiC planar 17 A discrete MOSFETs. Initially, I_{gss} is measured at room temperature (RT) with a gate voltage of 30 V, followed by the I_{gss} measurement at 150°C with a gate voltage of 34 V (~ 9 MV/cm). Subsequently, a constant-voltage Time-Dependent Dielectric

Breakdown (TDDB) test is conducted at 150°C to determine the lifetime of the gate oxide. Depending on the parameter information of the SiC MOSFETs from different vendors, the measured voltages of I_{gss} and t_{bd} are adjusted accordingly.

The breakdown characteristics of the gate oxide are analyzed using the Fowler-Nordheim (FN) tunneling and charge-to-breakdown (Q_{bd}) mechanisms [10–14], as described in Eq. 1–3. In addition, the oxide lifetimes obtained from the TDDB tests are plotted using Weibull distribution [15]. Based on the cumulative distribution function (see Eq. 4), the oxide lifetime with different failure rates can be calculated. The value of I_{gss} for devices that cannot reach $t_{F\%}$ is predicted from the fitted line of I_{gss} and t_{bd}.

Table 1. Commercial 1.2 kV SiC devices studied.

Type	Discrete Device	Discrete Device	Power Module	Discrete Device	Discrete Device
Current (A)	17	115	450	11	17
Structure	Planar	Planar	Planar	Planar	Double-Trench
t_{ox} (nm)	~38	~38	~38	~46	~55

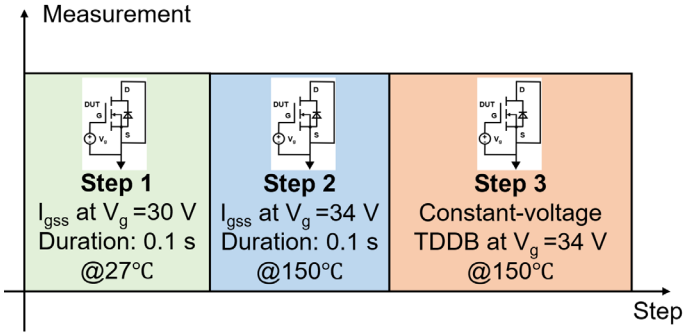

Fig. 1. Test procedures for SiC planar 17 A discrete MOSFETs.

$$J_{FN}(T) = A(T)E_{ox}^2 \exp(-\frac{B(T)}{E_{ox}}) \quad (1)$$

$$t_{bd} = \frac{Q_{bd}}{I_{FN}} \quad (2)$$

$$\log(t_{bd}) = \log(Q_{bd}) - \log(I_{FN}) \quad (3)$$

$$t_{F\%} = t_{63\%} * \exp\{\frac{1}{\beta}(\ln(-\ln(1-F)))\} \quad (4)$$

Results and Discussion

Constant-voltage TDDB tests at 150°C are conducted on SiC discrete MOSFETs and power modules, as illustrated in Fig. 2. The results show that a small percentage of commercial devices still experience early oxide breakdown. Moreover, the oxide lifetime distributions for power modules and trench devices exhibit greater variability compared to planar devices. Therefore, it is necessary to optimize the screening technology to reduce the probability of early oxide breakdown and allow the remaining devices to have a high uniform intrinsic lifetime of gate oxide. Fig. 3 shows the test curves of gate leakage current for SiC planar 17 A discrete MOSFETs devices, from the beginning of the TDDB test until oxide breakdown. The charge-to-breakdown (Q_{bd}) is calculated using the integration method. Fig. 4 illustrates the Weibull distributions of Q_{bd} for both SiC planar and trench discrete MOSFETs. Although the oxide lifetime of trench devices is highly variable, the Q_{bd} is uniformly distributed. This indicates that the gate oxide tends to break down when the total charge passing through it exceeds a certain threshold, and the charge-to-breakdown mechanism can be used to explain oxide intrinsic breakdown.

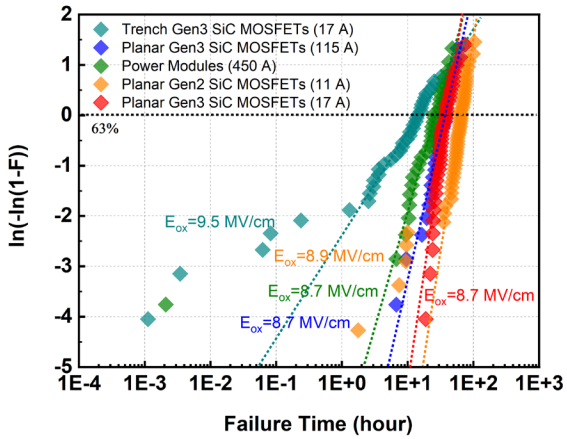

Fig. 2. Weibull distribution of measured oxide lifetimes for commercial SiC discrete MOSFETs and power modules.

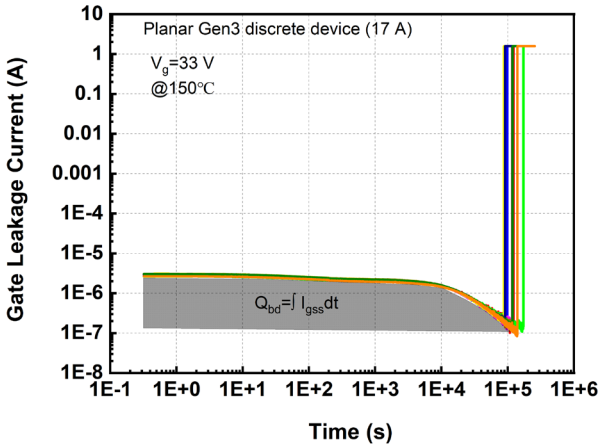

Fig. 3. Constant-voltage TDDB test curves for SiC planar 17 A discrete MOSFETs.

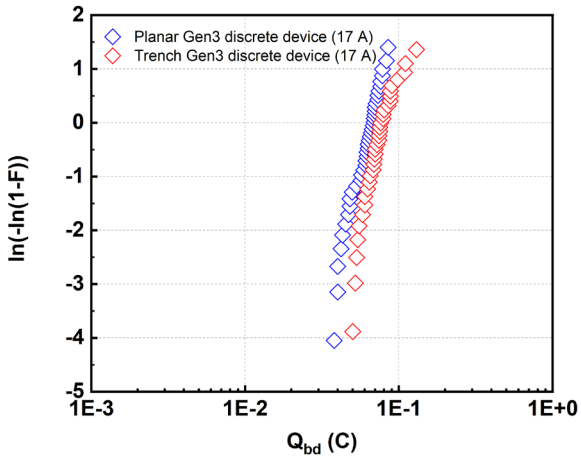

Fig. 4. Weibull distribution of Q_{bd} extracted from constant-voltage TDDB.

Fig. 5 illustrates the oxide lifetime at 150°C with failure rates of 63%, 1%, and 10 ppm for SiC planar 17 A discrete MOSFETs, calculated from Weibull statistics. It can be seen that planar 17 A discrete device with t_{bd} less than t_{10ppm} cannot meet the lifetime requirement of 20 years under operational conditions. To establish the relationship between gate leakage current and oxide lifetime for SiC planar 17 A MOSFETs, I_{gss} is measured at both 30 V@RT and 34 V@150°C. The measured I_{gss} values are correlated with the oxide lifetime at 34 V@150°C for each device, as depicted in Fig. 6 (a) and (b). Based on the negative correlation between t_{bd} and I_{gss}, SiC planar 17 A MOSFETs

with an I_{gss} greater than ~ 0.3 μA at 30 V @RT, and ~ 30 μA at 34 V@150℃ may exhibit a shorter lifetime than t_{10ppm}. It can also be found that devices with higher I_{gss} at 30 V@RT also exhibit higher I_{gss} at high V_g@150℃.

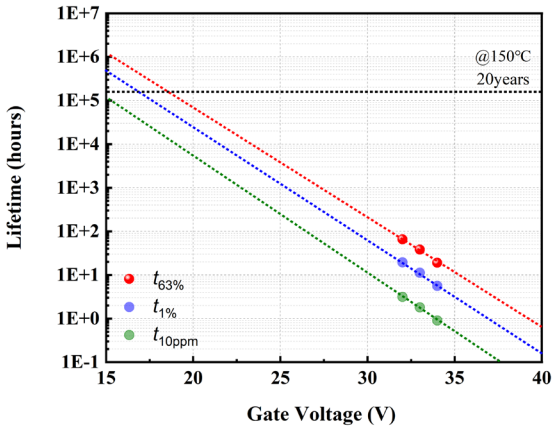

Fig. 5. Oxide lifetimes at 150℃ with the failure rate of 63%, 1% and 10 ppm for SiC planar 17 A discrete MOSFETs.

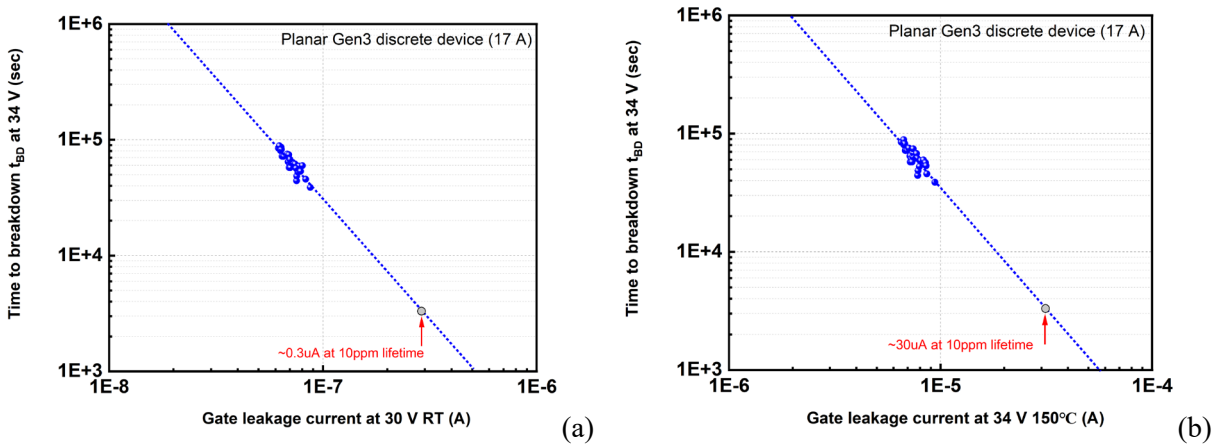

Fig. 6. Correlation between gate leakage current and oxide lifetime for SiC planar 17 A discrete MOSFETs: (a) I_{gss} at 30 V@RT vs. oxide lifetime at 34 V@150℃. (b) I_{gss} at 34 V@150℃ vs. oxide lifetime at 34 V@150℃.

The same negative correlation is observed in other commercial devices, as shown in Fig. 7. Higher gate leakage current in SiC MOSFETs correlates with shorter oxide lifetime. According to recent studies, the charge-to-breakdown mechanism provides a reasonable explanation for intrinsic oxide breakdown. This mechanism suggests that a certain amount of charge must be transported before breakdown occurs. During the TDDB test, the gate leakage current primarily consists of electrons injected into the SiO_2 conduction band from SiC via FN tunneling. The FN tunneling current density can be expressed by Eq. 1, which shows that leakage current density depends on the oxide electric field (E_{ox}). Due to variations in fabrication, there are differences in effective oxide thickness (t_{ox}) between devices. A smaller t_{ox} results in a larger E_{ox} at the same gate voltage, leading to higher leakage current in devices. Since Q_{bd} is a constant value, devices with higher leakage current will exhibit shorter lifetimes. Extrinsic breakdown can be described as defect-related breakdown. This breakdown is caused by irregularities in the SiO_2, or the surface and interface roughness. The tiny distortions lead to thickness fluctuation. In this case, locally enhanced electric field near the steps accelerates oxide breakdown. Also, the enhanced electric field at the defect site can increase the locally leakage current. Based on the present results, not all devices with extrinsic failures have large

leakage current. The total leakage current may depend on the type of defect, the location of the defect and the defect density. The physical mechanism of extrinsic breakdown requires further study.

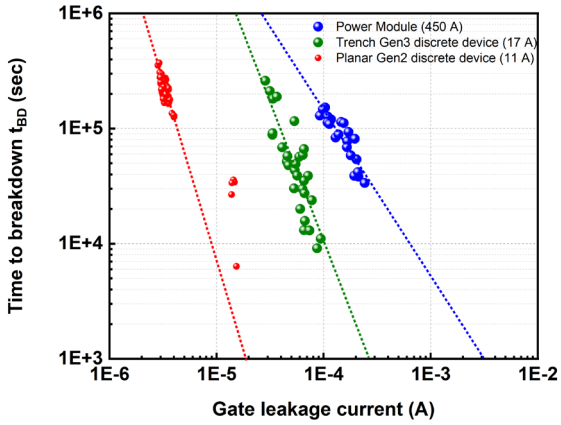

Fig. 7. Correlation between the gate leakage current and the oxide lifetime for SiC discrete MOSFETs and power modules.

Based on the above test results and analysis. An optimized screening technique based on leakage current is proposed. This approach is to obtain I_{gss} by applying gate voltage and identify SiC MOSFETs with low oxide lifetime according to the value of I_{gss}. Generally, devices with higher I_{gss} at low voltage and RT also exhibit higher I_{gss} at elevated temperatures and voltages. However, high temperature and high voltage conditions are more effective in screening out devices prone to infant failures. Therefore, high temperature and high voltage conditions serve not only as a test for I_{gss} but also as a screening process for the devices. Previous studies have shown that during 100 ms screening at 150°C, the maximum acceptable oxide electric fields for SiC planar and trench MOSFETs, without causing negative threshold voltage shifts, are 9 MV/cm and 8 MV/cm, respectively [16,17].

To demonstrate the effectiveness of this method, two new batches of SiC MOSFETs with planar and trench gate structures are selected for screening and TDDB testing. Fig. 8 (a) and (b) show the gate leakage current under different stress conditions and the t_{bd} distribution for each SiC planar and trench MOSFET, respectively. As shown in Fig. 8 (a), there are five leaky SiC planar MOSFETs detected at 30 V @RT and 34 V @150°C. Five leaky devices do not exhibit oxide failure after undergoing the I_{gss} test. Subsequently, the oxide lifetime is measured using the TDDB test. The results show that oxide failure time of these five devices is in the range of 1.7 and 10 hours, which is lower than the oxide lifetime of normal devices. Fig. 8 (b) shows the I_{gss} distribution of SiC trench MOSFETs at 30 V @RT and 8 MV/cm @150°C. It can be observed that the gate oxide of one device fails under the stress of 8 MV/cm @150°C, which can be considered as an infant failure. The remaining SiC trench MOSFETs have a large variation in I_{gss} despite passing the I_{gss} test without breakdown. For trench devices with large oxide lifetime variation, a portion of the devices with I_{gss} exceeding a certain range can be removed, allowing the remaining devices to exhibit higher lifetime uniformity. It can be concluded that the screening method proposed in this paper considers SiC MOSFETs that exhibit higher I_{gss} at different oxide stress conditions as devices that will experience non-infant failure. By removing these devices, the failure probability is reduced. In addition, the process used to measure I_{gss} can also eliminate devices with infant failures.

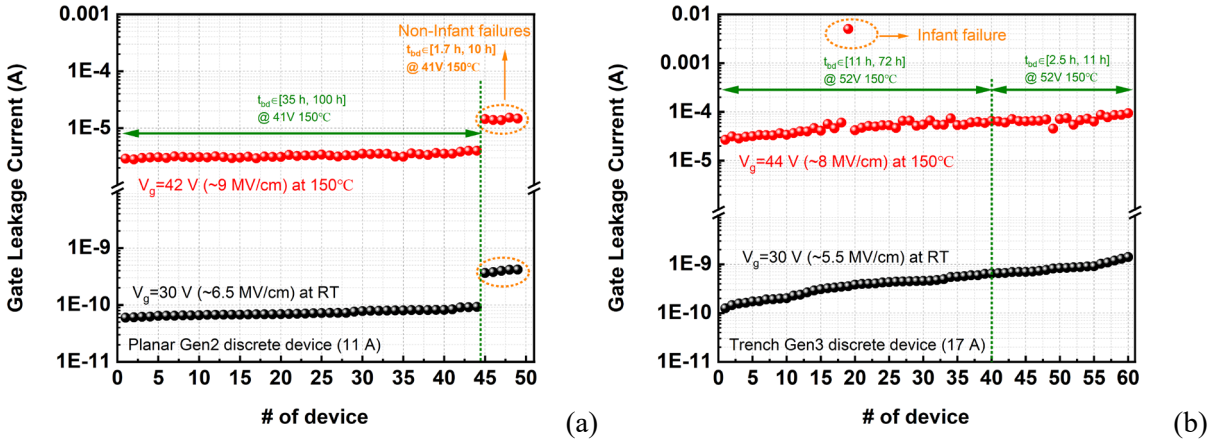

Fig. 8. Gate leakage current under different stress conditions for:
(a) SiC planar 11 A discrete MOSFETs. (b) SiC trench discrete MOSFET.

Summary

This study proposes a screening method to reduce the probability of gate oxide failure in commercial SiC MOSFETs, based on the observed negative correlation between I_{gss} and t_{bd}. The results indicate that devices with higher I_{gss} tend to have shorter oxide failure times. By removing leaky SiC MOSFETs, the intrinsic oxide lifetime distribution of the remaining devices becomes more uniform. Additionally, I_{gss} measurements under high-temperature and high-voltage conditions help to identify and eliminate some infant failures.

References

[1] T. Aichinger, M. Schmidt, Gate-oxide reliability and failure-rate reduction of industrial SiC MOSFETs, in: 2020 IEEE International Reliability Physics Symposium (IRPS), IEEE, Dallas, TX, USA, 2020: pp. 1–6. https://doi.org/10.1109/IRPS45951.2020.9128223.

[2] T. Liu, S. Zhu, M. Jin, L. Shi, M.H. White, A.K. Agarwal, Impacts of Area-Dependent Defects on the Yield and Gate Oxide Reliability of SiC Power MOSFETs, in: 2021 IEEE 8th Workshop on Wide Bandgap Power Devices and Applications (WiPDA), IEEE, Redondo Beach, CA, USA, 2021: pp. 5–8. https://doi.org/10.1109/WiPDA49284.2021.9645099.

[3] H. Miki, M. Sagawa, Y. Mori, T. Murata, K. Kinoshita, K. Asaka, T. Oda, Accurate screening of defective oxide on SiC using consecutive multiple threshold-voltage measurements, in: 2022 IEEE International Reliability Physics Symposium (IRPS), 2022: p. 8B.2-1-8B.2–7. https://doi.org/10.1109/IRPS48227.2022.9764583.

[4] J. Berens, T. Aichinger, A straightforward electrical method to determine screening capability of GOX extrinsics in arbitrary, commercially available SiC MOSFETs, in: 2021 IEEE International Reliability Physics Symposium (IRPS), 2021: pp. 1–5. https://doi.org/10.1109/IRPS46558.2021.9405152.

[5] Y. Zheng, R. Potera, T. Witt, Characterization of Early Breakdown of SiC MOSFET Gate Oxide by Voltage Ramp Tests, in: 2021 IEEE International Reliability Physics Symposium (IRPS), IEEE, Monterey, CA, USA, 2021: pp. 1–5. https://doi.org/10.1109/IRPS46558.2021.9405196.

[6] L. Shi, T. Liu, S. Zhu, J. Qian, M. Jin, H.L.R. Maddi, M.H. White, A.K. Agarwal, Effects of Oxide Electric Field Stress on the Gate Oxide Reliability of Commercial SiC Power MOSFETs, in: 2022 IEEE 9th Workshop on Wide Bandgap Power Devices & Applications (WiPDA), IEEE, Redondo Beach, CA, USA, 2022: pp. 45–48. https://doi.org/10.1109/WiPDA56483.2022.9955295.

[7] L. Shi, S. Zhu, J. Qian, M. Jin, M. Bhattacharya, M.H. White, A.K. Agarwal, A. Shimbori, T. Liu, Investigation of different screening methods on threshold voltage and gate oxide lifetime of SiC Power MOSFETs, in: 2023 IEEE International Reliability Physics Symposium (IRPS), IEEE, Monterey, CA, USA, 2023: pp. 1–7. https://doi.org/10.1109/IRPS48203.2023.10118276.

[8] L. Shi, J. Qian, M. Jin, M. Bhattacharya, H. Yu, M.H. White, A.K. Agarwal, A. Shimbori, Evaluation of Burn-in Technique on Gate Oxide Reliability in Commercial SiC MOSFETs, in: 2024 IEEE International Reliability Physics Symposium (IRPS), IEEE, Grapevine, TX, USA, 2024: pp. 1–6. https://doi.org/10.1109/IRPS48228.2024.10529373.

[9] Z. Chbili, A. Matsuda, J. Chbili, J.T. Ryan, J.P. Campbell, M. Lahbabi, D.E. Ioannou, K.P. Cheung, Modeling Early Breakdown Failures of Gate Oxide in SiC Power MOSFETs, IEEE Trans. Electron Devices 63 (2016) 3605–3613. https://doi.org/10.1109/TED.2016.2586483.

[10] M. Lenzlinger, E.H. Snow, Fowler-Nordheim tunneling into thermally grown SiO2, IEEE Transactions on Electron Devices 15 (1968) 686–686. https://doi.org/10.1109/T-ED.1968.16430.

[11] P. Moens, J. Franchi, J. Lettens, L.D. Schepper, M. Domeij, F. Allerstam, A Charge-to-Breakdown (Q_{BD}) Approach to SiC Gate Oxide Lifetime Extraction and Modeling, in: 2020 32nd International Symposium on Power Semiconductor Devices and ICs (ISPSD), IEEE, Vienna, Austria, 2020: pp. 78–81. https://doi.org/10.1109/ISPSD46842.2020.9170097.

[12] J. Qian, L. Shi, M. Jin, M. Bhattacharya, A. Shimbori, H. Yu, S. Houshmand, M.H. White, A.K. Agarwal, Modeling of Charge-to-Breakdown with an Electron Trapping Model for Analysis of Thermal Gate Oxide Failure Mechanism in SiC Power MOSFETs, Materials 17 (2024) 1455. https://doi.org/10.3390/ma17071455.

[13] J. Qian, L. Shi, M. Jin, M. Bhattacharya, H. Yu, M.H. White, A.K. Agarwal, A. Shimbori, Z. Xu, Investigation of the Constant Current Stress for Charge-to-breakdown Extraction in Commercial SiC Power MOSFETs, in: 2023 IEEE 10th Workshop on Wide Bandgap Power Devices & Applications (WiPDA), IEEE, Charlotte, NC, USA, 2023: pp. 1–4. https://doi.org/10.1109/WiPDA58524.2023.10382231.

[14] S. Zhu, T. Liu, L. Shi, M. Jin, H.L.R. Maddi, M.H. White, A.K. Agarwal, Comparison of Gate Oxide Lifetime Predictions with Charge-to-Breakdown Approach and Constant-Voltage TDDB on SiC Power MOSFET, in: 2021 IEEE 8th Workshop on Wide Bandgap Power Devices and Applications (WiPDA), IEEE, Redondo Beach, CA, USA, 2021: pp. 1–4. https://doi.org/10.1109/WiPDA49284.2021.9645100.

[15] W. Weibull, A Statistical Distribution Function of Wide Applicability, Journal of Applied Mechanics 18 (1951) 293–297. https://doi.org/10.1115/1.4010337.

[16] L. Shi, J. Qian, M. Jin, M. Bhattacharya, H. Yu, A. Shimbori, M.H. White, A.K. Agarwal, Investigation on gate oxide reliability under gate bias screening for commercial SiC planar and trench MOSFETs, Materials Science in Semiconductor Processing 174 (2024) 108194. https://doi.org/10.1016/j.mssp.2024.108194.

[17] L. Shi, J. Qian, M. Jin, M. Bhattacharya, H. Yu, M.H. White, A.K. Agarwal, A. Shimbori, Z. Xu, An Effective Screening Technique for Early Oxide Failure in SiC Power MOSFETs, in: 2023 IEEE 10th Workshop on Wide Bandgap Power Devices & Applications (WiPDA), IEEE, Charlotte, NC, USA, 2023: pp. 1–4. https://doi.org/10.1109/WiPDA58524.2023.10382194.