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Achieving Low D_{it} (~5×10^{10}eV^{-1}cm^{-2}), Competitive J_G (~ 5×10^{-10} A cm^{-2}) Performance and Enhanced Post-Stress Flatband Voltage Stability Using Deposited Oxide

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Abstract. In this work, we propose and experimentally validate a novel approach to achieve superior interface properties of the SiO_2/SiC MOS capacitors through a low-temperature oxide deposition technique for gate dielectric followed by a nitridation process. Low interface trap density (~ 5×10^{10} eV^{-1}cm^{-2}), robust flat-band voltage stability under positive bias stress, and decent leakage current density (J_G ~ 5×10^{-10} A cm^{-2}) can be unambiguously verified after nitric oxide (NO) gas post-deposition annealing.

Introduction

Silicon carbide (SiC) power MOSFETs are a key enabling technology in high-efficiency power electronics applications, particularly in systems requiring high voltage, high temperature, and high switching frequency. Despite their promise, one of the primary challenges SiC MOSFETs faces is their inherently low channel mobility, which limits overall device performance[1,2]. This issue is largely attributed to the high interface trap density (Dit) at the SiO_2/SiC interface, primarily caused by carbon-related defects formed during the high-temperature oxidation process to create the gate dielectric layer [2,3]. These defects introduce unwanted energy states within the bandgap, which act as traps, reducing the mobility of carriers and thereby degrading the on-state performance of the device.

Various strategies have been explored to mitigate these challenges, including modifications to the oxidation process and post-oxidation annealing treatments. Traditional oxidation methods at high temperatures often result in significant carbon contamination at the SiC interface, increasing the density of interface traps. Low-temperature deposition techniques have recently emerged as a promising alternative. These methods offer better control over the interface properties, reducing carbon-related defects and thus improving channel mobility [4,5]. However, despite the advantages,

the precise impact on long-term device reliability and performance remains an open area of research. A deeper understanding of the SiO_2/SiC interface engineering under these conditions is crucial to unlocking the full potential of SiC MOSFETs.

In this work, we explore the effectiveness of a low-temperature deposited oxide as a gate dielectric in mitigating interface-related challenges in SiC MOSFET technology. Our results show that the deposited oxide approach yields a minimal D_{it} of ~ 5×10^{10} $eV^{-1}cm^{-2}$, excellent device-to-device uniformity, decent leakage current density (J_G), and superior flat-band voltage stability (V_{FB}) under positive bias stress.

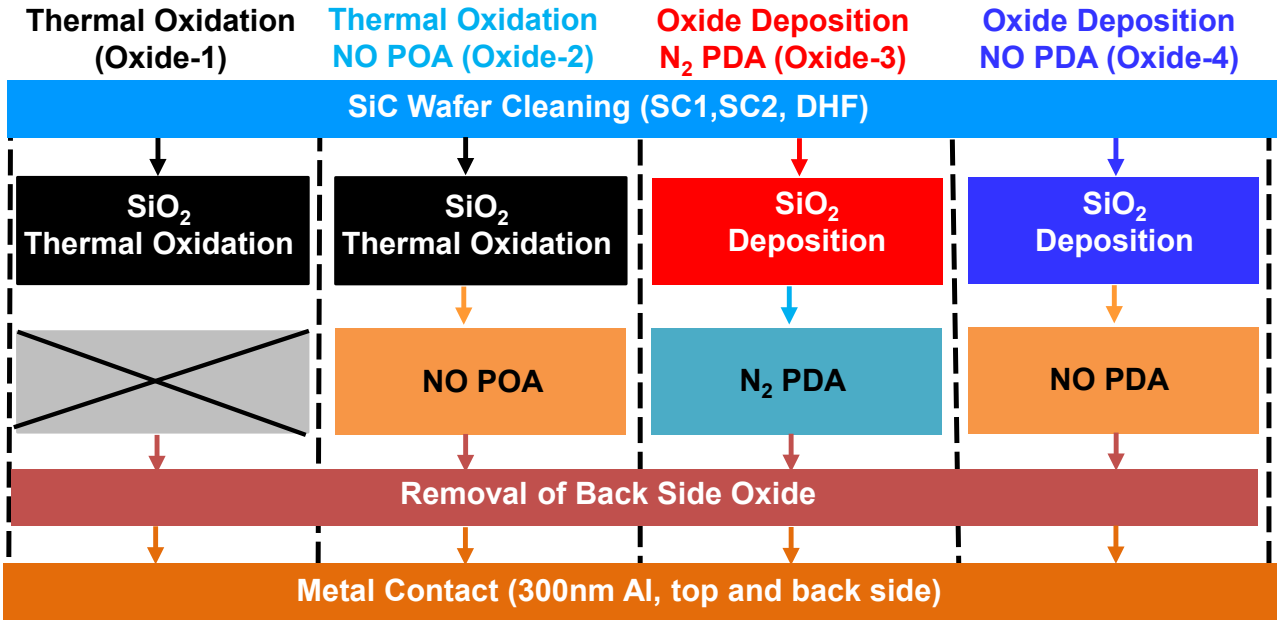


Fig. 1. Fabrication process flow for the SiO_2/SiC MOS capacitors.

Result and Discussion

SiO_2/SiC MOS capacitors were fabricated on a highly doped n-type 4° off-cut (0001) 4H-SiC substrate, with a 10 µm thick nitrogen-doped homo-epilayer. Key aspects of the process flow are illustrated in Fig. (1). High-resolution transmission electron microscopy (HRTEM) images were obtained for all the samples to investigate the presence of an additional layer at the SiO_2/SiC interface following post-oxidation/deposition annealing (POA/PDA). A sharp interface can be seen between SiO_2 and SiC [Fig. 2(a-b)]. To access device yield and uniformity, we randomly selected 15 devices of the same die and measured J_G [Fig. 3(a)]. The tight statistical distribution of J_G for randomly selected devices is shown in Fig. 3(b). Capacitance-voltage (C-V) measurement was conducted to investigate the impact of different methods on the SiO_2/SiC interface [Fig. 3(c-f)]. The oxide-4 devices significantly reduce D_{it} to ~ 5×10^{10} $eV^{-1}cm^{-2}$ [Fig. 4(a)], which may be attributed to the effective mitigation of carbon-related defects in deposited oxide, and the incorporation of nitrogen may further passivate dangling bonds at the SiO_2/SiC interface after NO POA. The tight distribution with small coefficient of variation (σ/μ) is observed for D_{it} [Fig. 4(b)]. X-ray photoelectron spectroscopy (XPS) study supported the existence of a slightly nitrogen-rich SiC surface after NO POA/PDA [Fig. 4(c)].

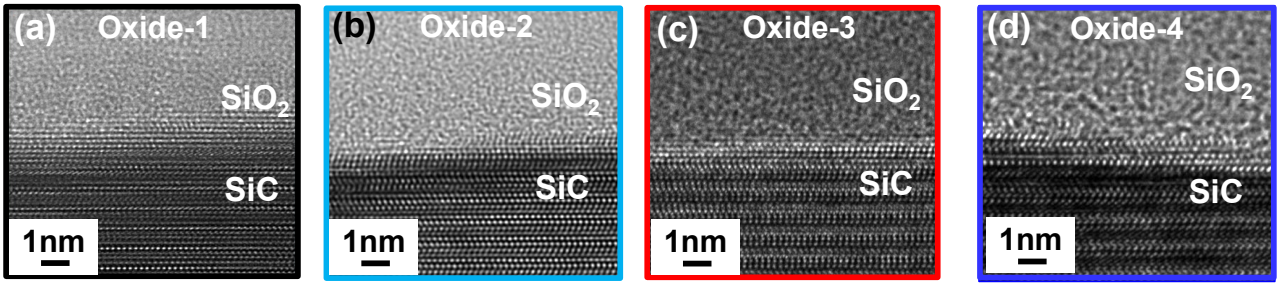


Fig. 2. (a-d) Cross-sectional TEM of the SiO_2/SiC interface for all the samples.

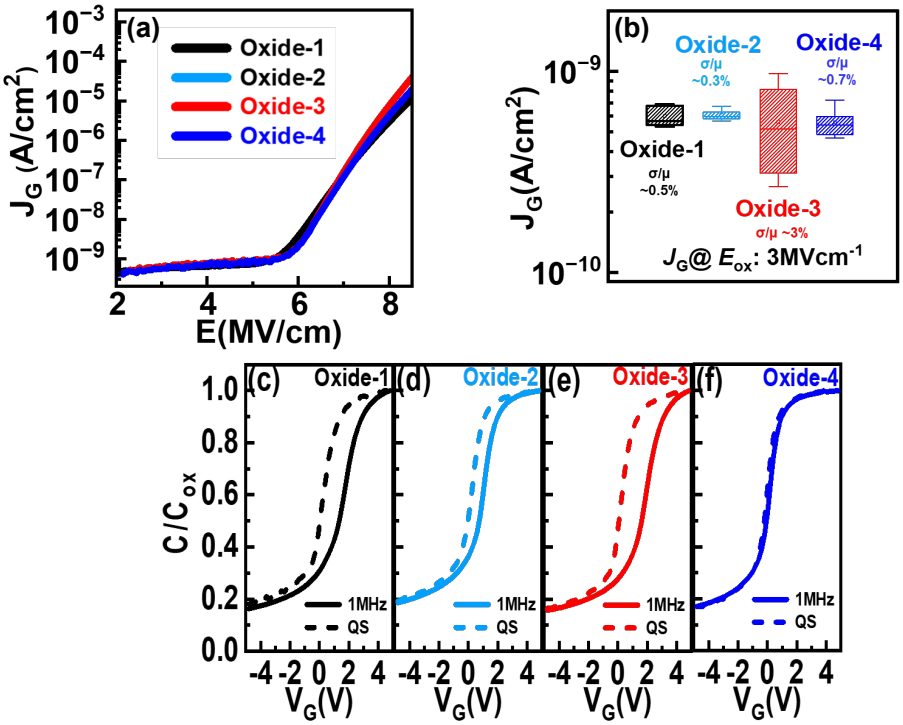


Fig. 3. (a) J_G -V_G for the SiC/SiO_2 MOS capacitors and (b) statistical distribution of J_G for randomly selected devices and (c-f) quasi static and 1 MHz C–V curves of the SiO_2/SiC MOS capacitors.

Next, the *C–V* measurements were repeated from −5 V to various accumulation voltages from 5 V to 25 V [Fig. 5(a-d)] to investigate the effect of high accumulation voltage on flat-band (V_{FB}) stability. The improved V_{FB} stability for the oxide-4 devices could be due to the reduction of interface defects and near interface traps at the SiO_2/SiC interface. Furthermore, we examined the V_{FB} stability by conducting a positive bias stress test. The oxide field (E_{ox}) is applied according to industry guidelines to ensure accurate and reliable testing procedures [10]. A constant voltage stress corresponding to E_{ox} values of 3, 5, and 7 MV/cm was applied for a duration of up to 10^3 s [Fig. 5(e-h)]. The bulk trap density (ΔN_{ox}) extracted as a function of bias stress time with various E_{ox} values of 3, 5, and 7 MV/cm shown in Fig. 6(a-d). The oxide-4 scheme device manifests superior V_{FB} stability against bias stress with the lowest extracted ΔN_{ox}.

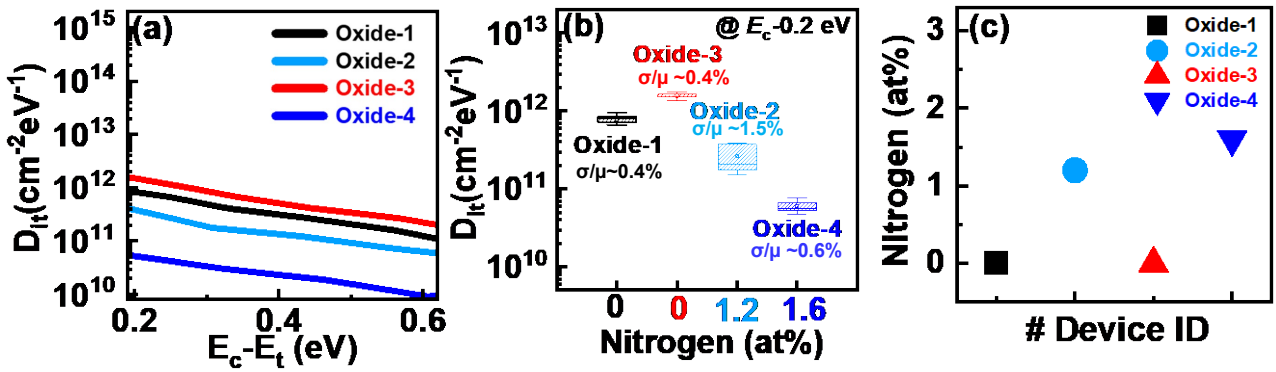


Fig. 4. (a) energy distribution of D_{it} estimated by the high-low method [2], (b) the distribution of D_{it} extracted at around E_c-0.2 eV, and (c) nitrogen concentration plotted for for all samples.

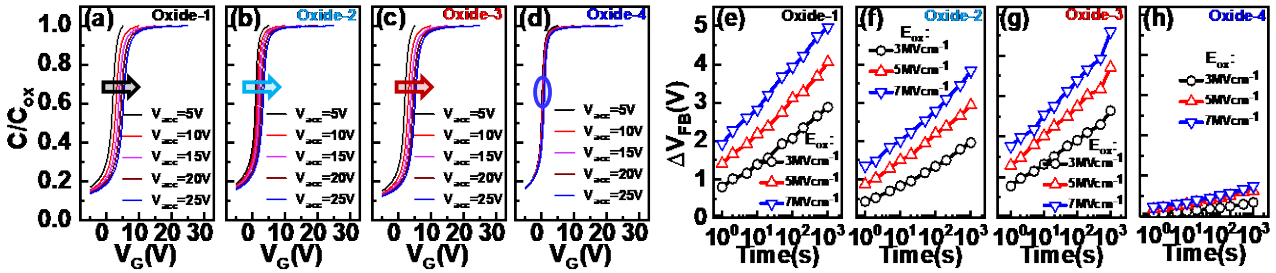
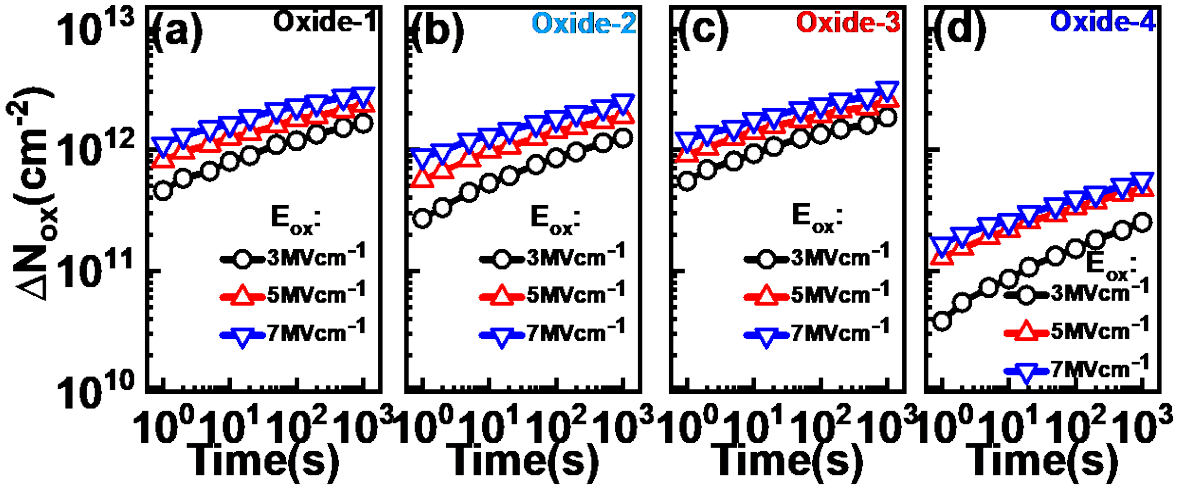
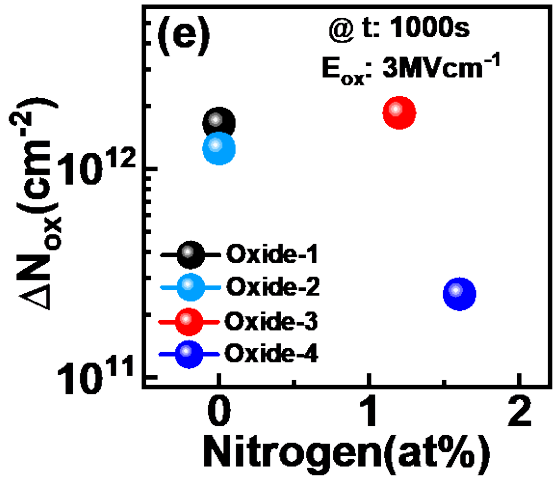


Fig. 5. (a-d) *C-V* curves with different accumulation voltages of the SiO_2/SiC MOS capacitors and (e-h) ΔV_{FB} as a function of bias stress time with various E_{ox} of 3, 5, and 7 MV/cm.

This can be attributed to the minimization of carbon-related defects through the deposited oxide approach, in which the trap states are further reduced by NO-PDA. Finally, we benchmark the D_{it} and J_G of our devices with previously reported deposited oxide SiC devices (Table I). It is reasonable to conclude that the oxide-4 device in this study has achieved the lowest J_G (~ 5×10^{-10} A cm^{-2}) and a satisfactory D_{it} value (~ 5×10^{10} eV^{-1}cm^{-2}).





Ref.	Oxide Deposition Technique	Post Treatment Gas/Tem(°C)/ Time(min)	t_{ox} (nm)	J_G (A/cm^2)	D_{it} (cm^{-2}eV^{-1})
This Work	LPCVD	NO/1300/30	40	5×10^{-10}	5×10^{10}
Ref-4	LPCVD	NO/1175/120	55	-	4×10^{11}
Ref-5	Sputter	CO_2/1250/240	33	1×10^{-9}	2×10^{11}
Ref-6	PECVD	N_2/1175/120	30	-	3×10^{11}
Ref-7	PECVD	N_2/1400/45	30	1×10^{-9}	4×10^{10}
Ref-8	LPCVD	NO/1250/120	50	1×10^{-9}	2×10^{11}
Ref-9	CVD	N_2/1300/600	45	1×10^{-9}	4×10^{11}

Table-1: Benchmark

Fig. 6. (a-d) ΔN_{ox} as a function of bias stress time with various E_{ox} field of 3, 5, and 7 MV/cm. (e) change in ΔN_{ox} plotted as a function of nitrogen concentration and Table-1 Benchmark of this work with reported work.

Conclusion

In summary, our deposited gate oxide on SiC with NO-POA had produced low D_{it} and led to a significant enhancement in MOS capacitor device performance and reliability such as superior V_{FB} stability under positive bias stress.

Acknowledgement

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