Key Engineering Materials
ISSN: 1662-9795, Vol. 1024, pp 29-37
doi:10.4028/p-O0YawH
© 2025 The Author(s). Published by Trans Tech Publications Ltd, Switzerland.
Submitted: 2024-09-20
Accepted: 2025-05-05
Online: 2025-09-12

Investigation of Overcurrent Turn-Off Robustness of 1200 V SiC MOSFETs

Madhu Lakshman Mysore[1,a*], Darshan Koorana Prasanna Kumar[2,b], Chaohao Wang[1,c], Josef Lutz[1,d], Thomas Basler[1,e]

[1]Chemnitz University of Technology, Chair of Power Electronics, Chemnitz, Germany

[a*]madhu-lakshman.mysore@etit.tu-chemnitz.de,
[b]darshan-koorana.prasanna-kumar@etit.tu-chemnitz.de, [c]chaohao.wang@etit.tu-chemnitz.de,
[d]josef.lutz@etit.tu-chemnitz.de, [e]thomas.basler@etit.tu-chemnitz.de

Keywords: Overcurrent turn-off, Robustness, Gate-leakage, Gate oxide, Electric field, TCAD.

Abstract. The aim of this study is to investigate the overcurrent turn-off robustness limit of SiC MOSFETs from three different manufacturers with three different cell technologies up to very high turn-off currents to determine a possible destruction limit and failure type. The influence of the negative gate-source voltage ($V_{GS,off}$) was studied because of the high drain-source overvoltage in connection with the decreased $V_{GS,off}$, which is the most critical point for the gate oxide field stress for the different cell technologies. All measurements were performed at a positive gate-source voltage ($V_{GS,on}$) above the specified datasheet values to reach high currents without channel pinch-off. In addition, the influence of temperature on the overcurrent robustness was studied. Finally, TCAD simulations were performed to determine the reason for the failure mechanism under the overcurrent turn-off conditions. All the manufacturer devices can withstand several times higher gate-source voltages under overcurrent conditions than the values recommended in the datasheet.

Introduction

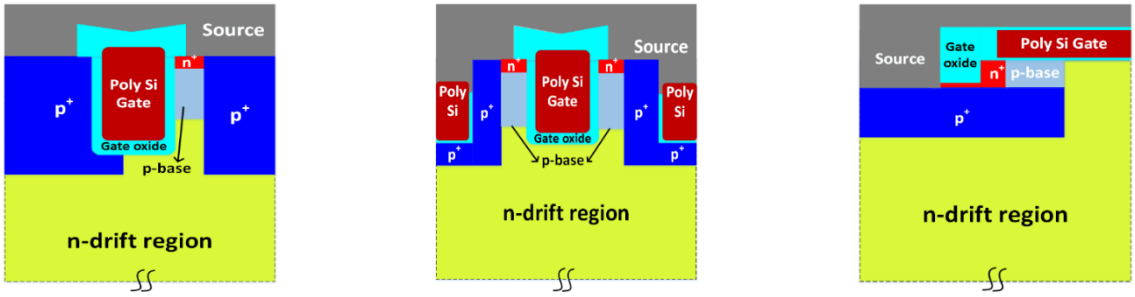
Silicon Carbide (SiC) power MOSFETs are widely adopted in various applications due to their superior material properties such as low intrinsic carrier density, high breakdown field, and high thermal conductivity [1]. Owing to their material advantages, SiC-based power devices can achieve higher operating temperatures, faster switching speeds and lower conduction losses than those of Si IGBTs.

SiC MOSFETs are used in various applications such as electric vehicles, motor drives, and renewable energy systems. For example, on-board chargers or wind turbine converters must handle overcurrent events due to grid faults or sudden changes in wind speed. During an overcurrent event, a SiC MOSFET might be subjected to excessive current levels beyond its rated specifications. In response to an overcurrent event, SiC MOSFETs must also able to turn-off high currents to protect the device and circuitry. This leads to significant voltage spikes due to the parasitic inductive components of the switching circuits. As a result, the device may operate in avalanche mode which can lead to a catastrophic failure of the device. Moreover, the SiC MOSFETs have thinner gate oxide and can withstand one order magnitude of higher electric field in the bulk than its Si counterparts. These very high voltage spikes can be critical for the gate oxide. Hence, to ensure the stable operation of such systems, it is important to understand the overcurrent turn-off and its limits for SiC MOSFETs under various conditions. In [2] a first study of repetitive overcurrent turn-off events was performed within the recommended gate bias. Although the robustness of SiC MOSFET continues to increase, there are still concerns about the gate oxide reliability [3, 4]. Consequently, in this study, the overcurrent turn-off capabilities of 1.2 kV SiC MOSFETs were evaluated for different cell technologies from three different manufacturers using a double-pulse test. The devices were driven at very high gate voltages, far beyond the allowed range along with various other conditions that strongly influence the dynamic gate switching for the devices. Furthermore, electro-thermal simulations were carried out to investigate overcurrent turn-off failures.

This article is an open access article under the terms and conditions of the Creative Commons Attribution (CC BY) license (https://creativecommons.org/licenses/by/4.0)

Device Under Test and Experimental Setup

The Device Under Test (DUTs) were commercially available 1.2 kV SiC MOSFET from three different manufacturers (M1, M2, and M3) with similar current ratings. These three SiC MOSFETs have different cell technologies, as shown in Fig. 1. The device parameters for the different SiC MOSFETs are listed in Table. 1. The gate oxide thickness was estimated by measuring the gate leakage current until breakdown using a source measurement unit (SMU).

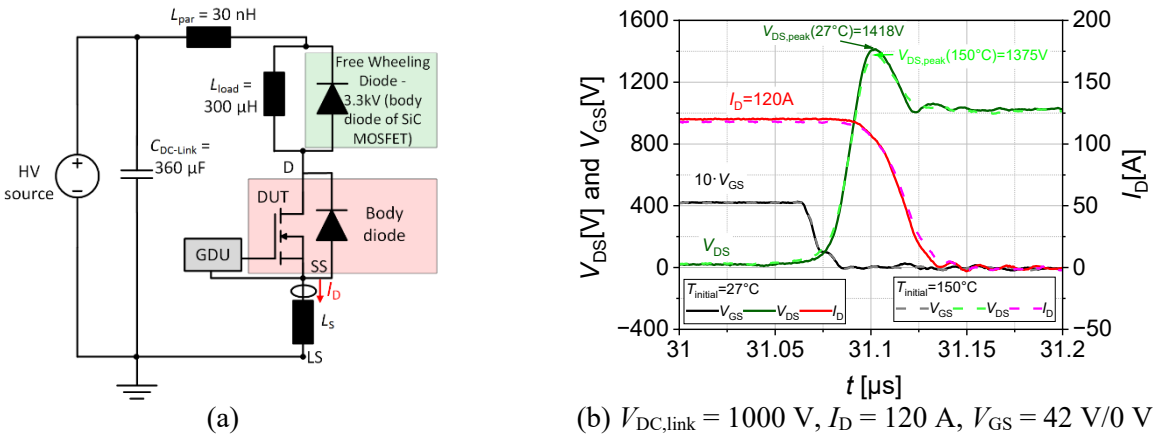


(a) M1 b) M2 c) M3

Fig. 1. Schematic cross-section of the cell head of SiC MOSFETs from different manufacturers.

Table 1. Device parameters of the SiC MOSFETs from different manufacturers.

Device parameters	**M1**	**M2**	**M3**
Gate technology	Trench	Double trench	Planar
Estimated gate oxide thickness	65 nm	55 nm	45 nm
Measured drain-source breakdown voltage at 1 mA (27°C)	1440 V	1615 V	1515V
Rated current	31 A	31 A	32 A
$R_{ds,on}$	80 mΩ	80 mΩ	60 mΩ
Recommended $V_{GS,on}$	20 V	18 V	15 V
Recommended $V_{GS,off}$	0 V	0 V	-4 V
Package type	TO-247-4		



(a) (b) $V_{DC,link}$ = 1000 V, I_D = 120 A, V_{GS} = 42 V/0 V

Fig. 2. (a) Schematic of the overcurrent turn-off equivalent circuit (b) Measured overcurrent turn-off behaviour of M3 devices at two different initial temperatures for given conditions of R_G = 2 Ω, L_{load} = 300 µH.

A schematic diagram of the measurement setup to measure the overcurrent turn-off capability of the SiC MOSFETs is shown in Fig. 2(a). The parasitic inductance (L_{par}) of the commutation loop was 30 nH. A 3.3 kV SiC MOSFET with V_{GS} = 0 V was utilized as a freewheeling diode (FWD). The load inductance (L_{load}) is connected in parallel to the FWD. The magnitude of the turn-off drain current (I_D) of the DUT can be adapted by adjusting the turn-on time (t_{on}). The gate-source voltage (V_{GS}) and drain-source voltage (V_{DS}) were measured at the sense-source (SS) terminal without the influence of load-source inductance (LS). A Rogowski coil was used to measure the current.

An exemplary overcurrent turn-off measurement at a DC-link voltage of 1000 V with V_{GS} switched from 42 V/0 V at two different initial temperatures is shown in Fig. 2(b). At a turn-off current of 120 A, the SiC MOSFETs turn-off with a fast rate of current slope ($\mathrm{d}I_D/\mathrm{d}t$) causing a significant induced overvoltage across the drain and source. The increase in initial junction temperature (T_{inital}) shows slightly lower $\mathrm{d}I_D/\mathrm{d}t$ and subsequently lower overvoltage.

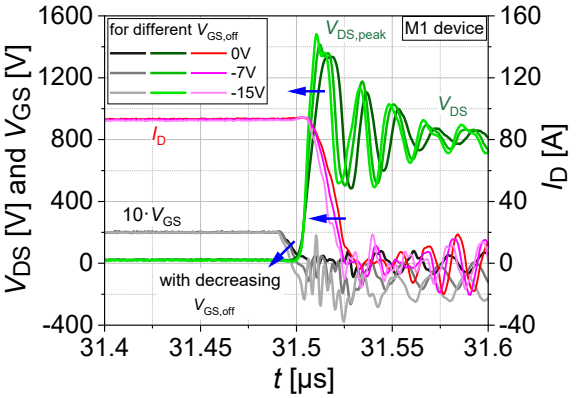


Fig. 3. Impact of negative gate bias on measured overcurrent turn-off for M1 device. Conditions: I_D = 93 A, $V_{GS,on}$ = 20 V, R_G = 2 Ω, L_{par} = 30 nH, $T_{initial}$ = 27°C, $V_{DC,link}$ = 800 V, L_{load} = 300 µH.

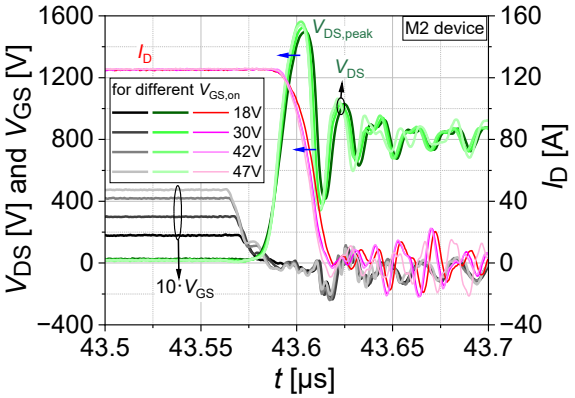


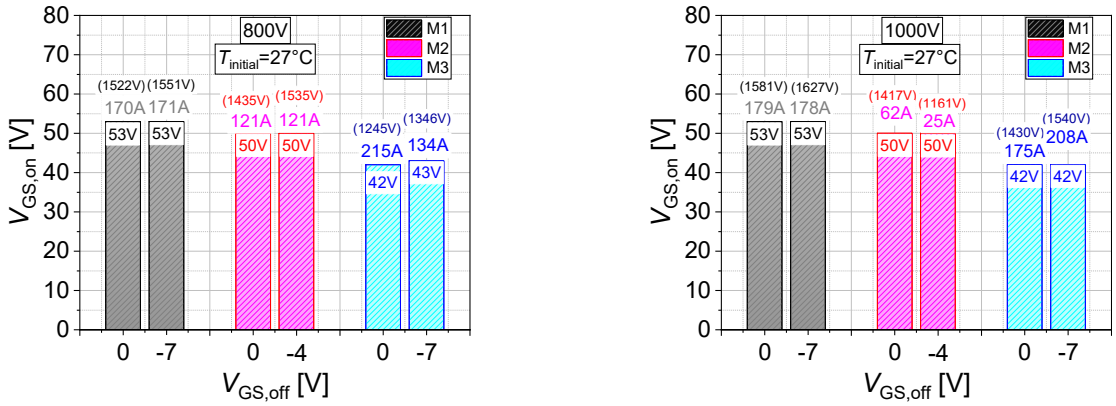
Fig. 4. Impact of positive gate bias on measured overcurrent turn-off for M2 device. Conditions: I_D = 126 A, $V_{GS,off}$ = -4 V, R_G = 2 Ω, L_{par} = 30 nH, $T_{initial}$ = 27°C, $V_{DC,link}$ = 800 V, L_{load} = 300 µH.

The influence of different negative gate voltages on the overcurrent turn-off behaviour of the MOSFET at a fixed $V_{GS,on}$ of 20 V and 800 V is shown in Fig. 3. Due to the higher amplitude in the switched gate bias, an acceleration of the turn-off was recorded. This leads to a higher $\mathrm{d}i_D/\mathrm{d}t$ and correspondingly a higher overvoltage ($V_{DS,peak}$) shortly before avalanche breakdown. In Fig. 4, the positive gate bias was varied at fixed $V_{GS,off}$ of -4 V and DC-link voltage of 800 V for M2 device. The turn-off measurements were carried out at four times the datasheet specified value and showed slightly faster $\mathrm{d}i_D/\mathrm{d}t$ for increased $V_{GS,on}$ values. For both measurements in Fig. 3 and Fig. 4, the $V_{DS,peak}$ was above the rated voltage of the devices to operate at the border of the safe-operating area. At overcurrent turn-off, the voltage and current derivate can be adjusted by varying $V_{GS,on}$ and $V_{GS,off}$.

Results and Analysis

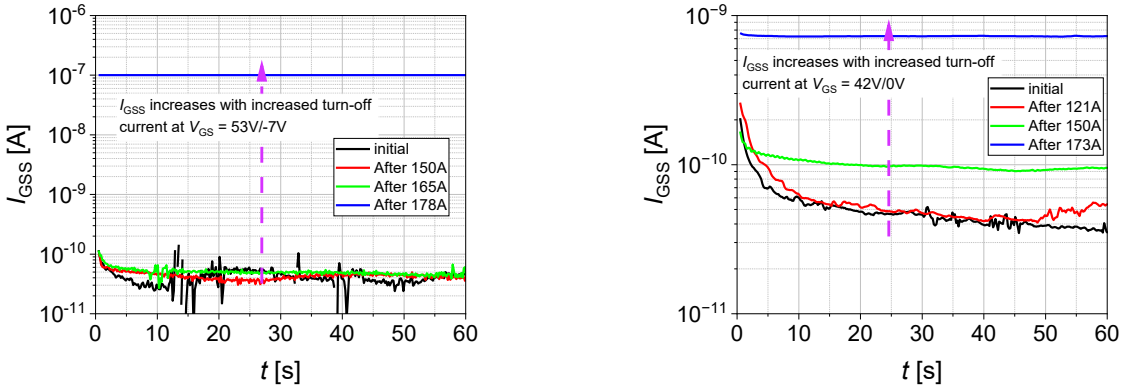
The overcurrent turn-off capability was determined by gradually ramping the drain current in steps of 5 A for a fixed $V_{GS,on}$ and $V_{GS,off}$. Once the channel pinch-off was observed at a high turn-off current, the measurement was stopped, and $V_{GS,on}$ was increased in steps of 1 V. The overcurrent turn-off measurement steps were repeated until the destruction of the DUTs occurred or a strong drift in the electrical parameters was observed, such as gate leakage current (I_{GSS}), or loss of blocking capability or increased drain-source leakage current (I_{DSS}).

At $T_{initial}$ = 27°C: Fig. 5 shows the overcurrent turn-off robustness limit with the help of the last-pass $V_{GE,on}$ for different manufacturers at two different DC-link voltages. The minimum allowed $V_{GS,off}$ values, was chosen as recommended by the datasheet. For measurements below 800 V, the devices do not exhibit any failures in the investigated current ranges for all manufacturers. M1 devices show the highest robustness limit with last-pass $V_{GS,on}$ of 53 V for two different $V_{GS,off}$. M1 SiC MOSFETs exhibit the highest last-pass $V_{GS,on}$ for both DC-link voltages as compared to other manufacturers because of thicker gate oxide as mentioned in Table 1. Moreover, the M2 devices at 1000 V and V_{GS} switched from 50 V to -4 V shows lower overcurrent turn-off capability as compared to V_{GS} switched from 50 V to 0 V. M3 devices at 800 V show increased last-pass $V_{GS,on}$ by 1 V with lower $V_{GS,off}$. Furthermore, at 1000 V and $V_{GS,off}$ of -4 V, the M3 device shows higher overcurrent turn-off capability than $V_{GS,off}$ of 0 V, which is in contrast to M2 devices.



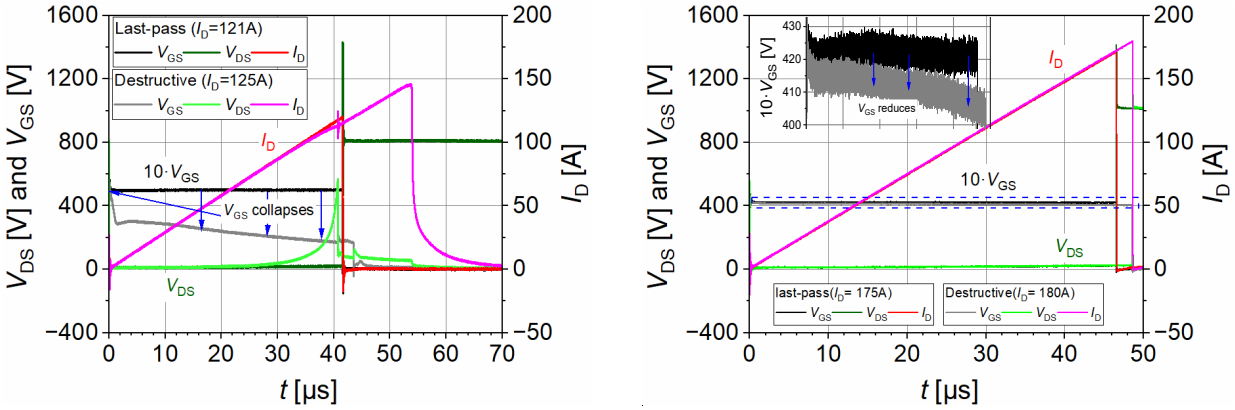
(a) DC-link of 800 V (b) DC-link of 1000 V

Fig. 5. Overcurrent turn-off robustness of the different manufacturers: last-pass $V_{GS,on}$ for two different $V_{GS,off}$. The last-pass current and its $V_{DS,peak}$ of the devices are mentioned on the top of each bar along with last-pass $V_{GS,on}$. Measurement conditions: L_{load} = 300 µH, R_G = 2 Ω, $T_{initial}$ = 27°C, L_{par} = 30 nH.



(a) For M1 device at V_{GS} = 53 V/-7 V (b) For M3 device at V_{GS} = 42 V/0 V

Fig. 6. Measured I_{GSS} in between overcurrent turn-off measurements at DC-link voltage of 1000 V for different manufacturers at $T_{initial}$ = 27°C. Note: change in y-axis scale.

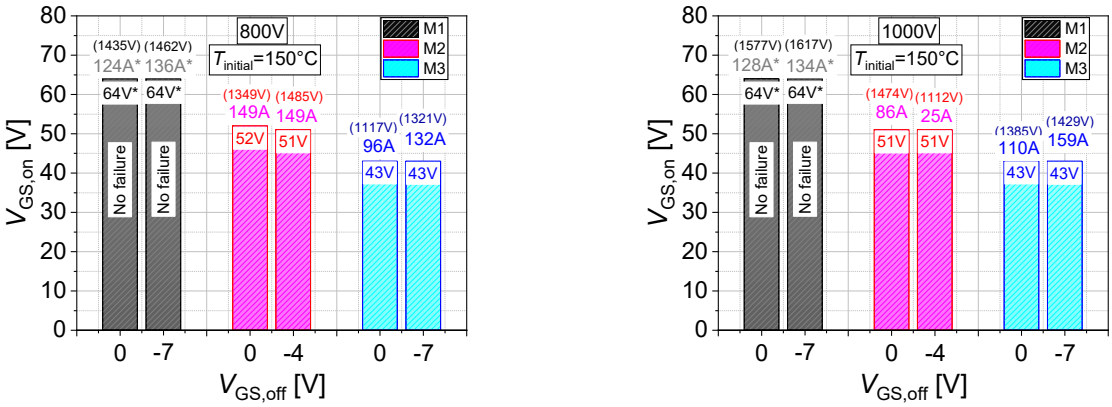


(a) M2 at $V_{DC,link}$ = 800 V, V_{GS} = 50 V/0 V (b) M3 at $V_{DC,link}$ = 1000 V, V_{GS} = 42 V/0 V

Fig. 7. Comparison of the last-pass and destructive pulses at overcurrent turn-off of the SiC MOSFETs for (a) M2 (b) M3 at a given condition of L_{load} = 300 µH, R_G = 2 Ω, $T_{initial}$ = 27°C. Inset: zoomed V_{GS} of the last-pass and destructive pulses.

All the devices failed due to an increased I_{GSS} independent of the manufacturer. The measured I_{GSS} in between the current pulses shows an increased leakage current for a higher turn-off current, as shown in Fig. 6. The M1 devices however do not show a significant change in I_{GSS} with increased turn-off current, but a sudden increase in I_{GSS} after turn-off current of 178 A with V_{GS} of 53 V/-7 V,

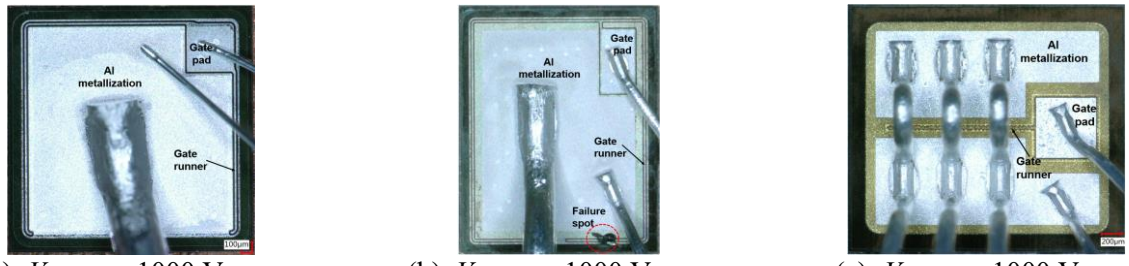
as shown in Fig. 6(a). Conversely, the M3 devices show a slight increase in I_{GSS} with higher turn-off current, as shown in Fig. 6(b). This increase in the I_{GSS} indicates pre-damage to the gate before the destructive overcurrent turn-off pulse. Any further overcurrent turn-off measurements with increased I_{GSS} will lead to catastrophic failure or a gate voltage drop, as shown in Fig. 7. A sudden V_{GS} collapse at the beginning of pulse for M2 devices, eventually leading to failure is plotted in Fig. 7(a). Moreover, M3 devices show a drop in the $V_{GS,on}$ value during V_{GS} steady state phase, indicating gate damage and correspondingly increased I_{GSS} above the maximum datasheet values [see inset Fig. 7(b)].



(a) DC-link of 800 V (b) DC-link of 1000 V

Fig. 8. Overcurrent turn-off robustness of the different manufacturers: last-pass $V_{GS,on}$ for two different $V_{GS,off}$. The last-pass current and its $V_{DS,peak}$ of the devices are mentioned on the top of each bar along with last-pass $V_{GS,on}$. Measurement conditions: L_{load} = 300 µH, R_G = 2 Ω, $T_{initial}$ = 150°C, L_{par} = 30 nH.

At $T_{initial}$ = 150°C: In general, all the tested devices from different manufacturers show an increased last-pass $V_{GE,on}$ with increased junction temperature, as shown in Fig. 8. The tendency of the $V_{GE,off}$ influence is similar to the room temperature. Interestingly, the M1 devices show significantly increased overcurrent turn-off capability without any failure up to $V_{GS,on}$ of 64 V. The measurements were stopped at 64 V due to the limitation of the gate driver unit (GDU). Moreover, the M2 and M3 devices show an increased last-pass $V_{GS,on}$ in the range of 1 V to 2 V as compared to the measured results at 27°C (Fig. 5). Furthermore, the increase in last-pass $V_{GS,on}$ was due to the reduced $V_{DS,peak}$ at increased temperatures, see Fig. 2(a). At higher temperatures, the overcurrent turn-off capability of the M2 devices increases. M3 devices show lower overcurrent turn-off capability with increased $T_{initial}$. The M2 and M3 devices showed increased gate leakage currents at last-pass $V_{GS,on}$ and failure types were the same as discussed at room temperature. For all the SiC MOSFETs and both temperatures, the increased gate leakage current is probably due to trap-assisted tunnelling from the generated defects in gate oxide [5].



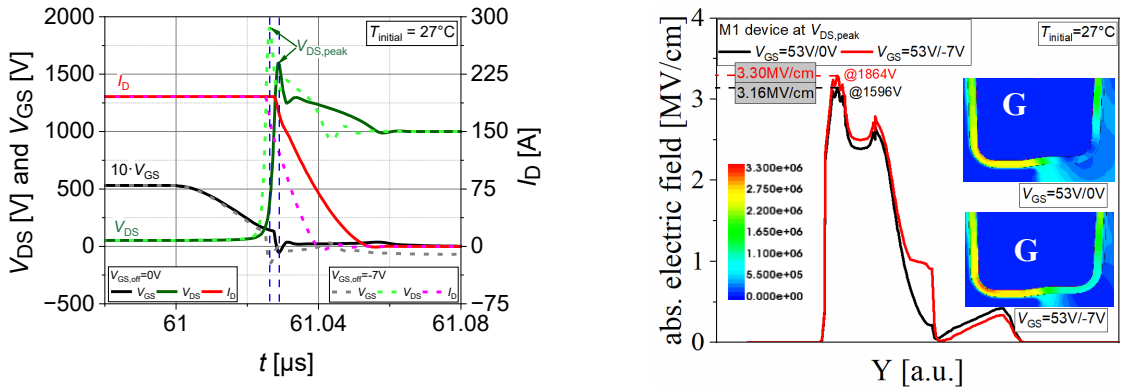
(a) $V_{DC,link}$ = 1000 V, V_{GS} = 53 V/-7 V, $T_{initial}$ = 27°C (b) $V_{DC,link}$ = 1000 V, V_{GS} = 50 V/-7 V, $T_{initial}$ = 27°C (c) $V_{DC,link}$ = 1000 V, V_{GS} = 43 V/0 V, $T_{initial}$ = 150°C

Fig. 9. Post-failure chip surface of the failed devices under overcurrent turn-off condition for (a) M1 (b) M2 (c) M3.

Fig. 9 shows the post-failure chip surface of the different manufacturer devices after decapsulating the TO packages. M1 and M3 devices do not directly show any failure region on the chip surface or even on the gate runner. However, the M2 device shows the failure spot on the gate runner for all the measured conditions.

Electro-Thermal Simulation Results

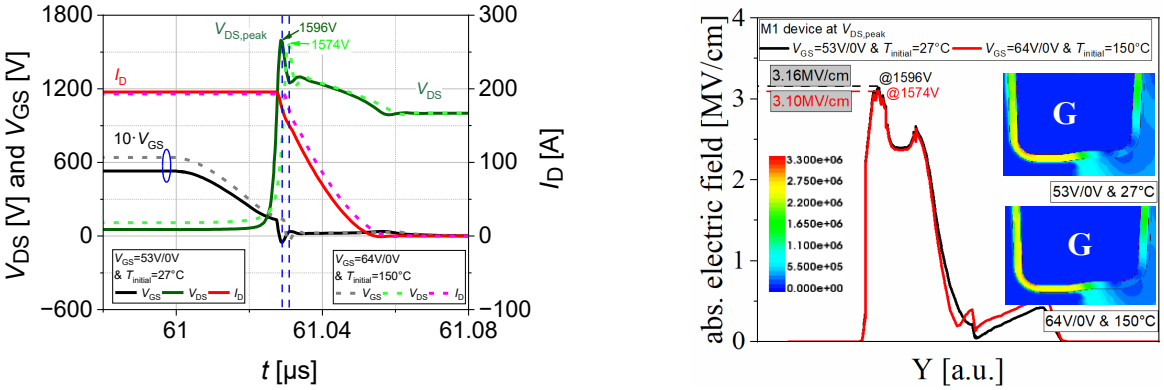
In this section, electro-thermal simulations were performed to understand the gate failure mechanism under overcurrent turn-off conditions with different gate biases for three different cell technologies using *Synopsys TCAD [6]*. For this, self-built 1200 V half-cell trench-gate, double-trench-gate and planar-gate structures were designed corresponding to the real structure and calibrated, see also Fig. 1.



(a) $V_{GS,on}$ = 53 V, $V_{DC,link}$ = 1000 V, I_D = 200 A (b) Electric field at $V_{DS,peak}$

Fig. 10. (a) Simulated overcurrent turn-off for M1 devices for two different $V_{GS,off}$ values at 27°C (b) electric field distribution in the bottom gate oxide at time point of $V_{DS,peak}$. Simulation conditions: L_{load} = 300 µH, R_G = 2 Ω, L_{par} = 30 nH. Inset: simulated electric field in the gate oxide.

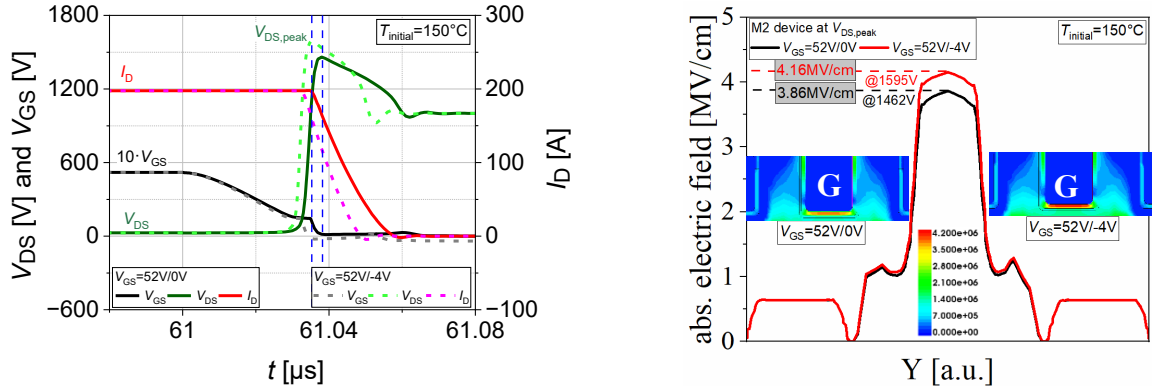
The overcurrent turn-off capability of the M1 device was approximately the same irrespective of the applied $V_{GS,off}$ values for 800 V and 1000 V at both temperatures. To verify this, overcurrent turn-off simulations were performed and compared at $V_{GS,off}$ values of 0 V and -7 V with $V_{GS,on}$ of 53 V and 27°C, as shown in Fig. 10(a). The simulation shows a faster di_D/dt and correspondingly higher $V_{DS,peak}$ for lower $V_{GS,off}$ value similar to the measurements. Fig. 10(b) displays the plotted electric field distribution at the bottom gate oxide for two different $V_{GS,off}$ values at their corresponding $V_{DS,peak}$. The high electric field at the pn-junction during overcurrent turn-off at $V_{DS,peak}$ and the V_{GS} driven gate oxide field sum up to an effective high electric field, eventually triggering pre-damage to the gate oxide of the devices which fits to increased I_{GSS} at turn-off currents. The influence of the negative $V_{GS,off}$ shows a small increase in the corner and bottom gate oxide electric field even though the overvoltage at turn-off increases strongly. This is due to the shielding by the deep p^+-doped regions below the gate, see Fig. 1(a).



(a) 53 V/0 V & 27°C and 64 V/0 V & 150°C (b) Electric field at $V_{DS,peak}$

Fig. 11. (a) Simulated overcurrent turn-off for M1 devices for different gate bias along with change in temperature (b) electric field distribution in the bottom gate oxide at time point of $V_{DS,peak}$. Simulation conditions: I_D = 200 A, $V_{DC,link}$ = 1000 V, L_{load} = 300 µH. Inset: simulated electric field in the gate oxide.

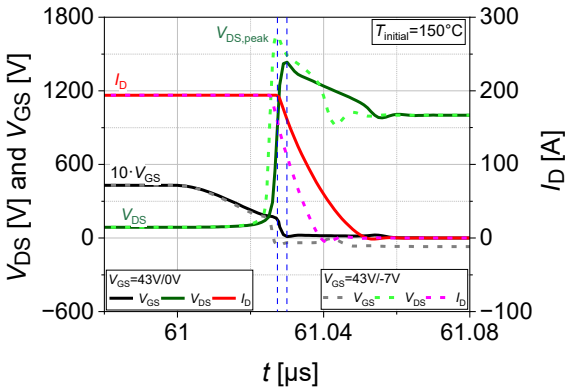
Fig. 11(a) shows the compared simulation results for 53 V/0 V at 27°C with 64 V/0 V at 150°C to understand the influence of the initial junction temperature on increased last-pass $V_{GS,on}$ or increased overcurrent turn-off robustness. The electric field in the gate bottom oxide at the corresponding $V_{DS,peak}$ was plotted in Fig. 11(b). As the initial temperature increased, the electric field in the bottom gate oxide decreased due to the reduced $V_{DS,peak}$ at higher temperatures even though $V_{GS,on}$ increased to 64 V, see Fig. 11(b). Also, the ionization coefficient decreases with higher temperatures hence, the critical electric field required for impact ionization increases with temperature.



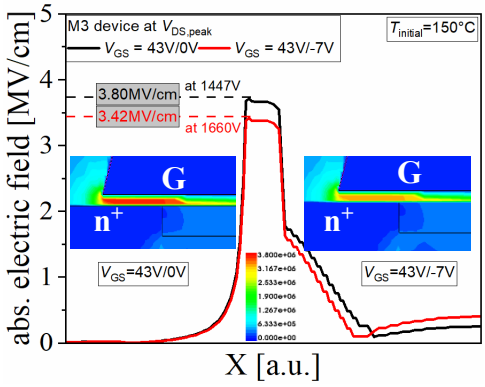
(a) $V_{GS,on}$ = 52 V, $V_{DC,link}$ = 1000 V, I_D = 200 A (b) Electric field at $V_{DS,peak}$

Fig. 12. (a) Simulated overcurrent turn-off for M2 devices for two different $V_{GS,off}$ values at 150°C (b) electric field distribution in the bottom gate oxide at time point of $V_{DS,peak}$. Simulation conditions: L_{load} = 300 µH, R_G = 2 Ω, L_{par} = 30 nH. Inset: simulated electric field in the gate oxide.

For M2 SiC MOSFETs, the simulations were performed to verify the reduced overcurrent turn-off robustness at lower $V_{GS,off}$ values. At 150°C and 1000 V, the measured overcurrent turn-off capability was reduced by 61 A for $V_{GS,off}$ values of -4 V compared to the 0 V case. Fig. 12(a) shows the simulated overcurrent turn-off results for M2 device with two different $V_{GS,off}$ values at 150°C and $V_{GS,on}$ of 52 V. The electric field distribution in the gate oxide at the bottom trench for $V_{GS,off}$ values of 0 V and -4 V is plotted in Fig. 12(b). The $V_{DS,peak}$ increases by 133 V and correspondingly, the electric field in the bottom gate oxide increases strongly and exceeds 4 MV/cm at $V_{GS,off}$ = -4 V. The gate oxide shielding seems not to be sufficient for M2 devices. Although the 4 MV/cm are still below the dielectric breakdown point the tendency in the simulation is shown, also compared to M1. Similar simulated results were found under unclamped inductive switching in [7].



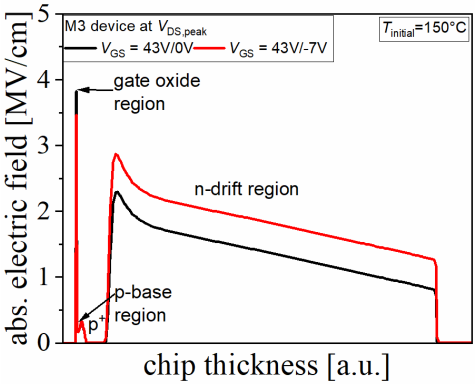
(a) $V_{GS,on}$ = 43 V, $V_{DC,link}$ = 1000 V, I_D = 200 A



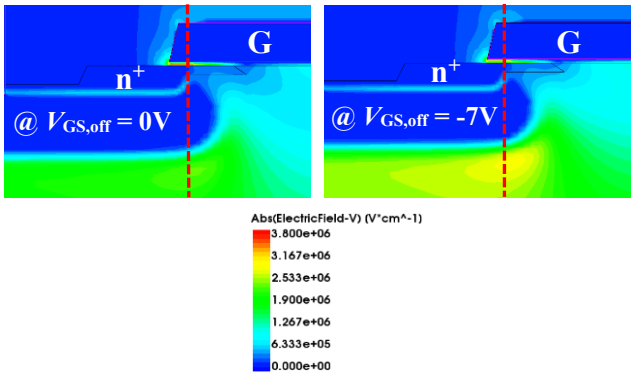
(b) Electric field at $V_{DS,peak}$

Fig. 13. (a) Simulated overcurrent turn-off for M3 devices for two different $V_{GS,off}$ values at 150°C (b) electric field distribution in the planar gate oxide at time point of $V_{DS,peak}$. Simulation conditions: L_{load} = 300 µH, R_G = 2 Ω, L_{par} = 30 nH. Inset: simulated electric field in the gate oxide.

The measured M3 results show increased overcurrent turn-off capability with lower $V_{GS,off}$ values, which is vice-versa to M2 devices. To understand this behaviour, overcurrent turn-off simulations were performed for two different $V_{GS,off}$ values at 150°C with $V_{GS,on}$ of 43 V, as shown in Fig. 13(a). The electric field distribution in the planar gate oxide at $V_{DS,peak}$ shows a higher magnitude of electric field at $V_{GS,off}$ of 0 V as compared to -7 V, as shown in Fig. 13(b). Even though, the $V_{DS,peak}$ increases strongly for negative $V_{GS,off}$ values, the gate oxide field is reduced as shown in the Fig. 14.



(a) Electric field across the chip at $V_{DS,peak}$



(b) Electric field distribution at $V_{DS,peak}$

Fig. 14. Simulated electric field distribution in the M3 devices with planar gate oxide at time point of $V_{DS,peak}$ from Fig. 13(a). Simulation conditions: $T_{initial}$ = 150°C, L_{load} = 300 µH, R_G = 2 Ω, L_{par} = 30 nH.

The simulations for different cell technologies have shown a high electric field in the gate-oxide region during turn-off. The simulated electric fields are in a range between 3.10 MV/cm to 4.16 MV/cm for the investigated cell technologies. This electric field magnitude along with possible defects in gate oxide and geometrical weak points (like corners etc.,) are a vulnerable point during turn-off. It has been noted that in reality, the electric fields in the gate oxide could be much higher since our simulation structures were just ideal as compared to the real structures. Furthermore, the overcurrent turn-off capability increase with increased $T_{initial}$ is due to reduced $V_{DS,peak}$.

Summary

The overcurrent turn-off capability of the SiC MOSFETs with distinct cell technologies from different manufacturers was studied in detail by measurements and supplemented with TCAD simulations. All the devices show different last-pass gate-source voltages due to their dissimilar gate oxide thickness, structure and shielding. The measured last-pass gate-source voltages are far beyond the safe operating area at DC-link voltages of 800 V and 1000 V. The measurements below 800 V do not show any failure for the measured conditions, the channel pinch-off is the limiting factor. The influence of the negative gate-source voltage strongly depends on the device design. As the initial temperature was increased, the last-pass $V_{GS,on}$ increases for all the manufacturers. Especially, the M1 devices show a significantly increased last-pass $V_{GS,on}$ at high temperatures. All the devices show an increased gate leakage current at last-pass $V_{GS,on}$. TCAD simulations have shown a stronger electric field in the gate oxide at $V_{DS,peak}$ during turn-off in the range of 3.10 MV/cm to 4.16 MV/cm depending on the cell technologies.

References

[1] T. Kimoto and J. A. Cooper, Fundamentals Silicon Carbide Technology: Growth, Characterization, Devices, Applications Singapore: Wiley, Nov. 2014.

[2] B. Findenig, et. al., “Robustness of SiC MOSFETs under Repetitive High Current Pulses” 19th ICSCRM conference, Davos, Switzerland, 2022, in Material Science Forum, Vol. 1092, pp. 119-125.

[3] D. Peters, et. al., “The new CoolSiC™ Trench MOSFET Technology for Low Gate Oxide Stress and High performance” in PCIM, Nuremberg, Germany, 2017, pp. 168-174.

[4] R. Boldyrjew-Mast, et. al., “Impact of Degradation Mechanisms in Gate Stress Tests on the Hard-Switching Behavior of 1.2 kV SiC Power MOSFETs” in 34th Proc. of ISPSD, Canada, 2022, pp. 229-232.

[5] J. W. McPherson, “Time dependent dielectric breakdown physics – Models revisited” in Microelectronics Reliability 52, 2012, pp. 1753-1760.

[6] *TCAD Sentaurus Manual,* Synopsys Inc., Mountain View, CA, USA,2022.

[7] K. Yao et. al., “Investigation of UIS Failure Mechanism in 1.2 kV Trench SiC MOSFETs using Electro-Thermal-Mechanical Stress Analysis” in 33rd Proc. of ISPSD, Nagoya, Japan, 2021, pp. 115-118.