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Dynamic Switching Energy Monitoring during Gate Switching Stress to Evaluate Performance Degradation in Hard Switching Electric Power Conversion Systems

Andrea Piccioni[1,a*], Maximilian W. Feil[1,b], Thomas Aichinger[1,c]

[1]Infineon Technologies Austria AG - Siemensstraße 2, 9500 Villach, Austria (AT)

[a]andrea.piccioni@infineon.com, [b]maximilian.feil@infineon.com, [c]thomas.aichinger@infineon.com

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Abstract. In addition to the well-known bias temperature instability (BTI) phenomena, recently, it has been revealed that SiC MOSFETs show another instability during high-frequency repetitive switching between $V_{GS(L)}$ and $V_{GS(H)}$, referred to as gate-switching instability (GSI). This study shows the increase in switching energy caused by gate-switching instability $V_{GS(th)}$ drift as key performance parameters in electric power conversion systems, especially, when operating in hard-switching mode. A new methodology based on double pulse test was applied at each readout. The results highlighted the significance of the degradation mechanism through its impact on hard-switching applications with high-switching frequency. Therefore ruggedness against GSI plays a pivotal role in the long-term re- liable operation of SiC MOSFET devices to ensure durable and efficient power conversion systems.

Introduction

The increasing adoption of SiC MOSFETs is attributed to their superior performance characteristics compared to conventional silicon-based power devices. The advantages of SiC MOSFETs are their ability to operate at elevated temperatures, lower switching losses due to their faster switching speeds, and higher critical electric field strength; resulting in improved efficiency and reduced energy losses. Consequently, SiC MOSFETs are well-suited for high-power applications such as electric vehicles, renewable energy systems, and industrial power supplies. However, since the early days of SiC MOSFET development, the SiC/SiO_2 interface has posed a challenge [1]. Significant advancements in reducing the defect density at the SiC/SiO_2 interface significantly boosted the commercialization of SiC MOSFETs, however, both research and academia are still striving to reduce it even further. The bias temperature instability (BTI) in MOSFETs has been a well-documented phenomenon for decades, previously observed in silicon p-MOSFETs [2][3]. Recently, a new degradation mechanism affecting the long-term reliability of SiC MOSFET devices, known as gate-switching instability (GSI), has been identified. This phenomenon superimposes BTI effects but is triggered only under repetitive gate-switching stress (GSS) between a negative ($V_{GS(L)}$) and a positive ($V_{GS(H)}$) gate bias. Since its discovery in 2018 by Infineon Technologies AG, GSI has been extensively studied [4][5][6] to understand its physical motivations and dependencies, leading to advanced modeling approaches [7]. In addition to Infineon Technologies AG, other semiconductor manufacturers [8] and research groups [9][10] have also contributed to improving the understanding of this phenomenon. Recently, it was discovered that V_{DS} bias in GSS can cause an additional impact on GSI [11]. As this is the latest discovery, the effect of V_{DS} is not included in this study. Additionally, [12] shows that the devices also used in this paper (from manufacturer M1) don´t show V_{DS} influence during GSS. While significant research has focused on electrical characteristics (parametric screening of $V_{GS(th)}$, $R_{DS(on)}$, $I_D(V_{GS})$, I_{GS}, $V_{GS(hyst)}$) over the time/cycle of stress, little attention has been given to the switching losses impact. The novel method proposed in Fig. 1a quantifies the application impact of the $V_{GS(th)}$ drift caused by

the GSI (with stress parameters as close as possible to real usage), by monitoring turn-on - E_{on} – and turn-off - E_{off} - energy at each readout. This approach is used to strengthen the understanding of this phenomenon in the application of power conversion systems.

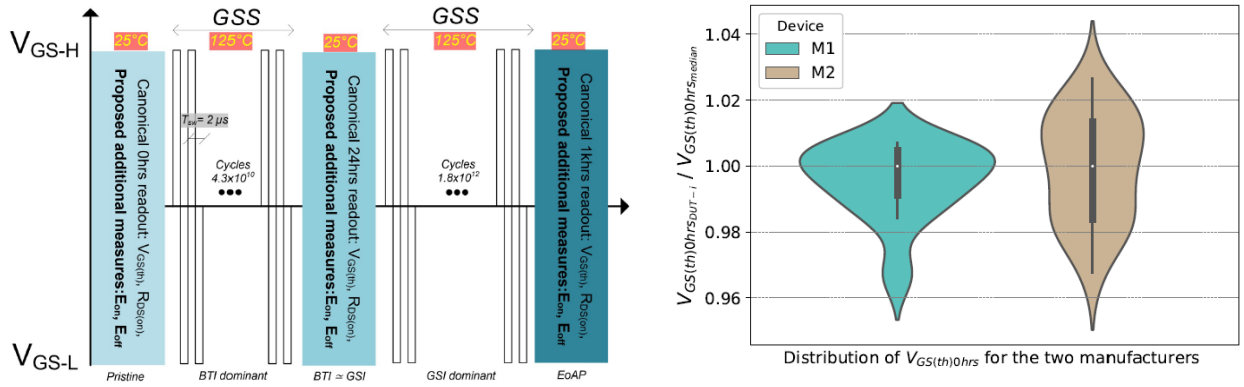

Fig. 1. (a) Proposed GSS methodology with electrical parameters readout and novel double pulse tests. (b) Violin plots with gate-source threshold voltage from the two manufacturers at their pristine state, calculated relative to their median.

Proposed GSS with Dynamic Switching Performance Monitoring

Method Description. To ensure a comparison of technologies and a sufficient statistical population, 23 SiC MOSFET devices in the TO-247-4 package from each of the two vendors are stressed and measured. Figure 1b shows their $V_{GS(th)_{0hrs}}$ distribution. The devices of manufacturer 1 (M1) were 2nd generation trench SiC MOSFETs, and the devices of manufacturer 2 (M2) were 3rd generation planar SiC MOSFETs. Although the devices from both M1 and M2 were in the 75 mΩ range, their gate charge (Q_g) differed significantly ($Q_{g_{M1}}$ = 21 nC and $Q_{g_{M2}}$ = 53 nC). Therefore, the gate resistance (R_g) was selected accordingly to ensure a fair comparison. Figure 1a illustrates the proposed application-oriented gate-switching stress (GSS) measurement procedure, which incorporates double pulse tests (DPTs) at each readout to simulate real-world operating conditions. In accordance with the JEP195 guideline [13], the key GSS parameters are defined in Table 1 with a focus on application-driven requirements. At each readout, the following stress levels were applied:

- 24 hours equivalent of $43.2x10^9$ cycles
- 1000 hours equivalent of $1.8x10^{12}$ cycles: Representative of the end point in time of a given application profile (EoAP)

Electrical parameters were monitored, and double pulse tests were performed at each readout. For completeness, the JEP195 guideline [13] encourages comparing at least exemplary switching behavior and switching losses before and after GSS. The boundary conditions for the double pulse test for the two manufacturers are listed in Table 1. The same 1200 V SiC Schottky Diode IDW40G120C5B was used as a high-side device in the double pulse test half-bridge leg.

Results: Electrical Parameters. Figure 2a illustrates the $V_{GS(th)}$ values of the devices under test (DUT) after 24 hours and 1000 hours of gate-switching stress (GSS), referenced to their pristine values. A notable difference in $V_{GS(th)}$ drift is observed between the devices from manufacturer 1 (M1) and manufacturer 2 (M2). Specifically, the median $V_{GS(th)_{M1}}$ drift after 24 hours was 3.82%, and 6.95% after 1000 hours, indicating a relatively stable threshold voltage. In contrast, the median $V_{GS(th)_{M2}}$ drift after 24 hours was 12.63%, and 22.76% after 1000 hours, suggesting a more pronounced degradation of the threshold voltage. The static performance of the devices, characterized by the on-state resistance ($R_{DS(on)}$), deteriorated proportionally to the $V_{GS(th)}$ drift due to the reduction in over-drive voltage, which is the difference between the gate-source voltage (V_{GS}) and the threshold voltage ($V_{GS(th)}$). Figure 2b shows that the median $R_{DS(on)_{M1}}$ drift was 0.62% after 24 hours and 0.89% after 1000 hours, indicating a relatively small increase in on-state resistance.

In contrast, the median $R_{DS(on)M2}$ drift was 1.21% after 24 hours and 2.48% after 1000 hours, suggesting a more significant degradation of the on- state resistance. These results suggest that the M1 devices demonstrated a higher ruggedness against electrical parameter drift caused by GSI, which is a critical aspect of device reliability.

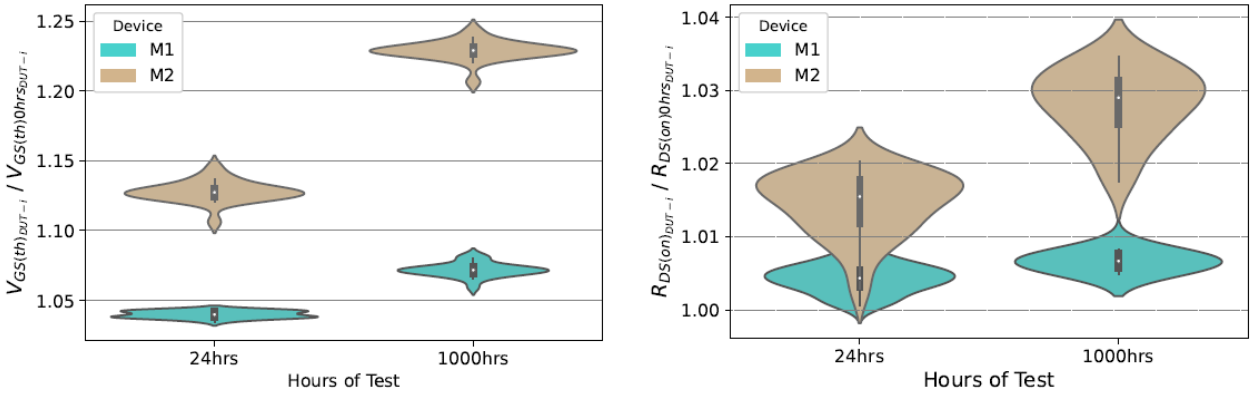

Fig. 2. Violin plots with electrical parameter readouts from the two manufacturers over the test hours, relative to the electrical parameter readouts at their pristine state (a) gate-source threshold voltage (b) drain-source on-state resistance.

Table 1. Application-relevant GSS and DPT parameters - * max values by datasheets.

	Gate-switching stress					**Double-pulse test**				
Param.	$V_{GS(H)}$*	$V_{GS(L)}$*	f_{sw}	T_{meas}	T_{stress}	V_{DC}	I_D	R_g	T_{vj}	V_{GS}
Unit	V	V	kHz	°C	°C	V	A	Ω	°C	V
M1	23	-7	500	25	125	800	9,20	33m 56, 100	25	-2, +18
M2	19	-8	500	25	125	800	9,20	15, 33, 56	25	-4, +15

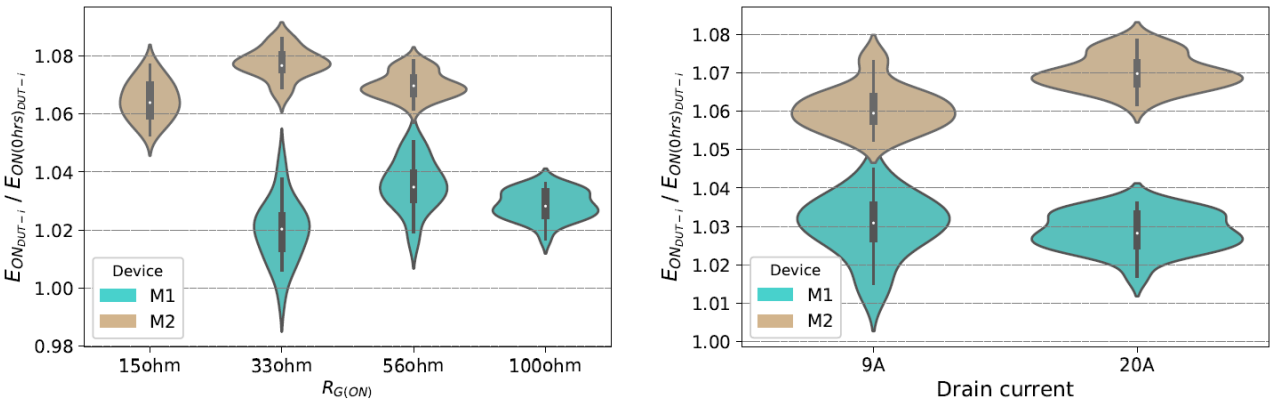

Fig. 3. Violin plots with double pulse test readouts from the two manufacturers at 1000 hours, relative to the double pulse test readouts at their pristine state (a) E_{on} at 20 A function of external gate resistance (b) E_{on} function of drain current with R_{gM1} = 100 Ω and R_{gM2} = 56 Ω.

Results: Dynamic Performance. The drift of electrical parameters, such as $V_{GS(th)}$ and the transfer characteristic, have a direct impact on the device performance during turn-on and turn-off events, which are respectively represented by E_{on} and E_{off}. While an increase in $V_{GS(th)}$ is beneficial for E_{off}, it has the opposite effect on E_{on}. However, E_{on} is typically 2.5- to 4 times higher in magnitude than E_{off}, which means that improvements in E_{off} have only a marginal impact on the total losses in the hard-switching applications. Therefore, it is essential to focus on the turn-on event, which dominates the total losses. Figure 3a illustrates the $E_{on_{20A}} = f(R_g)$ values after 1000 hours of GSS, referenced to their pristine values. The results indicate a minor decrease in the performance of the devices from manufacturer 1 (M1), which is consistent with the lower $V_{GS(th)}$ drift. Specifically,

the increment in median $E_{on_{M1}}$ with R_g= 56Ω was 2.84% after 1000 hours, suggesting a relatively small increase in turn-on energy losses. In contrast, the increase in median $E_{on_{M2}}$ with R_g=33 Ω was 7.69%, indicating a more significant degradation of its turn-on performance. Figure 3b shows the $E_{on} = f(I_{DS})$ values after 1000 hours of GSS, referenced to their pristine values. The impact of current density on devices from M2 is noteworthy, unlike the quasi-constant behavior of devices from M1. This suggests that the devices from M2 are more prone to aggravated degradation of their dynamic performance at higher current densities, which can become critical for their performance and reliability in applications with overload requirements.

Summary and Conclusion

In conclusion, the long-term reliability of SiC MOSFET devices is dependent on their ability to withstand GSI, which can significantly impact the performance and efficiency of power conversion systems. The proposed method with its application-driven approach provides a unique perspective on the consequences of GSI, highlighting its profound effects on the dynamic performance of SiC MOSFET devices. The results of this study are remarkable: after 1000 hours of GSI stress, devices from manufacturer 1 (M1) exhibited a median $V_{GS(th)}$ drift of approximately 7%, resulting in a moderate median increase of turn-on energy of only 2.83%. In contrast, devices from manufacturer 2 (M2) suffered from a median $V_{GS(th)}$ drift of approximately 22%, leading to a substantial median increase of turn-on energy of 7.69%, which can have significant implications for end-of-application profile operation. These findings clearly demonstrate that ruggedness against GSI should be of major priority when selecting SiC MOSFETs for a demanding application. This is important for designers and engineers to ensure the development of efficient and reliable power conversion systems that meet the stringent requirements of modern applications. Further research into the application impact of GSI is essential for the continued advancement of SiC-based power conversion. Having realized this, Infineon has been extensively studying [6][7] and improving this new phenomenon and has provided customers with clear mitigation strategies and application-tailored design guidelines [14] to ensure reliability over the lifetime.

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