

Prospects and Challenges for SiC Power Devices in MMC-VSC-HVDC Applications

Olayiwola Alatise^{1,a}, Saeed Jahdi^{2,b*}, Peter Gammon^{1,c},
Jose Ortiz-Gonzalez^{1,d}, Mana Hosseinzadeh^{2,e},
Konstantinos Floros^{3,f} and Ingo Lüdtkke^{3,g}

¹University of Warwick, Coventry, CV4 7AL, United Kingdom

²University of Bristol, Bristol, BS8 1UB, United Kingdom

³Compound Semiconductor Applications Catapult, Newport, NP10 8BE, United Kingdom

^aO.Alatise@warwick.ac.uk, ^bsaeed.jahdi@bristol.ac.uk, ^cP.M.Gammon@warwick.ac.uk,

^dJ.A.Ortiz-Gonzalez@warwick.ac.uk, ^em.hosseinzadeh@bristol.ac.uk,

^fkonstantinos.floros@csa.catapult.org.uk, ^gingo.ludtke@csa.catapult.org.uk

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Abstract. Voltage-Sourced Converters (VSC) that are used in High Voltage Direct Current (HVDC) systems are currently implemented in silicon Insulated Gate Bipolar Transistor (IGBT) technology. Advocates of Silicon Carbide (SiC) as a high voltage technology suggest that SiC has the potential to enhance the performance of these systems by improving the energy conversion efficiency. The preferred topology for the latest VSC-HVDC systems is modular multilevel converters (MMC), which are comprised of cascaded half-bridge or full-bridge sub-modules with voltages ranging between 1.3 kV and 2.8 kV. However, the ratings of current state of the art SiC power devices is not adequate. Furthermore, the low switching frequencies in Modular Multi-level Converter (MMC) topology of VSC-HVDC systems means that conduction losses dominate, hence, the fast-switching capability of SiC power devices is not necessarily an advantage. State of the art high voltage silicon devices exhibit comparable if not lower losses. This review evaluates the potential performance of SiC power devices in MMC-VSC-HVDC systems and reviews the challenges ahead for SiC devices.

Introduction

VSC-HVDC systems are now considered to be a critical component of future power system with more renewable energy generation, interconnection of asynchronous Alternate Current (AC) systems, developments of DC super-grids as well as the implementation of reactive power compensation technologies like Static Compensators (STATCOMs). Traditionally, HVDC was implemented as current source Line Commutated Converters (LCC) based on series connected thyristor valves. This choice of converter technology was predicated on the fact that phase-controlled thyristors did not have self-turn-off capability, hence, phase to phase commutation was initiated by voltage reversal of the AC system. This meant that the switching frequency of the converter was limited to the system frequency (50 Hz or 60 Hz), hence, the sizes of the filters for harmonic management could not be optimized. Although bulk power transfer was made possible, current source LCC converters exhibited numerous limitations including commutation failure in weak AC systems, inability to black-start and large filter sizes from low switching frequencies [1]. Hence, self-commutating VSC technology based on IGBTs arose as an alternative to LCC systems in applications such as offshore power transmission from wind farms where the physical size of the converter is limited by the size of off-shore platform.

Unlike the thyristor, which is a 4-layer latching device that conducts current through impact ionization induced avalanche multiplication, the IGBT conducts current through MOS-channels based on drift-diffusion mechanisms thereby making IGBTs more controllable with inherent self-turn-off capability. IGBT based self-commutating VSC technology is capable of 4-quadrant operation, can operate in weak AC systems, does not need reactive power compensation, can black-start and is not limited by the AC system frequency. However, VSC-HVDC, whether the earlier 2-level topology with series connected devices or the more recent modular multilevel converter

(MMC) topology with cascaded half-bridge (2 devices) or full H-bridges (4 devices), suffer from higher losses since IGBT modules and their package are not as well optimized as thyristors for high currents [2].

The limited performance of silicon IGBTs in VSC-HVDC systems is one of the motivations behind the development of SiC as a high voltage power device. SiC is a wide-bandgap power semiconductor material with a high critical electric field and low intrinsic carrier concentration, making it suitable for high-voltage blocking at high junction temperatures. Its high thermal conductivity also makes it efficient at dissipating power. Historically, SiC was first released as Schottky diodes, before power Metal-Oxide-Semiconductor Field-Effect-Transistors (MOSFETs) became commercially available, first at 1.2 kV and more recently at 1.7 kV. Manufacturers have demonstrated 3.3 kV [3], 6.5 kV [4] and 10 kV SiC MOSFETs together with 15 kV SiC IGBTs [5], however, as experimental prototypes with low current capability. Medium voltage grid converters such as Solid-State Transformers, Dual Active Bridge DC-DC Converters and STATCOMs based on 10 kV and 15 kV SiC devices are demonstrated.

SiC power MOSFETs and diodes are well-known for high-speed switching capability resulting from their unipolar characteristics since bipolar devices that use conductivity modulation suffer from tail currents in the case of IGBTs and reverse recovery in the case of PiN diodes and it exacerbates further with increased minority carrier lifetime. However, in MMC applications where maximum switching frequencies are 150 Hz thereabouts, the switching capabilities are not much of an advantage since conduction losses dominate. Furthermore, the temperature characteristics of silicon bipolar devices are better than those of SiC unipolar devices at high current ratings since minority carrier lifetime in bipolar devices increases with temperature thereby counteracting the resistive losses.

There are still significant challenges despite all the recent successes in SiC based power electronics. These challenges include, but are not limited to, gate oxide reliability, relatively low current handling capability, limited die size, high defect densities during crystal growth, low epitaxial growth rates and conduction losses that still are not as good as contemporary high voltage silicon bipolar technologies like IGBTs, Gate Turn-Off Thyristors (GTOs) and Integrated-Gate Commutated Thyristors (IGCTs). This paper balances the performance of current state of the art SiC power devices with the requirements of modern MMC-VSC-HVDC systems.

Device Technology Performance in VSC-HVDC

The first VSC-HVDC topology was a 2-level VSC comprising of series connected IGBT modules for voltage sharing in the off-state [6]. The high switching losses, electromagnetic stresses, lack of modularity and the design complexities regarding dynamic voltage balancing motivated academic and industrial research towards multi-level converter topologies including diode clamped, flying capacitor, cascaded H-bridges and MMC [7]. MMC topologies, where the AC sine waves are synthesized by discrete voltage levels from separate DC sources, have been the preferred option due to its modularity and fault tolerance. By using bypass thyristors and mechanical switches, defective voltage units can be shorted thereby making the converter significantly more fault tolerant than the preceding 2-level VSC or the multi-level NPC. MMC topologies can be Half-Bridge (HB), Full-Bridge (FB) or hybrids like the Alternate Arm Converter (AAC) [8] or the Series Bridge Converter (SBC) [9]. Although the FB and AAC offer fault blocking capability, the additional losses (due to higher device count in the current flow path) and additional control complexities means that the HB-MMC is the only variant that has been commercialized to date. A typical MMC-VSC comprises of 6 valves for the 3 phases with each phase comprised of the required number of series connected voltage units required to block the total DC voltage in the off-state. There is a fundamental trade-off between the number of units (which depends on the unit's voltage) and the complexity of the overall control system. A high number of levels implemented with lower voltage units will produce a smoother sinewave and reduce the voltage requirements of all unit components; however, with a more complex control system. A smaller number of levels implemented in higher voltage modules reduces the complexity of the control system however at the expense of producing a less smooth sinewave and needing high voltage rated voltage unit components including capacitors, busbars and ancillary

electronics. The number of levels can be at least 100 voltage units for eliminating the need to install output filters, however, even a converter with only 23 voltage steps can provide a harmonics output of 3%. On the contrary, today's VSC-HVDC converters have a significantly higher number of levels in the region of a few hundred. This is driven by the fact that the typical line-to-line voltage of ± 320 kV (so valve voltage of 640 kV) needs to be shared between voltage-sourced levels.

Using the half bridge MMC topology shown in Fig. 1 together with the system level parameters in table 1, the performance of commercially available 1.7 kV SiC MOSFETs (from Wolfspeed) together with high voltage IGBTs (1.7 kV, 4.5 kV and 6.5 kV) and IGCTs from Hitachi (then ABB) is analyzed. The converter is simulated under 6 different conditions as stated in table 2. Table 3 shows the power module technology simulated with the critical datasheet parameters used for the simulation.

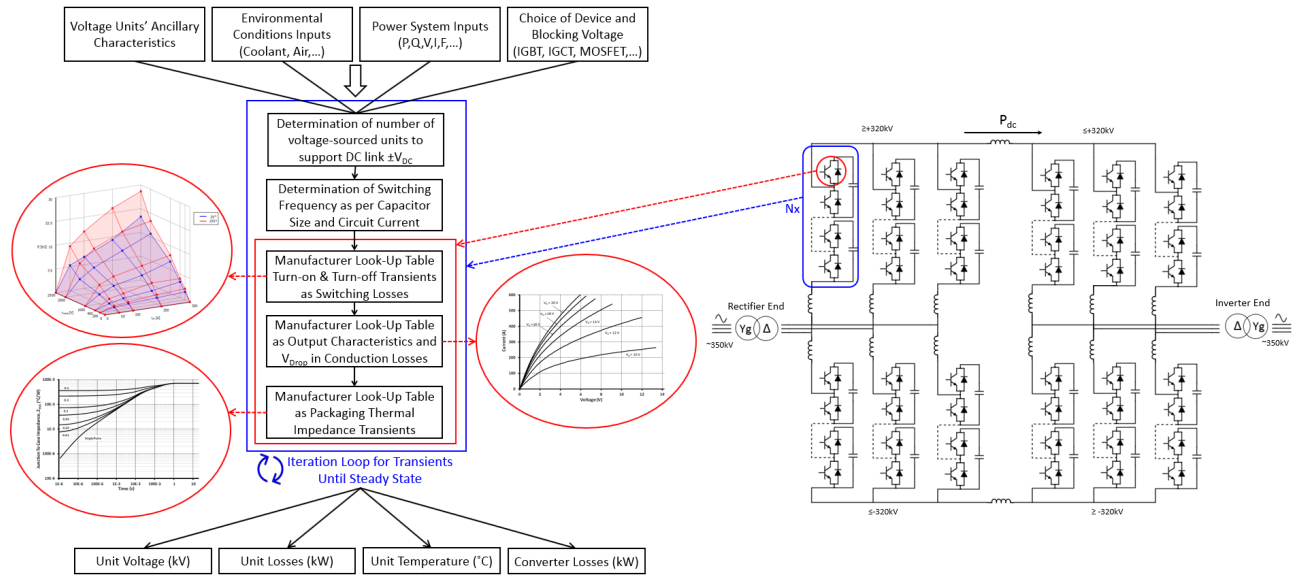


Fig. 1. The MMC-VSC-HVDC-HB converter topology used as the architecture to explore impact of SiC technology on HVDC power systems.

Table 1. System parameters for the MMC converter. **Table 2.** MMC converter operation modes.

Parameter	Value	Unit	Case	Operation Mode	Reactive Power
AC Voltage	350	kV	1	Rectifier	UPF
DC Voltage	± 320	kV	2	Inverter	UPF
DC Current	350	A	3	Rectifier	Capacitive
Active Power	225	MW	4	Inverter	Capacitive
Reactive Power	-200 - 200	MVar	5	Rectifier	Inductive
Frequency	50	Hz	6	Inverter	Inductive

Table 3. Device parameters used in MMC simulation.

Device	Make	Voltage (kV)	Current (A)	Switch Thermal Resistance ($^{\circ}\text{C}/\text{W}$)	Diode Thermal Resistance ($^{\circ}\text{C}/\text{W}$)	V_{CE} at 300 V & 125 $^{\circ}\text{C}$ (V)
SiC MOSFET	CREE	1.7	325	0.071	0.065	5.1
Silicon IGBT	ABB	1.7	800	0.021	0.036	1.7
Silicon IGBT	ABB	4.5	1200	0.009	0.019	1.8
Silicon IGBT	ABB	6.5	1000	0.009	0.017	2.5
Silicon IGCT	ABB	6.5	1290	0.008	0.017	1.8

The voltage rating of the individual units will ultimately determine the number of units needed to block a given DC voltage. Fig. 2 shows the number of voltage source units for the different power modules under analysis where the number of units needed increases as the voltage rating of each unit decreases. It should be noted that the module blocking voltages are considered to be de-rated by 70% i.e. it is assumed that the maximum blocking voltage imposed on the device is 70% of its rated breakdown voltage so the 1.7 kV module is operated at 1.2 kV, the 4.5 kV devices are operated at 3.2 kV and finally 6.5 kV devices are operated at 4.5 kV.

The converter losses are calculated solely according to the information extracted from the datasheets. The following steps are used in modelling the conversion losses of the converter [10]:

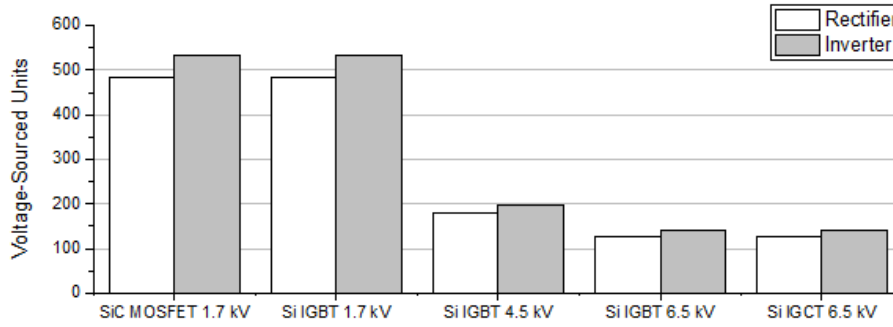


Fig. 2. The number of voltage units per converter's device technology. The devices with higher voltage ratings will support the line voltage with smaller number of units connected in series impacting the overall conduction and switching losses.

- i The operating mode of the converter determined by the control algorithm is used to determine the load current through the transistor and anti-parallel diode.
- ii The recommended gate drive voltage is used to determine the on-state voltage drop from the output characteristics
- iii The temperature and current-dependent conduction loss is calculated from look-up tables.
- iv The temperature and current-dependent switching loss is calculated from look-up tables.
- v The combined losses are input to the thermal model which is derived from the datasheet thermal impedance characteristics (the case temperature is fixed).
- vi The calculated junction temperature determines the new losses together with load current and switching state.

Fig. 3(a) shows a technology comparison of the unit losses, voltage of each units, number of voltage units, total converter losses and the junction temperature while the MMC is in inverter mode. Fig. 3(b) shows the same comparison while the converter is in rectifying mode. It can be seen from Fig. 3(a), that as far as the total converter losses are concerned, the 6.5 kV silicon IGCT is the most efficient technology whereas the 1.7 kV SiC MOSFET is the least efficient. Fig. 4 shows the simulated maximum junction temperature of the devices in the power module during (a) capacitive mode and (b) inductive mode of operation. During inverting operation, the junction temperature refers to the transistor and in rectification mode, the junction temperature refers to the diodes. Looking at the junction temperatures, the SiC MOSFET module exhibits the highest junction temperatures. This is due to the fact that SiC power devices typically have higher junction-to-case thermal resistances compared to comparatively rated silicon IGBTs as can be seen in table 3. This is because SiC chips have considerably smaller active areas compared to comparatively rated silicon IGBT chips. Early generation SiC chips had thicker substrates (for ease of mechanical handling), despite having thinner drift layer thicknesses that result in low conduction losses. The new generations, though, use advanced substrate thinning techniques that improve thermal impedance between junction and case.

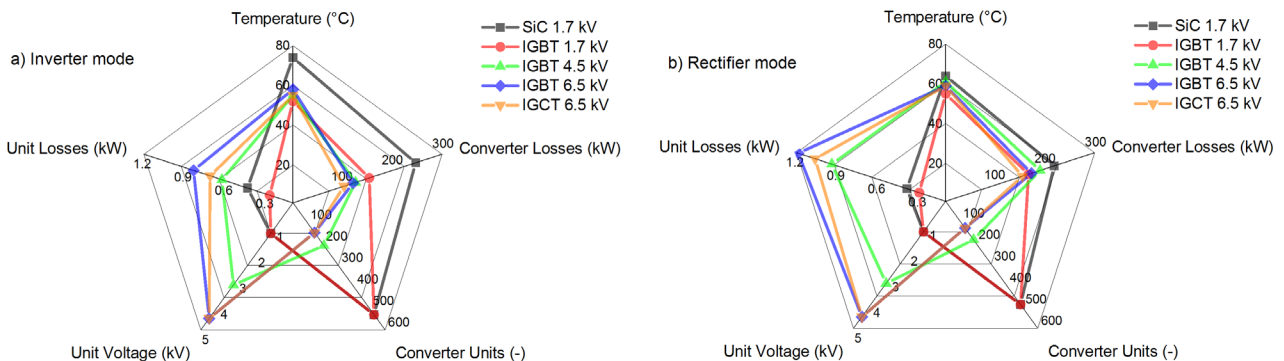


Fig. 3. Comparison of the main converter parameters for different power module technologies for the (a) Inverter, and (b) Rectifier modes.

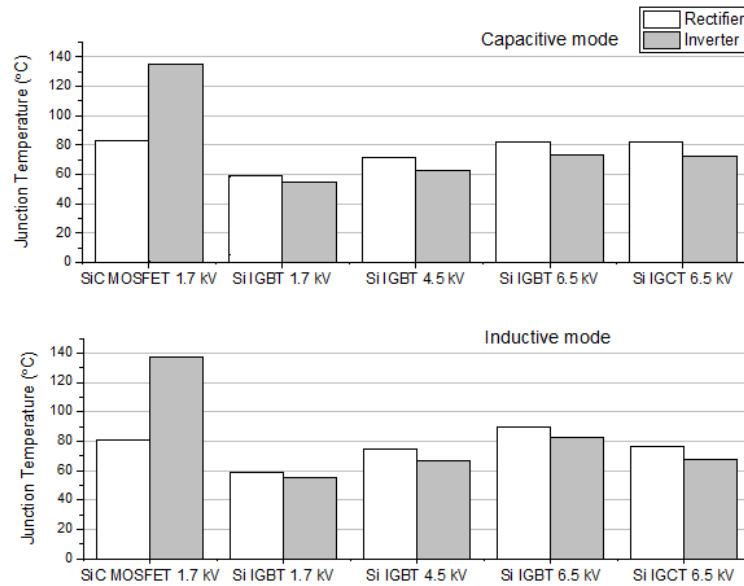


Fig. 4. Junction temperature of power devices in capacitive and inductive modes of operation.

Fig. 5 shows the total voltage unit and converter losses for the different device technologies in the MMC in inverter and rectifier operation for both inductive and capacitive modes of operation. In this figure, the 1.7 kV silicon IGBT has the lowest losses followed by the 1.7 kV SiC MOSFET module. This is expected since they are the lowest voltage rated devices, hence, will have the lowest conduction losses. The 1.7 kV silicon IGBT module exhibits half the losses of the 1.7 kV SiC MOSFET module. When looking at the total simulated converter losses, the silicon bipolar (IGBTs and IGCT) based converters have lower losses than the 1.7 kV SiC MOSFET based converter. The high losses of the SiC MOSFET converter compared to IGBTs and thyristors is due to the fact that the MOSFET is unipolar while the IGBT and IGCT are bipolar. Bipolar devices use conductivity modulation from minority carrier injection to ensure low conduction losses while MOSFETs rely only on the drift of majority carriers. As far as conduction losses are concerned, high voltage SiC MOSFETs are not as efficient as silicon IGBTs and this difference becomes magnified as the voltage level of devices increase. This is one of the key motivations behind research into SiC IGBTs.

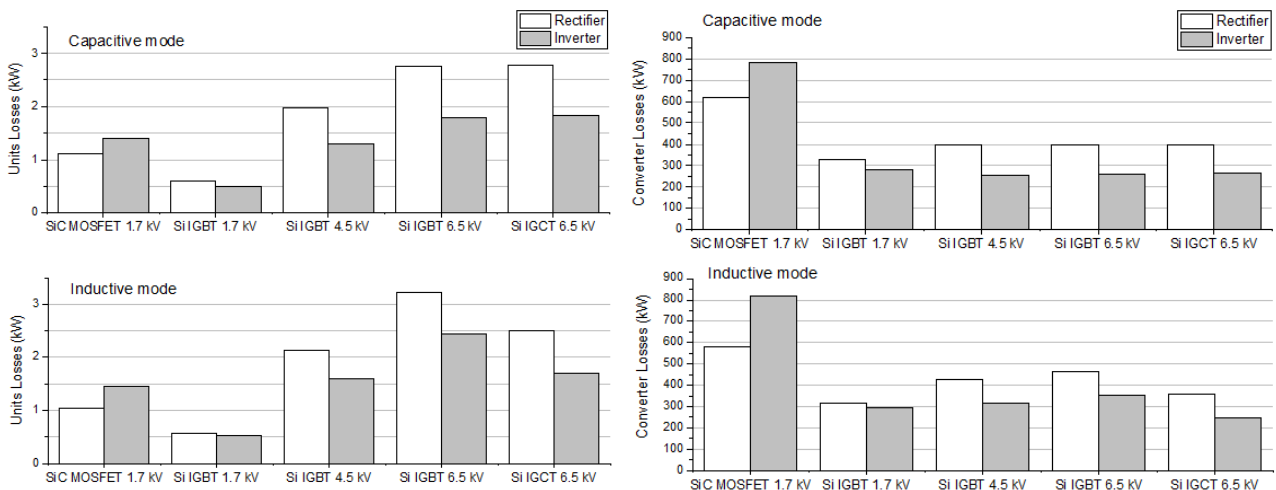


Fig. 5. The simulated voltage units losses, and converter losses, for different devices in the MMC.

Challenges for SiC Implementation

Gate Driving Issues in SiC. Fast switching rates in SiC power MOSFETs result in low switching losses. Being unipolar, these losses are determined by the charging and discharging of parasitic capacitances. In high power bipolar devices like IGBTs and thyristors, the switching rate is not only determined by capacitance discharge but also by the extraction and recombination of minority carriers

in voltage blocking drift layers. This results in tail currents for IGBTs and reverse recovery for PiN diodes. The high dV/dt and dI/dt enabled by SiC causes problems in the presence of parasitic capacitances and inductances [11]. Due to the much higher voltage and current commutation rates inherent in SiC MOSFET switching, electromagnetic oscillations (ringing) is a well-known problem that results from resonating LC components. Higher switching dI/dt generates more voltage oscillations. Likewise, higher dV/dt will generate more current oscillations.

Other problems that result from high voltage/current commutation rates include Miller-capacitance feedback effects (between transistors in the same phase leg) leading to short circuits across the DC link of the converter [12]. This is sometimes referred to ‘parasitic gate turn-on’ or ‘cross-talk’. High dV/dt across the SiC MOSFET coupled with the Miller capacitance induces a parasitic current and flows through the gate resistance and results in a parasitic gate voltage. If this unintentional gate voltage exceeds the threshold voltage, then the device turns-on thereby causing a temporary short circuit. This problem is solved in IGBTs by turning off with negative gate voltages thereby increasing the offset between the off-state and threshold voltage. This approach works in SiC as well, however, this can have reliability implications since the gate oxide is not as reliable as in silicon. Slowing down the device can mitigate cross-talk; however, this will be at the expense of increased switching losses.

Gate Dielectric Reliability. Gate dielectrics in silicon MOSFETs and IGBTs are formed simply by the thermal oxidation of silicon. Interface and fixed oxide traps result from imperfections in the silicon/SiO₂ interface. Over the decades, these traps have been well managed by improved process recipes in silicon, however, academic and industrial publications [13] show that the SiC/SiO₂ interface is more challenging. This is due to excess carbon atoms, originating from the SiC, which get trapped at the oxide interface during gate formation via thermal oxidation [14]. There has been significant research into the development of reliable oxide interfaces for SiC MOSFETs [15]. Threshold voltage shift and bias temperature instability (BTI) are well-known reliability problems in SiC that are due to increased interface and fixed oxide traps [13]. BTI results from electron capture from the channel into the gate dielectric when the device is in inversion (device is on and V_{GS} is high) and hole capture from the channel when the device is in accumulation (device is off and V_{GS} is negative). The result is a downward threshold voltage drift for negative BTI (NBTI) and an upward threshold voltage drift for positive BTI (PBTI). PBTI can cause a marginal increase in on-state resistance, however, NBTI can cause destructive failure through current crowding in high current modules where parallel devices are required to share current and gate synchronization is lost due to unequal NBTI shifts between parallel devices [13]. Typically, the IGBT characteristics for the unstressed device and the stressed device overlap, meaning there is virtually no V_{TH} shift. This is not the case with SiC as there is a shift in the transfer characteristics for PBTI and NBTI.

The previous section on gate driving issues in SiC highlighted the need to turn-off SiC power MOSFETs with negative voltages to avoid cross-talk between devices in the same phase leg. The improved gate dielectric properties in silicon devices means high off-state negative gate voltages can be used to suppress the effect completely. However, in SiC there are limitations to how high the off-state negative gate voltage can be and there are long term reliability implications for the continued use of negative voltages due to NBTI. For this reason, negative turn-off voltages for SiC MOSFETs are lower compared with Silicon devices.

Thermo-Mechanical Reliability of SiC Devices. In applications with high failure costs, like HVDC, the reliability of the packaging system is paramount for increasing the speed of adoption of SiC power modules. The traditional Direct-Bond Copper (DBC) based packaging technology was developed for silicon devices hence the different thermomechanical properties of the silicon chip have an impact on the stresses on the packaging elements and its reliability. The stiffness of the SiC chip, a result of its Young’s Modulus being three times higher compared with a silicon chip, causes higher thermomechanical stresses in the solder due to Coefficient of Thermal Expansion (CTE) mismatch, hence the fatigue increases and its lifetime reduces [16]. The physical size of SiC chips, which are smaller in area and thicker than Silicon IGBT chips, also contribute to higher stresses on the solder [17]. All these factors initially contribute to a reduced power cycling capability of modules

using SiC chips [16], hence the development of packaging more suitable for SiC chips is necessary. Research studies [18] have shown alternative packaging alternative for SiC chips, with improved interconnects, metallization, solders, ceramic substrates and assemblies are proposed and evaluated. There are studies already presenting an improved power cycling capability of SiC modules: using sintered silver die attach [19] and sintered copper [20]. A packaging alternative which has demonstrated a superior power cycling capability and reliability is pressure packaging (press-pack or pressure contacts), where the solder and wirebonds are removed and the semiconductor chip is sandwiched between two copper poles using two intermediate contacts for CTE matching [21]. This packaging system ensures failure into a stable short-circuit [22], which is a requirement for topologies with series connected devices, as used in alternate arm converter MMC topologies. Some initial studies of SiC using pressure contacts have been presented, for example [23], and a higher power cycling capability has been reported [24], together with stable short-circuit capability. However, as the chip size is smaller compared with silicon, the development of a high current press-pack module will be challenging as it involves the parallel connection [25] of multiple chips [26].

Prospect of SiC in HVDC

The results of the current study indicate that the application of currently available SiC transistor technology is not yet fully practical in HVDC converters [27]. However, the properties of SiC devices are rapidly improving and there could be a room in the future for these devices in HVDC converters. This holds as SiC technology was initially developed for medium voltages and high frequency applications and reduction of on-state resistances and switching speeds were main design targets. In HVDC switching speed is not that important so a targeted designed device for this application could change the current landscape. For this to be realized, SiC MOSFETs with very low on-state resistances and acceptable price are required to outperform IGBTs. The voltage rating of devices should increase to 4.5 kV with larger chips which should increase the current rating of devices to at least 500 A for viable paralleling solutions. Larger chip size would improve the thermal resistance characteristics, so the excessive junction temperatures seen in current SiC device would no longer exist. SiC devices show strong avalanche ruggedness compared with silicon device and this could be useful in heavy-duty applications. The breakthrough would of course be significant reduction in price coupled with complete elimination of the gate oxide failure mode in fabrication and increase in rating.

Summary

This paper has reviewed the feasibility of SiC power MOSFETs for VSC-HVDC applications at the time of writing. MMC simulations have been used to compare the performances of 1.7 kV SiC MOSFET modules with 1.7 kV Silicon IGBT modules as well as higher voltage rated IGBT and IGCT modules. The results show that overall converter losses are highest with the SiC MOSFET modules because the conduction losses are still higher compared to silicon IGBT and IGCT modules. The number of voltage sourced units required for a given DC voltage is higher because of the reduced breakdown voltage available in SiC MOSFETs compared to silicon IGBT technology where 4.5 kV and 6.5 kV voltage blocking capability is available. SiC IGBTs appear to be the ideal candidate for VSC-HVDC systems since SiC MOSFET technology exhibits unacceptable conduction losses. There are still major technological challenges regarding the fabrication of high voltage and high current SiC modules suitable for HVDC systems. Until then, silicon bipolar technology will continue to dominate.

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