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Dynamic Characterization and Robustness of SiC MOSFETs Based on SmartSiC™ Engineered Substrates

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Abstract. The improvement of the electrical properties of power semiconductors using engineered substrates is becoming increasingly significant. This paper investigates the dynamic performance and robustness of SiC MOSFETs based on SmartSiC™ engineered substrates, focusing on the reverse recovery of the body diode and their ruggedness under overload conditions such as short-circuit and surge current. A comparison with SiC MOSFETs based on conventional monocrystalline substrates was performed to evaluate the results. A significant decrease in reverse recovery charge was observed, particularly at higher temperatures, while the robustness during short-circuit type I and surge current was not affected.

Introduction

Power semiconductor devices based on silicon carbide (SiC) are increasingly being adopted, particularly in the automotive industry. To meet the constantly growing demand, the availability of high-quality 4H-SiC base material is crucial. Moreover, there is a need to further optimize factors such as cost and wafer yield. SmartCut™ technology addresses this by combining a thin (350-800 nm) high-quality monocrystalline SiC layer with a thick (350 µm) low-resistivity polycrystalline SiC carrier wafer through wafer bonding and wafer cut by hydrogen implantation [1, 2]. This results in an engineered SmartSiC™ substrate with a low resistivity (< 5 mΩ·cm), significantly lower than that of commercial monocrystalline 4H-SiC material (20 mΩ·cm). Furthermore, the ability to reuse the monocrystalline donor wafer multiple times after the splitting process improves the utilization efficiency of the SiC starting wafer.

The reliability of power devices using the SmartSiC™ engineered substrates, particularly in terms of power cycling capability, has been explored in several publications [2, 3]. However, assessing dynamic performance, such as the reverse recovery process, and ensuring robustness under overload conditions is also crucial. The electrical and thermal properties of the SmartSiC™ engineered substrate can impact the power device's performance in these scenarios. Therefore, this paper examines the extent to which the dynamic performance and the overload robustness are influenced.

Methodology and Devices Under Test

To evaluate the performance of a power device based on a SiC engineered substrate, it is crucial to compare it with a device based on a conventional pure monocrystalline substrate as reference. For this purpose, SiC MOSFETs of the 1200 V voltage class with a trench structure were fabricated using both SiC engineered and conventional monocrystalline substrates. By processing

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these two types of SiC MOSFETs under similar conditions, their performance can be directly compared, enabling an evaluation of the SiC engineered substrate's impact. The cell design, the n⁻- base region and the buffer layer are identical for both devices types. Furthermore, the assembly and interconnection technology (AIT), based on a die top system (DTS), is the same for both types of SiC MOSFETs. However, it is important to note that the MOSFET based on a SiC engineered substrate is 30% thicker than the reference SiC MOSFET. The schematic cross section of both devices is depicted in Fig. 1.

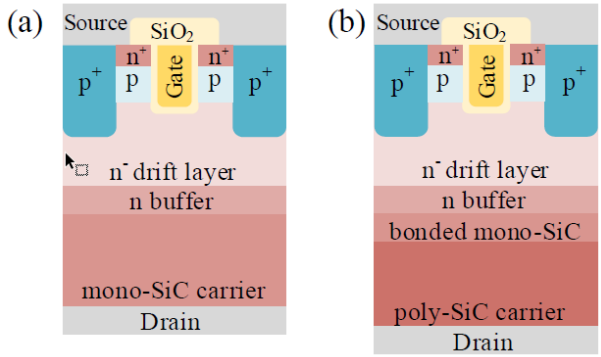


Fig. 1. Schematic cross section of (a) reference and (b) SiC engineered substrate based MOSFET.

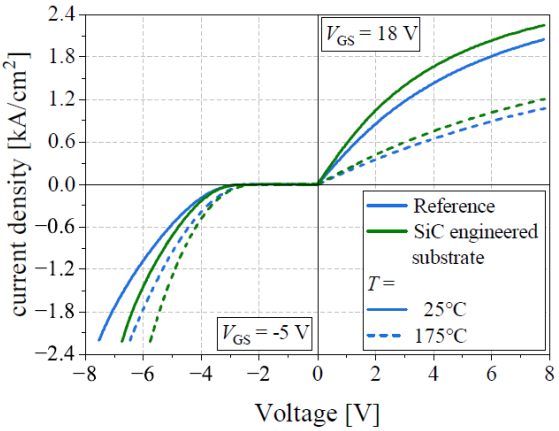


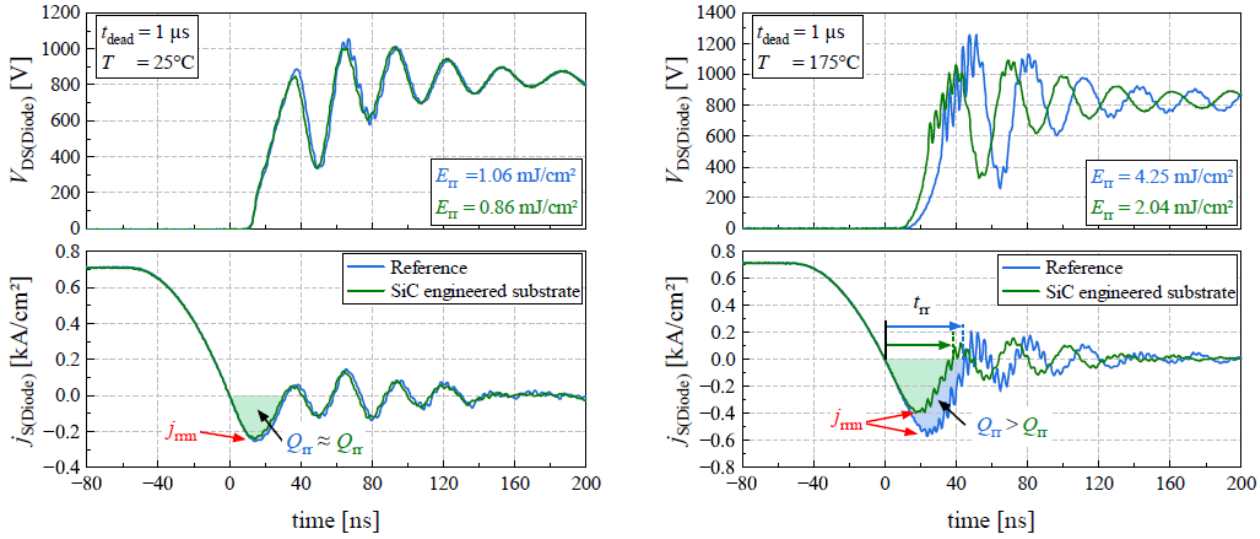
Fig. 2. Comparison of IV-characteristic for different T.

The substrate resistance in a MOSFET based on a SiC engineered substrate can be divided into three individual components: the resistance of the thin monocrystalline layer, the resistance at the bonding interface, and the resistance of the polycrystalline layer. The resistivity of the bonding interface is extremely low, typically ranging from 3 to 10 μΩ·cm² [4]. In total, these resistances are up to 35% lower than that of a conventional substrate [1]. Given that the resistance of the n-channel/JFET-region is the dominant component in a 1200 V SiC MOSFET, the overall reduction in total resistance ($R_{DS,on}$) for the MOSFET based on a SiC engineered substrate will be less pronounced. Fig. 2 shows a comparison of the IV-characteristic for both SiC MOSFETs. A reduction in the voltage drop and consequently the resistance can be observed in both quadrants at both measured temperatures (T) for the MOSFET based on the SiC engineered substrate. However, to obtain a qualitative assessment of the resistance reduction, the resistance of 35 devices was measured for each of the two device technologies. A trend toward lower $R_{DS(on),sp}$ is observed for the MOSFET based on a SiC engineered substrate, with an average reduction of 13% compared to the reference.

Measurement Results and Discussion

Reverse Recovery Behavior. Initially, the reverse recovery behavior was measured during the turn-off process of the body diode. A measurement setup and methodology described in [5] was used to perform this investigation. The high-side and low-side MOSFET are the same type of MOSFET. The DC-Link voltage was set to 850 V for all measurements. To ensure an equitable comparison of the reverse recovery at similar switching speeds, identical gate resistances $R_{G(on)}$ and $R_{G(off)}$ values were chosen for both device technologies. Fig. 3 compares the reverse recovery behavior of the reference and SiC engineered substrate based device at different temperatures.

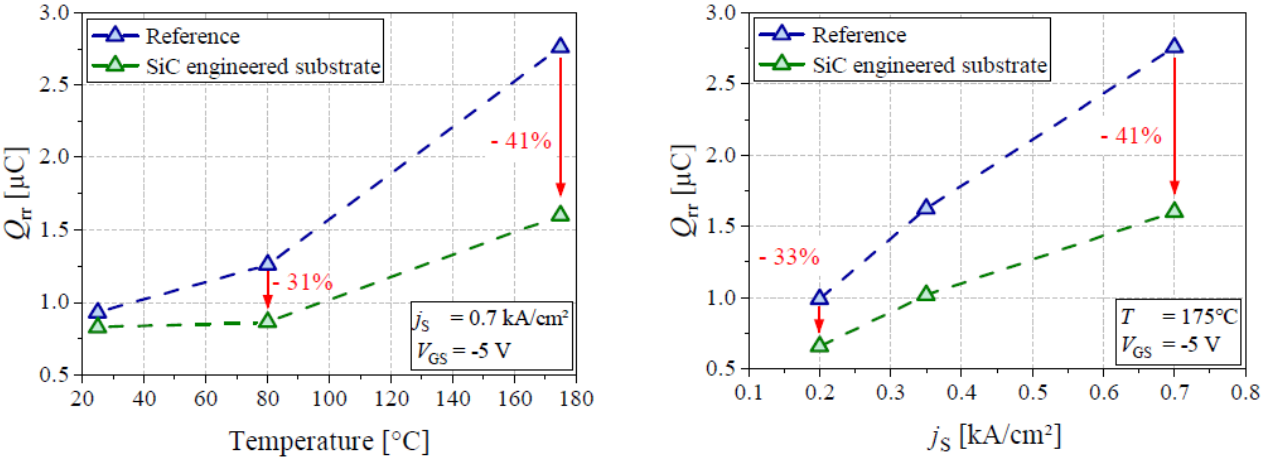
At T = 25°C, no significant difference can be observed between voltage (V_{DS}) and current density (js) for both technologies. A typical, almost capacitive-only switching behavior is observed. However, at T = 175°C, the device based on the SiC engineered substrate shows a lower reverse recovery current peak density (j_{rrm}) and time (t_{rr}). Consequently, the losses during reverse recovery (E_{rr}) are reduced.



(a) $T = 25°C$ (b) $T = 175°C$

Fig. 3. Comparison of the measured reverse recovery behavior for different T at $V_{DS} = 850$ V, $V_{GS(Diode)} = -5$ V, $t_{dead} = 1$ µs and $j_S = 0.7$ kA/cm².

The reverse recovery charge (Q_{rr}) is comprised of a capacitive stored charge (Q_C) and a stored charge from charge carriers (Q_{Plasma}) [6]. Fig. 4a illustrates the temperature dependency of Q_{rr}, revealing that both substrate technologies show an increase in Q_{rr} at higher T. This increase is attributed to a higher ionization degree of the p-doped region and a higher carrier lifetime at elevated temperatures, leading to a more pronounced influence of Q_{Plasma}. Additionally, the difference in Q_{rr} between the reference and the SiC engineered substrate based device increases with elevated T. At 175°C, the Q_{rr} of the device based on a SiC engineered substrate is reduced by 41% compared to the reference device. Further measurements were conducted at elevated temperatures and various current densities. A higher current density results in a higher Q_{rr}, as the increased current density enhances plasma in the drift region (see Fig. 4b). Thus, the Q_{Plasma} contribution to Q_{rr} increases. The reduced Q_{rr} of the device based on a SiC engineered substrate is also noticeable under different current densities, with the reduction becoming more significant as the current density increases.

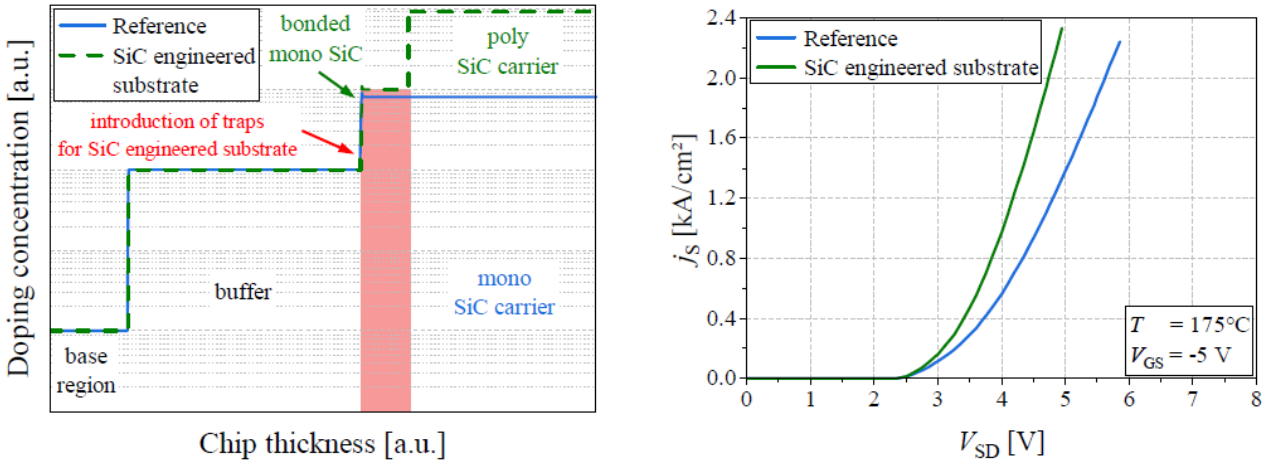


(a) Q_{rr} at different T (b) Q_{rr} at different j_S

Fig. 4. Reverse recovery charge for different temperatures and current densities at $V_{DS} = 850$ V, $t_{dead} = 1$ µs and $V_{GS(Diode)} = -5$ V.

The device based on a SiC engineered substrate shows a reduced voltage drop in the 3rd quadrant and a lower Q_{rr}, which initially appears contradictory. Therefore, a more detailed understanding of plasma behavior during reverse recovery is necessary to explain these findings from the measurements for both technologies. To investigate this, electro-thermal simulations were

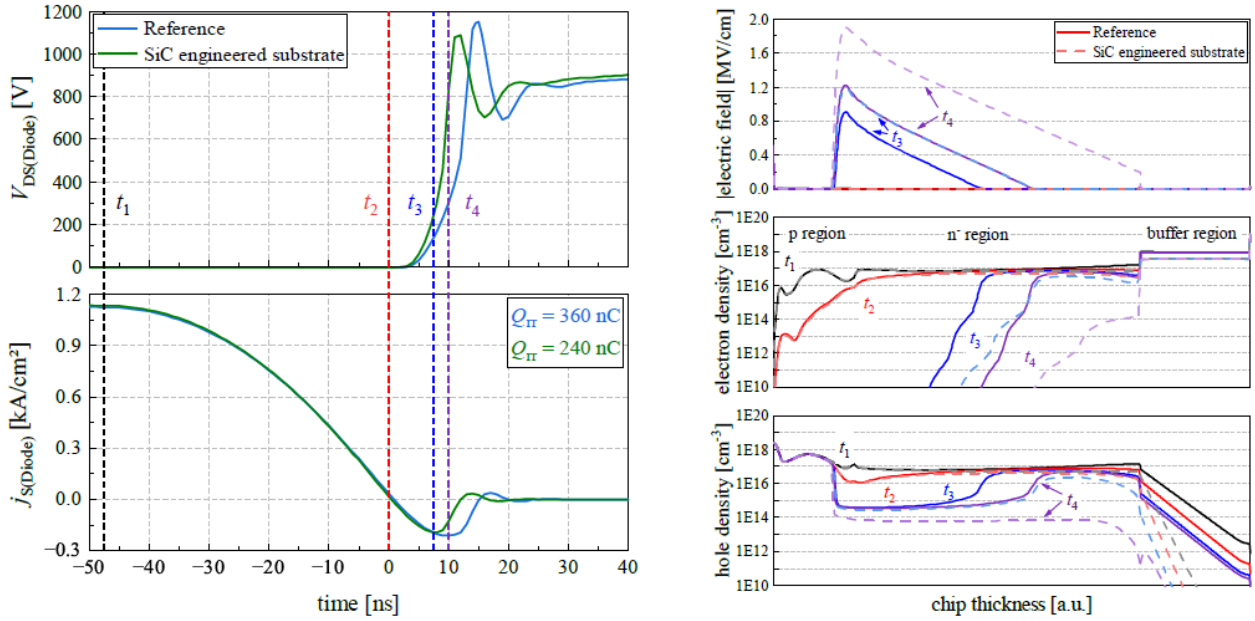
carried out on a self-designed 1200 V half-cell SiC MOSFET with a trench-cell structure using Synopsys TCAD [7]. Furthermore, the devices' substrate compositions were considered, as shown in Fig. 1. For the device based on a SiC engineered substrate, the doping concentration on the drain-side was adjusted (see Fig. 5a). The poly-SiC material has a higher doping concentration compared to mono-SiC, resulting in higher electrical conductivity [4]. Additionally, a hypothesis was made that the bonded mono-SiC contains a higher density of trap levels due to hydrogen implantation [8]. The IV-characteristic curve in the 3rd quadrant for both structures, simulated at an temperature of 175°C, is illustrated in Fig. 5b. The body diode of the device based on a SiC engineered substrate shows a lower voltage drop as compared to the reference device, similar to the measured IV-characteristic (see Fig. 2).



(a) doping concentration at the drain-side (b) simulated IV-characteristic in 3rd quadrant

Fig. 5. Doping concentration and simulated IV-characteristic in 3rd quadrant for both device technologies.

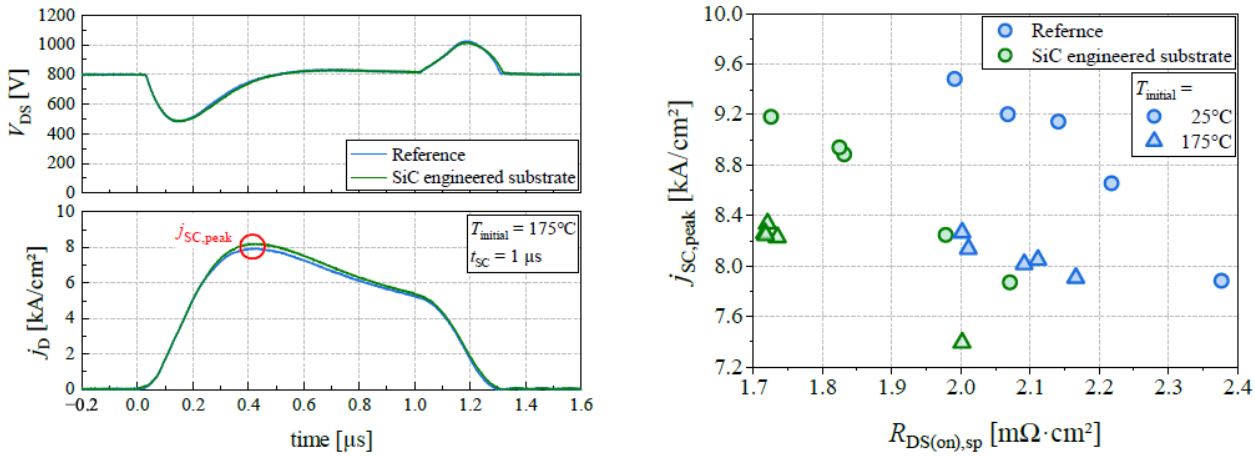
A time-dependent electro-thermal reverse recovery behavior was simulated at a DC-link voltage of 850 V, and T of 175°C for both structures. The simulated reverse recovery behavior for reference and SiC engineered substrate based MOSFET is shown in Fig. 6a. The t_{rr} and j_{rrm} are lower for the SiC engineered substrate based device as compared to the reference device. Hence, the simulated results show 33% reduced Q_{rr}. To understand the plasma behavior during reverse recovery, four time points were considered (see Fig. 6a). The electric field, electron and hole density were plotted at the corresponding time points in Fig. 6b. At time point t_1, the body diode operates in conduction mode. For the device based on a SiC engineered substrate, a higher density of trap levels introduced by the bonded mono-SiC, results in a reduced electron injection from the drain-side. Consequently, the hole density is lowered at the interface between the n^--base and the buffer, along with the penetration depth into the buffer region. In total, this leads to a reduced back-side emitter efficiency and charge carrier lifetime. The time point t_2 was selected at the zero crossing of the current during the onset of the diode turn-off. For both t_1 and t_2, the electric field is negligible as the device is still in the conduction mode. Subsequently, the electron and hole densities near the p-region decrease for both structures as the current density reduces. However, at the n^--region/buffer interface, the hole density and penetration depth remain lower for the device based on a SiC engineered substrate. At time point t_3, the device based on a SiC engineered substrate reaches the reverse recovery current peak. Additionally, it shows a stronger electric field expansion with higher magnitude. At time point t_4, the plasma is removed for the device based on a SiC engineered substrate and the electric field spans the entire n^--region due to faster depletion of charge carriers. Further, the hole density is three orders of magnitude lower than in the reference device at the drain-side of the n^--region. The reduced hole density, as well as the corresponding electron density, results in a lower Q_{rr} and t_{rr} for the device based on a SiC engineered substrate, as observed in the measurements.



(a) reverse recovery behavior (b) electric field and charge carrier density

Fig. 6. Comparison of simulated reverse recovery behavior and electric field and charge carrier density at different time points at V_{DS} = 850 V and T = 175°C.

Short-Circuit Behavior. In this section, the short-circuit type I (SC I) robustness of SiC MOSFETs based on a SiC engineered substrate is assessed and compared with the reference. The maximum short-circuit withstand time (t_{SCWT}) for each type was determined by gradually increasing the short-circuit duration by 50 ns until either failure occurred or a change in one of the static parameters was observed. The initial short-circuit time was set to 500 ns and the DC-link voltage was set to 800 V. Measurements were taken at $T_{initial}$ = 25°C and 175°C. Five DUTs were tested for each condition and device technology. A typical SC I waveform is shown for both device technologies in Fig. 7a.



(a) short-circuit type I waveform (b) short-circuit current density peak

Fig. 7. Comparison of the short-circuit type I behavior and maximum short-circuit current density peak at different $T_{initial}$ for V_{DC} = 800 V and V_{GS} = -5 V/18 V.

A significant difference in short-circuit behavior was not observed. However, a slightly higher short-circuit current density was noted for the device based on a SiC engineered substrate. Fig. 7b compares the measured maximum short-circuit current density as a function of $R_{DS(on),sp}$ for the measured $T_{initial}$. At each measured initial temperature, the maximum short circuit current remains within the same range, irrespective of the substrate used and the corresponding specific on-state resistance. The short-circuit current is primarily determined by the n-channel and, thus, the cell

design. Hence, the substrate resistance does not influence the short-circuit current. The saturation current ($I_{D,sat}$) of the MOS-channel, and thus the short-circuit current, can be calculated using the following equation:

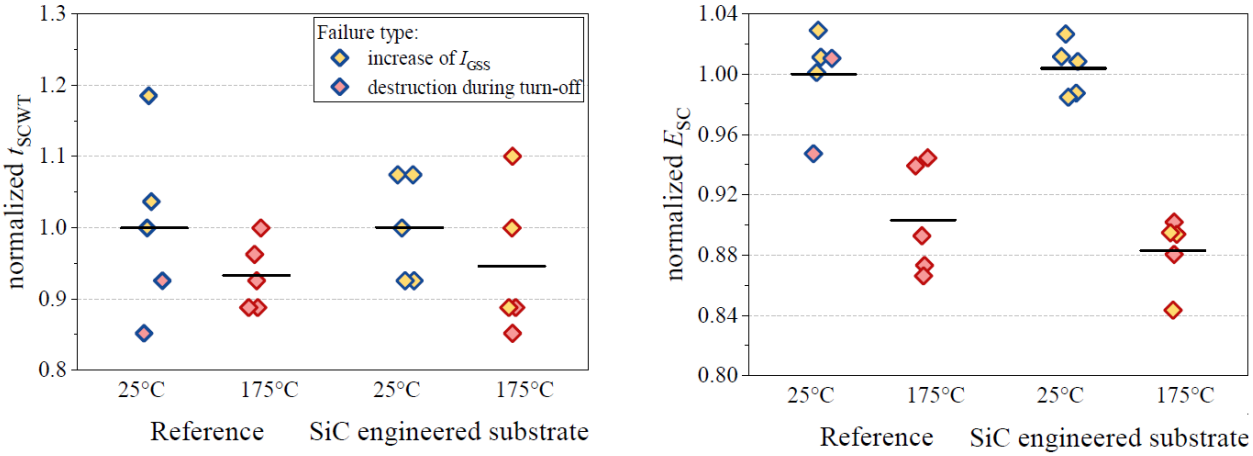
$$I_{\mathrm{D,sat}} = \frac{k}{2} \cdot \left(V_{GS} - V_{GS(th)}\right)^2 \quad (1)$$

with channel conductivity

$$\kappa = \frac{W \cdot \mu_n \cdot C_{ox}}{L} \quad (2)$$

where W - channel width, μ_n - mobility of electrons in the channel, C_{ox} - gate oxide capacitance, L - length of channel [9]. Fig.7b further indicates that within a device group, a lower specific resistance results in a higher short-circuit current. This effect is e.g. due to variations in the threshold voltage. In particular, a lower threshold voltage reduces channel resistance, leading to a lower total on-resistance. Additionally, a lower threshold voltage results in a higher short-circuit current, as described by Equation 1. At elevated temperature, the short-circuit current density decreases due to the reduction in the charge carrier mobility within the channel and bulk region.

Fig. 8 shows the obtained maximum short-circuit withstand time and the corresponding energy for both device technologies at different $T_{initial}$. Considering the average value for both, short-circuit withstand time and corresponding energy, no substantial difference between the two technologies is found. The variation in the maximum current peak leads to a variation in the achieved short-circuit duration. The failure of the DUT could be detected either by an increase in the gate leakage current (I_{GSS}) after the short-circuit stress or by the destruction of the device during the turn-off phase of the short-circuit.

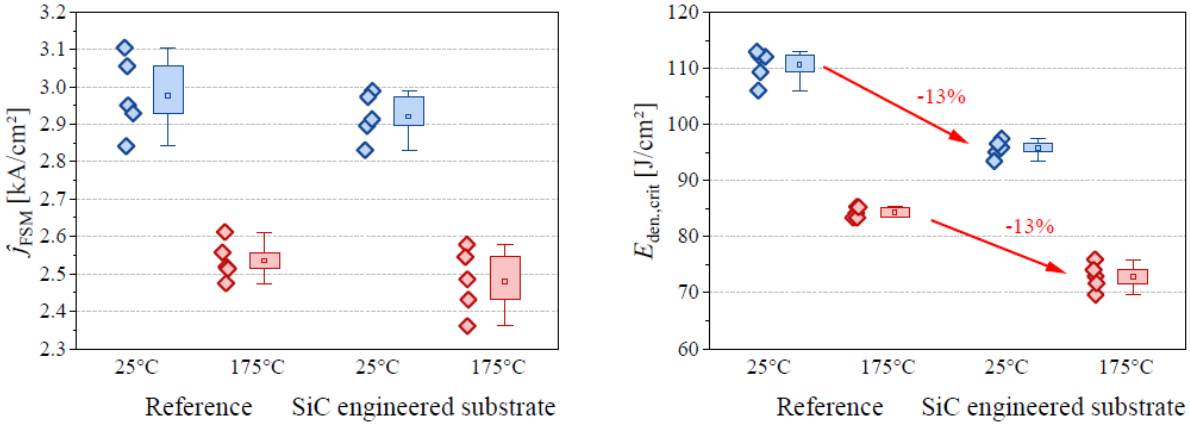


(a) critical short-circuit withstand time (b) critical short-circuit energy

Fig. 8. Comparison of the short-circuit type I capability at different $T_{initial}$ for V_{DC} = 800 V and V_{GS} = -5 V/18 V. (Note: line represents the mean value for each device group).

Surge Current Behavior. The surge current robustness of the SiC MOSFET based on a SiC engineered substrate in 3rd quadrant was evaluated with respect to a 10 ms current half-sine wave. The surge current capability was determined by increasing the surge current amplitude stepwise, till the DUT failed or a static electric parameter indicated the imminent destruction of the device. The investigation was carried out with a V_{GS} of -5 V, at two different $T_{initial}$ of 25°C and 175°C. Five DUTs were tested for each condition and device technology. A comparison of the surge current capability in terms of critical current density amplitude and corresponding energy density is given in Fig. 9. The device based on a SiC engineered substrate shows no significant change in the critical current density amplitude for both $T_{initial}$. However, the critical energy leading to failure is 13% lower for the device based on SiC engineered substrate. To analyze this behavior, a comparison of the surge current behavior was conducted. Fig. 10 shows a lower voltage drop during the surge

current for the device based on a SiC engineered substrate, leading to an 11% reduction in surge current energy. This reduction is explained by the low resistivity of the polycrystalline SiC. The reduction in critical energy density is expected, in principle, to lead to a higher surge current capability. Although the voltage drop and corresponding energy density decrease during the surge current, no significant change was observed in the critical surge current amplitude. Instead, a reduction in critical energy density was detected by 13% indicating that a critical temperature is reached at lower energy density levels. A failure of the devices was identified by an increase in I_{GSS} for both device technologies. The molten aluminium can damage the gate insulation, which may result in a short between gate and source contacts.



(a) critical surge current density amplitude (b) critical surge current energy density

Fig. 9. Comparison of the surge current capability at different $T_{initial}$ for V_{GS} = -5 V and t_{Surge} = 10 ms.

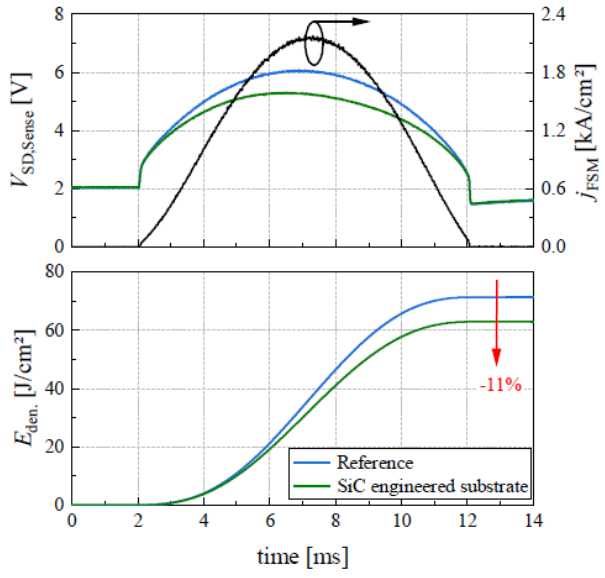


Fig. 10. Comparison of the surge current behavior at t_{Surge} = 10 ms, V_{GS} = -5 V and $T_{initial}$ = 175°C.

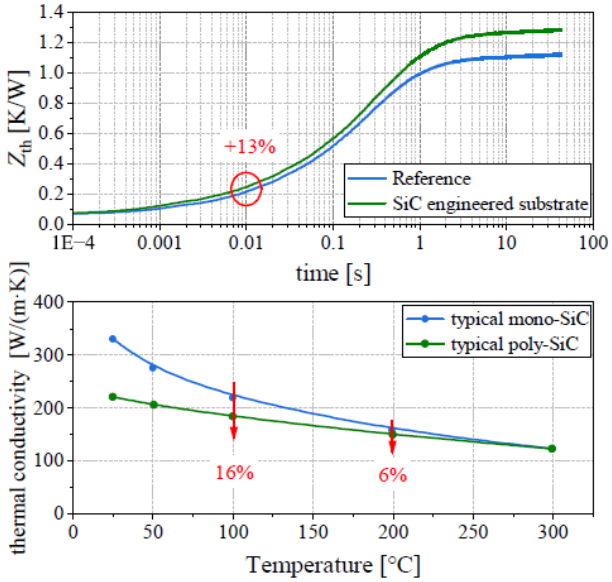


Fig. 11. Comparison of the thermal impedance Z_{th} of the devices and thermal conductivity of the substrates [4].

The results indicate a difference in thermal behavior between the two device technologies. The thermal behavior was evaluated through thermal impedance measurements, as depicted in Fig. 11. The thermal resistance during surge current could be approximated with the thermal impedance $R_{th} = Z_{th}(t=t_{surge})$. At this point, the device based on a SiC engineered substrate exhibits a 13% higher ther- mal resistance. The polycrystalline SiC has a lower thermal conductivity than monocrystalline SiC (see Fig. 11). However, the difference in thermal conductivity decreases at elevated temperature, thus reducing its impact during surge current as the device can reach temperatures above 300°C. Further, the chip is 30% thicker, which further increases thermal resistance. Nonetheless, the thicker chip also provides higher thermal capacity, partially counteracting the increased thermal resistance.

Summary

This study explores the dynamic behavior and robustness of MOSFETs fabricated using SiC engineered substrates, compared with those based on purely monocrystalline substrates. The results indicate that MOSFETs based on a SiC engineered substrate exhibit a 13% reduction in on-state resistance, attributed to the lower specific resistance of the polycrystalline SiC. The analysis of the reverse recovery behavior reveals that the MOSFETs based on a SiC engineered substrate achieve a lower reverse current peak and shorter reverse recovery time, especially at elevated temperatures and high current densities, resulting in a reduced reverse recovery charge and losses. TCAD simulations indicate that these improvements can probably be explained by a reduced electron injection and reduced hole density. In terms of robustness, no significant differences were observed in short-circuit type I behavior when comparing MOSFETs with a SiC engineered substrate to their monocrystalline counterparts. The reduction in substrate resistance does not lead to an increase in short-circuit current. However, a decrease in critical energy density during surge current events was noted, despite the critical current density remained unchanged. This decrease is attributed to variations in thermal behavior, which are partially due to the lower thermal conductivity and higher thickness of the MOSFETs based on a SiC engineered substrate.

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