Key Engineering Materials
ISSN: 1662-9795, Vol. 1024, pp 57-64
doi:10.4028/p-rS5BUg

Submitted: 2024-09-21
Revised: 2025-08-02
Accepted: 2025-08-04
Online: 2025-09-12

Device Performance and Reliability of SiC CMOS up to 400°C

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Keywords: MOSFET, CMOS, Field Effect Mobility, Threshold Voltage, Chemical Vapor Deposition, Transfer Characteristics, Interface Traps, Reliability, BTI

Abstract. This study evaluates the performance and reliability of SiC n- and p-MOSFETs across a temperature range from room temperature up to 400˚C, focusing on field effect (FE) mobility and threshold voltage variations under high thermal and bias stress conditions. By analyzing the variations in field effect mobility and threshold voltage under different stress conditions, our study illustrates distinct behaviors between devices with thermally grown oxides and those with chemical vapor deposited (CVD) oxide layers, underscoring significant differences in long term performance. Results indicate that while n-MOSFETs maintain threshold voltage shifts below 3% and exhibit robust characteristics up to 400˚C, p-MOSFETs exhibit permanent threshold voltage shifts of up to 10% and mobility reductions of 15% particularly above 300˚C DC stress. The 2 nm ultrathin thermal (UT) SiO_2 followed by 40nm CVD SiO_2, outperform thermal oxides, sustaining less degradation in mobility and less shift in threshold voltage under bias temperature instability (BTI) conditions at voltages up to ±25V and temperatures as high as 400˚C. This research advances SiC CMOS technology by confirming that SiC n-MOSFETs are ready for high-temperature circuit applications, while highlighting the need for further improvement in p-MOSFETs to enhance their reliability under extreme conditions.

Introduction

Silicon carbide (SiC) has accumulated significant attention in the semiconductor industry due to its outstanding physical and electronic properties [1]. As a wide bandgap material, SiC is inherently capable of operating at higher electric fields, power levels, and thermal environments compared to traditional silicon-based devices. This robustness makes SiC an ideal candidate for power electronics, particularly in applications requiring high efficiency and reliability under extreme conditions such as in electric vehicles, aerospace, and industrial power systems [2], [3]. SiC distinguishes itself from other wide-bandgap semiconductors by allowing the straightforward growth of gate oxides in a similar manner to silicon. This key advantage positions SiC as a superior choice for applications requiring wide bandgap materials due to its ease of fabrication and enhanced device performance. Despite its significant advantages, SiC technology, particularly in metal-oxide-semiconductor field-effect transistors (MOSFETs), encounters notable challenges that can impact device performance and reliability. One such challenge is the poor interface quality between the SiC substrate and the gate oxide. The interface quality is crucial because it affects the mobility of charge carriers and the stability of the device's electrical characteristics under different operating conditions. Imperfections at this interface, such as traps and defects formed mainly due to carbon cluster formations and oxygen

vacancies, lead to increased electron scattering, reduced carrier mobility, and fluctuations in threshold voltage, which in turn compromise the efficiency and lifespan of the MOSFET [4], [5], [6].

Due to these imperfections, high-temperature operations can accelerate the failure of SiC MOSFETs, worsening issues like increased leakage currents and dielectric breakdown [7]. One of the critical issues in SiC MOSFETs is the reliability of the gate oxide layer when subjected to temperatures exceeding 150°C, a standard threshold in power electronics [8], particularly regarding the degradation mechanisms that impact their long-term stability and performance. The reliability concerns arise from the significant presence of traps at the SiO_2/SiC interface. Strategies such as enhanced passivation layers and thermally stable contact materials are critical for maintaining device performance and longevity under these conditions. Among the reliability concerns, bias temperature instability (BTI), particularly negative BTI, poses a significant challenge for SiC MOSFETs, manifesting as large shifts in threshold voltage (V_{TH}) [9], [10], [11]. These shifts are exacerbated at high temperatures, leading to degraded device performance and lifetime [7]. The underlying cause often ties back to the quality of the gate oxide. Thermally grown silicon dioxide (SiO_2) on SiC tends to exhibit a higher density of interface traps (D_{it}), which are accentuated under thermal stress and electric bias, further compounding reliability issues [12], [13].

This paper represents the behavior of n- and p-type SiC MOSFETs across a wide temperature range, from room temperature up to 400°C, with a particular focus on mobility and threshold voltage variations. By conducting a comparative study of devices with thermally grown oxides versus those with CVD oxides, it highlights distinct performance differences under various stress conditions. Our results underscore the superior stability and performance of deposited oxide layers compared to traditional thermal oxides, particularly in high-temperature applications. It also provides new findings on how n- and p-MOSFETs respond differently to temperature-related stress, with n-MOSFETs showing less change in performance under these conditions, offering insights for improving SiC CMOS for extreme environment.

Fabrication Process

The fabrication of n- and p-channel MOSFETs was conducted at Analog Devices Inc., utilizing 6-inch epitaxially grown SiC wafers. The implanted channels were doped with nitrogen and aluminum at concentrations of $4x10^{16}$ cm^{-3} and $2x10^{16}$ cm^{-3} for n- and p-channels, respectively. A visual overview of the design is illustrated in Fig. 1. This study investigates three different gate oxide conditions: a standard thermally grown oxide and two CVD oxides, which were grown to thicknesses of 20 nm and 40 nm using ADI's established CVD method. Additionally, a 2 nm ultrathin thermal oxidation step was applied prior to the CVD process to enhance nucleation. More comprehensive details of the fabrication process are available in [9], [14].

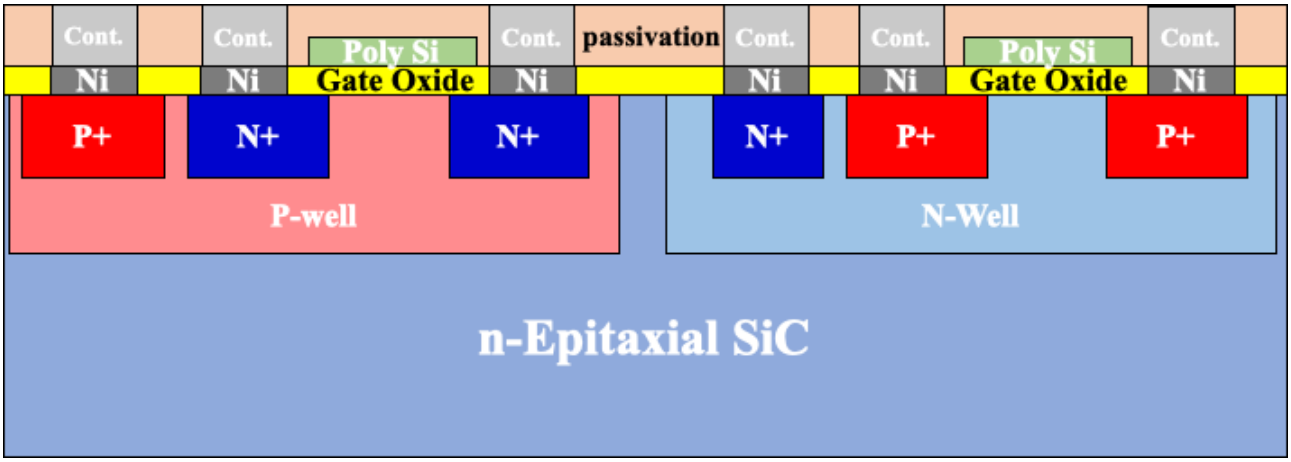

Fig. 1. The cross-section of the n- and p-channel MOSFETs is selectively illustrated that relates to the key findings of this study. For a comprehensive view and detailed analysis of the full cross-section, refer to the documentation presented in [9].

Characterization Method

Oxide capacitances were extracted by driving the device into accumulation to determine the effective oxide thickness (EOT). For all transfer characteristics, ± 0.1 V was applied to drain while source and substrate was at 0 V. All devices have 30 µm channel length and 30 µm channel width to keep *W/L*=1 and avoid any geometry effect. The peak FE mobility was extracted using,

$$\mu_{FE(peak)} = \frac{\max\left(\frac{\delta I_D}{\delta V_{GS}}\right)}{V_{DS} C'_{OX}} \quad (1)$$

Where, drain current = I_D, gate to source voltage = V_{GS}, drain to source voltage=V_{DS}, oxide capacitance in accumulation per unit area = C'_{OX} (in F/cm^2). To perform BTI characteristics, stress-sense-stress technique was used [11]. The threshold voltage was characterized using the intercept of maximum slope via linear extrapolation of I_D vs V_{GS} characteristics [15]. In order to minimize the time between two "stress" stage the "current level" is chosen from the drain current at threshold voltage and voltage shift was observed to achieve that "current level" is considered as V_{TH} shift for BTI measurement. This setup enabled the application of very low voltage stress for a very short time to "sense" the threshold voltage shift after each "stress" step.

Results and Discussions

Device Characteristics vs. Temperature. Fig. 2 illustrates the transfer characteristics of n- and p-channel MOSFETs with gate oxide formed using ultrathin thermal SiO_2 and thick CVD grown SiO_2 across a range of temperatures. As temperatures rise from room temperature (20°C) to 400°C, there is a decrease in the threshold voltage, attributed to the enhanced thermal voltage (ϕ_t) which boosts the inversion charge density in the channel of both n- and p-MOSFETs [16]. FE mobility in SiC predominantly increases with temperature due to mobility predominantly limited by Coulombic scattering [9], [17]. Lattice damage during implantation, incomplete recovery after activation annealing, surface roughness and large density of traps at/near interface provide significant amount of scattering centers for charge carriers. Initially, field effect (FE) mobility increases with temperature. As the device characteristics are analyzed beyond this point, the influence of Coulombic scattering diminishes with increasing temperature, while phonon scattering becomes more prevalent, acting as main constraints on mobility at elevated temperatures. As a result, the mobility shows a downward trend for both n- and p-channel MOSFETs as temperatures rise, with the decline starting around 300˚C for n-MOSFETs and 130˚C for p-MOSFETs. The complex interplays of different scattering mechanisms shapes the device performances at different temperatures.

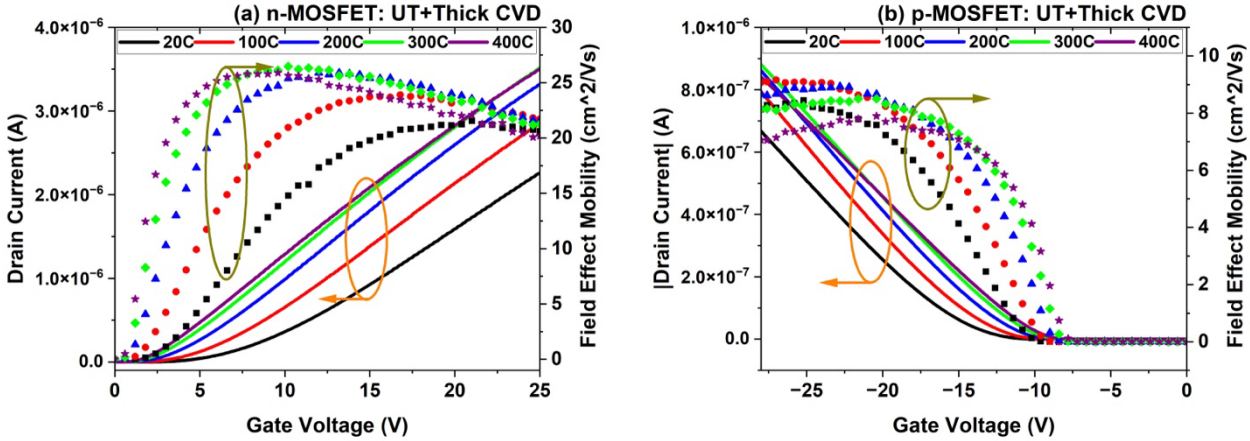

Fig. 2. Transfer characteristics of (a) n-channel and (b) p-channel MOSFETs with temperature ranging from 20˚C to 400˚C. Both MOSFETs have ultrathin thermal (UT) SiO_2/40 nm thick CVD grown SiO_2.

To gain a deeper understanding of how device mobility is influenced by temperature, the field effect (FE) mobility across different gate oxide conditions is extracted in Fig. 3. These conditions include a 50 nm thermal oxide, 2 nm UT SiO_2 + 40 nm CVD SiO_2, and 2 nm UT SiO_2 + 20 nm CVD SiO_2. The measurement temperature was varied from 20°C to 400°C. The FE mobility was derived using Eq. 1 and subsequently normalized to the corresponding room temperature mobility value to ensure consistency in comparison.

The variance in temperature behavior between n- and p-MOSFETs can be largely attributed to the fundamental scattering mechanisms affecting carrier mobility [16]. As temperature rises, charge carriers gain kinetic energy, enhancing their ability to overcome the potential barriers of ionized impurities. This results in a reduced probability of carrier scattering by these impurities, thereby increasing the Coulombic scattering-limited mobility. However, alongside this increase, temperature also amplifies lattice vibrations within the semiconductor material, enhancing phonon scattering. Phonon scattering involves the interaction of charge carriers with the vibrating atoms of the lattice, which increases with temperature due to greater vibrational energy. As a consequence, phonon scattering becomes a significant limitation on mobility at higher temperatures, ultimately leading to the observed decrease in mobility as temperatures approach and exceed the transition point. From Matthiesen's rule,

$$\mu_{total} = \frac{1}{\frac{1}{\mu_C} + \frac{1}{\mu_L} + \cdots} \tag{2}$$

where, μ_C and μ_L are coulombic scattering limited and phonon scattering limited mobility respectively. In SiC MOSFETs with SiO_2 as gate dielectric, the FE mobility is limited by coulombic scattering with μ_C being much less than μ_L. This is due to traps at SiC/SiO_2 interface [4]. With the increase in temperature, μ_C increases which gives rise to the effective mobility in Matthiesen's rule (Eq. 2). However, μ_L decreases with increase in temperature due to increased vibrational energy from higher temperature which eventually overturns the total mobility dependent solely on μ_L.

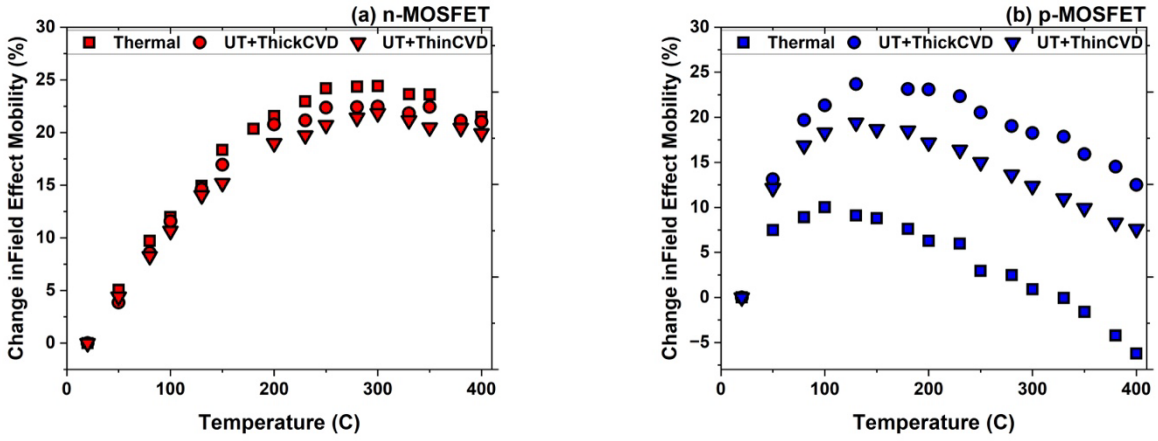

Fig. 3. Percentage change in FE mobility vs temperature for (a) n-channel and (b) p-channel MOSFETs.

For n-MOSFETs, there is a continuous increase in peak mobility up to a temperature of 250-300°C, at which point the mobility begins to decrease. This peak and subsequent decline mark a transition from mobility being primarily limited by Coulombic scattering to being limited by phonon scattering and the "transition point" indicates the temperature at which phonon interactions become sufficiently prominent to overshadow the effects of Coulombic scattering. For p-MOSFETs, however, this transition occurs at a significantly lower temperature of 100-130°C. This is due to the charge carriers (holes) in the p-MOSFETs have significantly heavier effective masses compared to the charge carriers (electrons) in n-MOSFETs [1]. The carriers with heavier effective mass have more energy at higher temperature to overcome the barrier for coulombic scattering centers which diminishes the effect of coulombic scattering quicker than lighter counterparts. Hence, the p-MOSFETs have lower

"transition" temperature compared to n-MOSFET. Furthermore, the mobility vs. temperature results for p-MOSFETs are very different for different gate oxide conditions compared to n-MOSFETs. The traps near conduction band are very much optimized over the last few decades with different annealing and POA while there is limited research on traps near valence band and the difficulty in extraction of traps near valence band. The difference in mobility change vs. temperature (Fig. 3 (b)) can be attributed to the differences in traps distribution near the valence band.

BTI vs. Temperature. BTI analysis is not only critical to diagnose the reliability and longevity of MOSFETs under combination of electrical and thermal stress but also provides crucial information about gate oxide quality and interface traps. A stress bias is applied at the gate while source, drain and substrate are grounded. The threshold voltage shifts due to injection of charges into the dielectric traps located at or near the oxide/semiconductor interface with different stress time. Positive and negative bias temperature instability measurements were conducted on both n- and p-channel MOSFETs. In order to contrast the results, the thermal oxide condition was characterized alongside the UT+CVD oxide condition. Fig. 4 shows the PBTI and NBTI shift of threshold voltages with ±25V (4MV/cm) stress and the temperature was varied from room temperature to 400˚C.

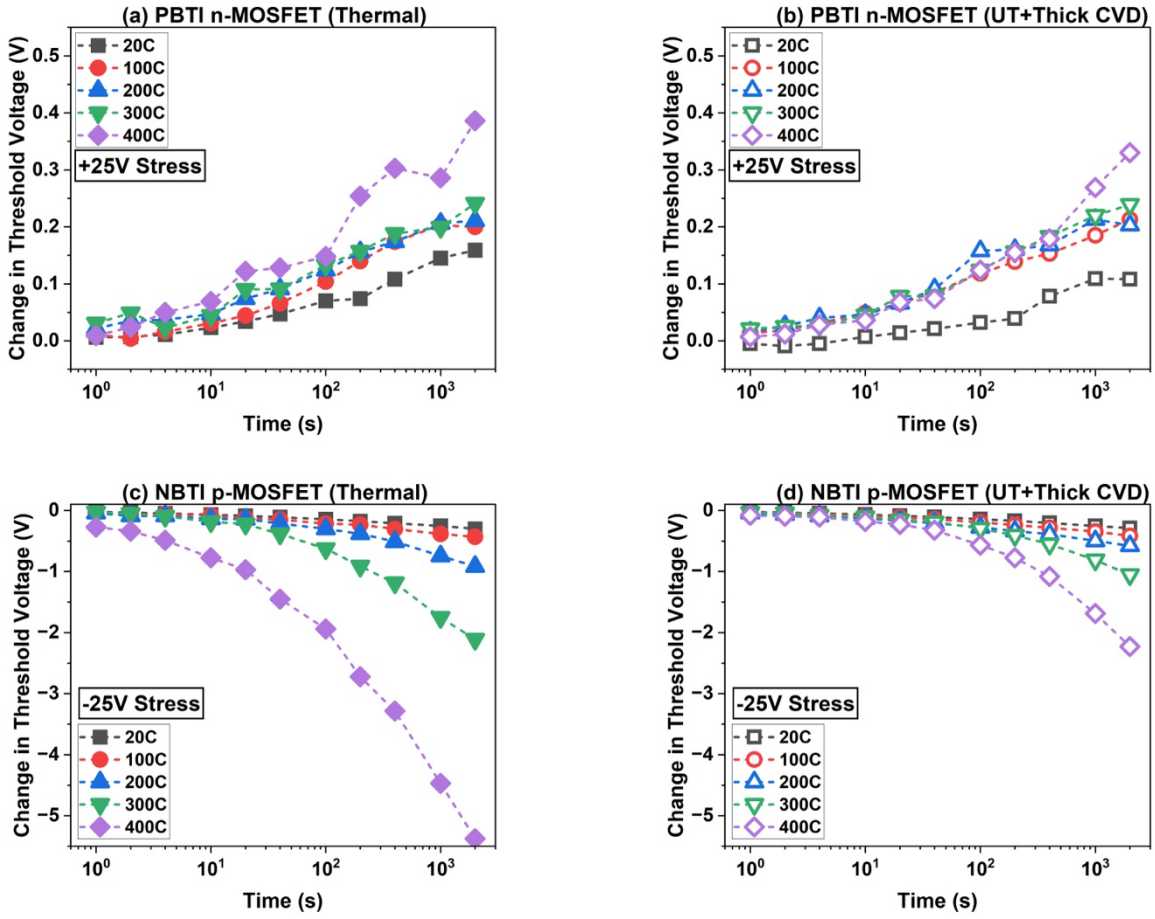

Fig. 4. BTI characteristics of n- and p-MOSFETs at various temperature with ±25 V DC stress. For each measurement, the "current level" was chosen before applying any stress at corresponding temperature.

In Fig. 4 (a) and (b), The PBTI shifts for both thermal and deposited oxides, respectively, indicate that both types of oxide are effectively optimized. The traps near the conduction band are passivated sufficiently to prevent substantial shift in the threshold voltage. As the temperature increases, the shift in V_{TH} also increases. Even though same gate bias was applied to stress the dielectrics, the reduction in threshold voltage at higher temperature causes an increase in the effective electric field. As a result, the V_{TH} shifts are slightly larger at higher temperature. The effective electric field can be extracted using the following equation-

$$E_{eff} = \frac{V_{GS} - V_{TH}}{EOT} \quad (3)$$

where, E_{eff} is the electric field that acts on the oxide and EOT is the effective oxide thickness. The electric field applied at the gate has two-fold role in MOS structure; one part acting upon necessary band bending to form the channel which essentially is equal to $\frac{V_{TH}}{EOT}$ whereas, the rest acts on the gate oxide. Few data points are off from the trend which indicates the charged mobile ion movement in gate oxide which can be ignored from the analysis. Nevertheless, the shift in V_{TH} for both types of oxides is less than 5% even with measurement temperature as high as 400˚C.

In Fig. 4 (c) and (d), we observe significant threshold voltage shifts in p-MOSFETs under -25V bias stress across different temperatures, more so than in n-MOSFETs. Due to the higher initial threshold voltage in p-MOSFETs, configured by using the same n+ poly-Si gate material and the presence of un-passivated interface traps near the valence band, the effective gate oxide electric field is much smaller compared to n-MOSFETs (-2.2 MV/cm for thermal oxide and -2.7 MV/cm for deposited oxide). The pronounced shift in p-MOSFETs is linked to the un-passivated carbon clusters and oxygen vacancies at the interface [12]. Additionally, a secondary slope becomes evident more quickly at higher temperatures, indicating an accelerated activation of defect states, which impacts the NBTI behavior significantly.

The prolonged bias application could activate deep-level traps, resulting in a distinct secondary slope in BTI studies [9]. These BTI characteristics include an increase in interface trap density (D_{it}), a reduction in field effect (FE) mobility, and a rise in threshold voltage, which notably do not revert even after the stress is removed. Higher temperatures increase band bending due to increased thermal voltage (ϕ_t) and facilitate the thermal generation of carriers. The band bending pushes more traps closer to the valence band at the gate oxide interface, which in turn activates additional deep-level traps under prolonged stress. Consequently, this process precipitates the emergence of the secondary slope earlier in the BTI timeline, thereby affirming the complex interplay among temperature, bias stress, and trap activation in p-MOSFETs. Since it has already established that thermal oxide has more traps near valence band compared to our novel deposited oxide, the secondary slope of thermal oxide starts at lower temperature than that of deposited oxide.

To complete our analysis, FE mobility was extracted following each BTI stress evaluation, with Fig. 5 demonstrating the percentage change in FE mobility in relation to its initial state. While n-MOSFETs showed a negligible change in mobility (<1.5%) at and up to 400˚C across both oxide types, p-MOSFETs registered more substantial declines: 5% for deposited oxides and 15% for thermal oxides at the same temperature. This marked degradation in thermal oxides correlates with their earlier activation of secondary slopes and a higher presence of interface traps near the valence band. This further establishes the enhanced stability and efficiency of our newly developed deposited oxides over conventional thermal oxides.

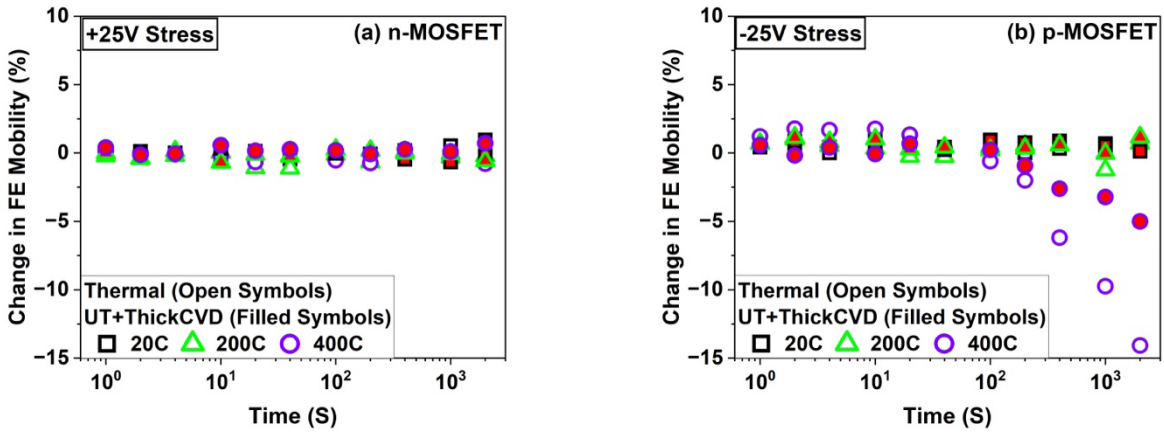

Fig. 5. FE mobility degradation after BTI measurement at varied temperature for (a) n-MOSFET and (b) p-MOSFET with thermal and deposited oxides.

Conclusion

In this study, n- and p-MOSFETs fabricated on 6-inch 4H-SiC wafers demonstrated distinct behaviors across different gate oxide conditions, from room temperature up to 400°C. Devices with ultrathin thermal combined with CVD SiO_2 exhibited superior field effect mobility and stability compared to those with traditional thermal oxides, particularly under high-temperature conditions. Bias temperature instability (BTI) tests revealed minimal threshold voltage shifts for n-MOSFETs under extreme thermal stress, highlighting their durability, whereas p-MOSFETs faced significant permanent threshold voltage shifts and mobility reductions above 300°C, pointing to un-passivated deep level traps within the bandgap near the valence band. These findings suggest the necessity for enhanced passivation strategies, particularly near the valence band, to improve the performance and reliability of SiC MOSFETs, and demonstrate that deposited oxide stacks offer a more reliable alternative to traditional thermal oxides for high temperature applications.

Acknowledgement

The work was funded by Advanced Research Projects Agency-Energy (ARPA-E) U.S. Department of energy, under Award Number DE-AR0001028

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