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Fabrication of 4H-SiC Low Gain Avalanche Detectors (LGADs)

Ben J. Sekely[1,2,a], Yashas Satapathy[1,2,b], Tao Yang[3,c], Greg Allion[4,d], Philip Barletta[4,e], Steve Holland[3,f], Stefania Stucci[5,g], Carl Haber[3,h], Spyridon Pavlidis[2,i], John F. Muth[2,j*]

[1]Department of Materials Science and Engineering, North Carolina State University, Engineering Bldg I, 911 Partners Way, Raleigh, 27606, NC, U.S

[2]Department of Electrical and Computer Engineering, North Carolina State University, 2410 Campus Shore Dr, Raleigh, 27606, NC, U.S

[3]Physics Division, Lawrence Berkeley National Laboratory, 1 Cyclotron Rd, Berkeley 94720, CA, U.S

[4]NCSU Nanofabrication Facility, North Carolina State University, 2410 Campus Shore Dr, Raleigh, 27606, NC, U.S

[5]Brookhaven National Laboratory, 98 Rochester St, Upton, 11973, NY, U.S

[a]bjsekely@ncsu.edu, [b]ysatapa@ncsu.edu, [c]tao.yang@lbl.gov, [d]grallion@ncsu.edu, [e]pbarlet@ncsu.edu, [f]seholland@lbl.gov, [g]stucci@bnl.gov, [h]chhaber@lbl.gov, [i]spavlidis@ncsu.edu, [j]muth@ncsu.edu

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Abstract. Low gain avalanche detectors (LGADs) offer high temporal resolution for high energy particle detection, which is critical for next generation experiments in hadron colliders. While silicon LGADs (Si-LGADs) have rapidly matured in the last decade, research into silicon carbide (SiC) LGADs has only recently begun. By accounting for fundamental differences in material properties and fabrication processes, we present a prototype device design and process flow for 4H-SiC LGADs with etch-based isolation. Critical steps of the process flow and their results are discussed, including plasma etching, passivation, and the formation of low resistivity contacts. Electrical characterization (I-V, C-V) shows sufficient depletion of the device structure to demonstrate low-gain charge carrier multiplication.

Introduction

In high energy hadron colliders, such as the High Luminosity Large Hadron Collider (HL-LHC), and possible future colliders, events contain increasingly large numbers of minimum ionizing particles (MIPs), with significant overlap of many simultaneous collisions in close proximity. Present tracking systems, based upon highly segmented silicon pixels or strips lack the timing resolution required to separate these events. Next generation collider detectors, now in preparation, will contain new fast timing devices, referred to as Silicon Low Gain Avalanche Detectors (Si-LGADs) with timing resolution in the range 30-50 ps, but with limited spatial resolution. Si-LGADs offer better time resolution than current pixels and strips. This is due to thinner drift regions allowing charge carriers to quickly travel across the device and signal amplification through the use of an avalanche mechanism [1].

Si-based detectors are however susceptible to bulk radiation damage effects and consequently must be operated at temperatures around -40 °C requiring complex, bulky, and expensive cooling systems.

The 2019 Department of Energy Basic Research Needs for High Energy Physics Detector R&D identified a number of priority research directions including improved spatial resolution for fast timing, the application of new alternative materials, and reduced cooling and mass requirements [2]. In the present work we are developing LGADs to address these directions by using 4H-SiC rather than Si.

There are several reasons to adopt 4H silicon carbide (4H-SiC) in place of Si in LGADs. Firstly, the ionization coefficient of holes exceeds that of electrons in SiC, unlike in Si. This, combined with the fact that the saturation velocity of electrons in SiC is over twice that of holes in silicon, means that a SiC LGAD structure should be constructed with n-type drift and gain layers. Consequently, the fast signal comes from the higher mobility avalanche electron drifting back across an n-type epitaxial layer, rather than slower hole drifting across a p-type layer in the case of a Si LGAD. Additionally, the wider band gap and greater atomic displacement energy threshold of 4H-SiC are expected to reduced the dark current and lead to a higher theoretical radiation resistance, respectively [3, 4]. Moreover, the larger thermal conductivity of SiC can simplify cooling requirements and reduce system complexity. 4H-SiC is also of interest due to its high technological maturity and large commercial availability. For all of these reasons, 4H-SiC is an attractive polytype choice for LGAD device development.

In the following, we describe the epitaxial design and development of first generation SiC LGADs for particle detectors. Each of the fabrication steps has been characterized. The resulting LGADs and associated test structures have been electrically tested to confirm they adhere to our expectations. We note that α-particle irradiation with a $^{210}_{84}$Po source using the same devices is not presented here, butm treated in a separate publication [5].

Epitaxial Design and Characterization

These stacks were purchased as 6” wafers from a commercial vendor with a 4° off-axis cut. The epi-stack shown in Fig. 1 is designed to collect holes at the front-side p-type contact layer. Thicknesses and doping concentrations were determined using Synopsys TCAD simulations with the following considerations:

The nitrogen-doped (N-doped) n-type drift region is as low doped as possible to decrease the depletion voltage and therefore operating voltage, allowing for reduced scattering of mobile charge carriers and a better timing performance. The concentration is the minimum dopant concentration that could be commercially achieved. The drift layer thickness requires a balance: a thin region achieves a better timing resolution as the carriers travel shorter distances but reduces the MIP interaction volume and generates fewer carriers, requiring a higher gain to achieve a higher signal-to-noise ratio and be read by the read-out electronics.

The N-doped gain layer must be highly doped to create a large E-field at the p-n junction to quickly sweep out generated e-h pairs as well as induce avalanching. The gain layer thickness must be thick enough to allow for carrier multiplication but thin enough to keep the device operating at low gain (10 - 20) [6]. Low gain is needed to amplify signals generated by MIPs since too high a gain can amplify background noise and increase event pileup that occurs when signals from multiple MIPs are too close in timing and are indistinguishable from one another.

The aluminum doped p-type layer must be highly doped to form a good metal-semiconductor contact and minimize the resistance generated carriers experience before being collected as signal. Additionally, the high p-type creates a large E-field at the p-n junction.

These stacks were epitaxially grown by a commerical vendor using metal-organic chemical vapor deposition (MOCVD) with the buffer and drift layers grown in one run, followed by the growth of the gain and p-type contact layer. A PiN diode epi-stack was grown similar to the LGAD but without the gain layer (Fig. 1). Secondary-Ion Mass Spectroscopy (SIMS) data confirms the doping and thickness of the contact and gain layer. Doping of the drift region is low enough to be outside the detection limit. The LGAD devices were fabricated in tandem with the PiN diodes. The two are compared to demonstrate carrier multiplication in the LGAD. The controllable low-gain mechanism of these devices is shown in a separate publication [5].

Process Flow

Device fabrication was carried out on a 1” die from the 4H-SiC epi-stacks shown in Fig. 1. Test structures and devices have been fabricated with the outlined process shown in Fig. 2. The device layout includes mesas of varying sizes (75 - 600 μm) and test structures for process testing and

electrical characterization. Additional devices are being fabricated with this process flow in epi-stacks with varying gain layer doping concentration to investigate the effects on avalanching behavior, but are not discussed in this paper.

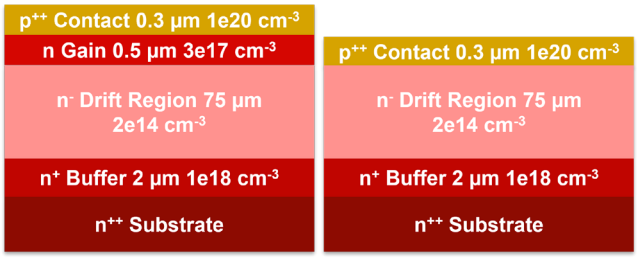

Fig. 1. Thickness and doping concentration of the left: LGAD and right: PiN diode.

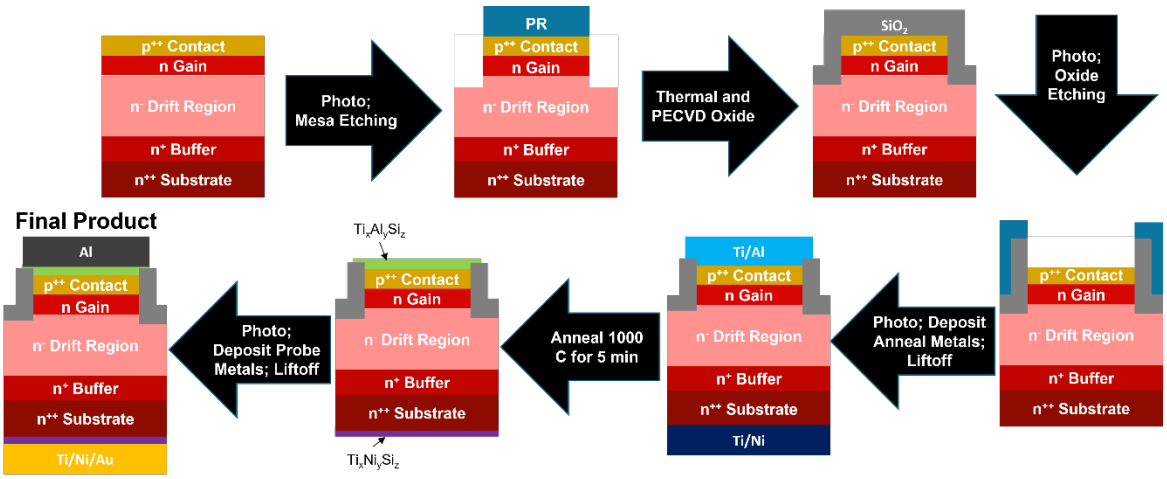

Fig. 2. Condensed process flow for the fabrication of an LGAD in 4H-SiC.

There exist several fabrication challenges when processing 4H-SiC. It is, for example, difficult to obtain smooth etched surfaces using plasma-based etch steps in 4H-SiC with high etch rates and achieve vertical sidewalls. Reduced surface roughness can be achieved using a select gas composition and pressure during Reactive Ion Etching (RIE) to obtain an etch of minimal roughness. This allows for a better interface between a passivation layer and the etched 4H-SiC and reduce the surface dark current from damage at the semiconductor surface. For LGADs, a good passivation strategy is important to reduce dark current and to minimize E-field enhancement at device edges and therefore avoid breakdown. Two different passivation methods were investigated: 1) plasma-enhanced chemical vapor deposition (PECVD) of silicon dioxide (SiO_2) and 2) thermal oxidation with a subsequent thicker PECVD SiO_2 layer. Devices are fabricated using each approach and the dark current is compared. Ohmic contacts are also desired in LGADs to minimize series resistance. The process for ohmic contact formation on p-type 4H-SiC is discussed since various thickness and compositional variations of metal stacks are used for p-type SiC contacts in the literature.

Reactive Ion Etching in 4H-SiC

Mesa etching is a relatively simple technique to control the E-field in the device. While E-field enhancement at the device edges using this approach is expected, which will reduce the expected break-down voltage of the devices, this approach is used to demonstrate initial device operation. Future implementations will target more sophisticated edge termination strategies, such as planar junction termination extensions (JTEs), which use ion implantation [1].

In this work, an etch recipe has been developed for a 4H-SiC mesa etch of 1.3 μm in depth in order to etch through the contact and gain layers and isolate the devices. RIE is used to etch the mesa structures and requires process refinement to achieve smooth surfaces for the required etch depth. A smooth etch surface is desired to reduce the number of surface defects that can contribute undesired leakage current paths, E-field enhancement and instability [7]. We use a photoresist mask rather

than metal since it is simple to deposit and remove. Compared to a metal mask, photoresists typically demonstrate reduced micromasking during the etch. Micromasking occurs when the etch mask is etched and redeposited on a previously exposed region, masking the region and creating a rougher etch result.

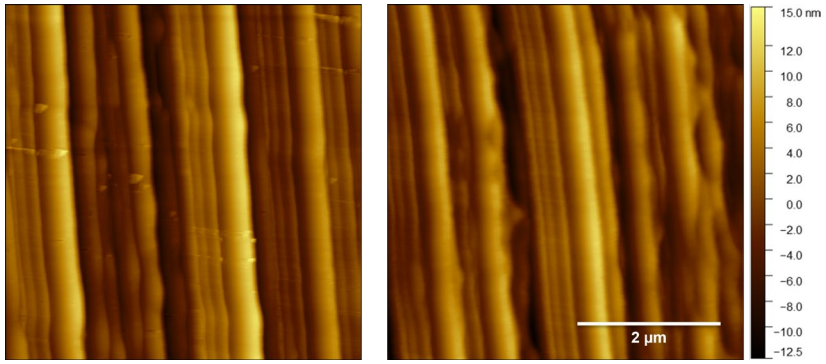

Fig. 3. AFM images of the left: unetched mesa and right: etched region.

The gasses used are a mixture of 68.8% fluoroform (CHF_3), 23% diatomic oxygen (O_2) and 8.2% argon (Ar). Fluoroform is used as a source for fluorine atoms and is primarily responsible for etching 4H-SiC. An oxygen gas flow of 20% demonstrates a good balance between etch rate and surface roughness in etched regions of 4H-SiC [8, 9].The RIE process of etching 4H-SiC with fluorinated and oxygenated species is described as a combination of physical ion bombardment and a chemically reactive process. The Si-terminated face of 4H-SiC is etched by fluorine ions while the C-terminated face is etched by both fluorine and oxygen ions [10]. Argon affects the etch process via physical bombardment, removing residual organics from the redeposited photoresist that might induce micromasking [11] and increase etch roughness.

A smooth etch result is demonstrated using atomic force microscopy (AFM) as shown in Fig. 3. The valley-to-peak heights in both cases is about 27.5 nm which indicates the etch is not roughening the silicon carbide. Using scanning electron microscopy (SEM) shown in Fig. 4, the angle of the etched mesa side walls are measured at 20°, indicating the selectivity of the SiC to the resist mask is low, as expected when using a photoresist mask. Vertical mesas are desirable to achieve a higher breakdown voltage and can be optimized in future studies.

Device Passivation Strategies

Device passivation is a critical step, in particular following mesa etching, to minimize surface traps capable of increasing dark current [12] or causing premature breakdown. Historically, researchers passivated 4H-SiC devices using thermally grown SiO_2 [13], Plasma-Enhanced Chemical Vapor Deposition (PECVD) SiO_2 and SiN [14], or with combinations of thermal oxides and deposited dielectrics [7]. Given the high thermal budget available at this stage in the process, we investigated two approaches: PECVD SiO_2 only, and the combination of dry thermal oxidation followed by PECVD oxide.

The PECVD SiO_2 was deposited using an Oxford Plasmalab 80 Plus PECVD with inlet gas con- centration of 53.3% helium (He), 32.0% nitrous oxide (N_2O) and 14.7% silane (SiH_4). The oxide was deposited at a pressure and temperature of 1000 mTorr and 300 °C, respectively. The alternate method consists of a thermal oxidation in a Titan II thermal oxidation chamber prior to the PECVD deposition. The sample is exposed to dry oxygen at 1100 °C for 5 hours. Before cooling down, the sample is annealed at the same temperature in a nitrogen environment.

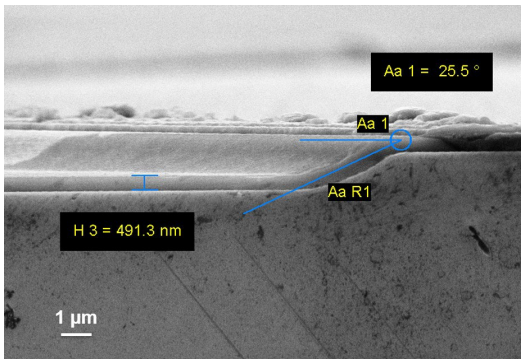

Fig. 4. Cross-sectional SEM image of a mesa in the 4H-SiC PiN diode. The sidewall and oxide thickness are measured at 25.5° and 491.3 nm, respectively.

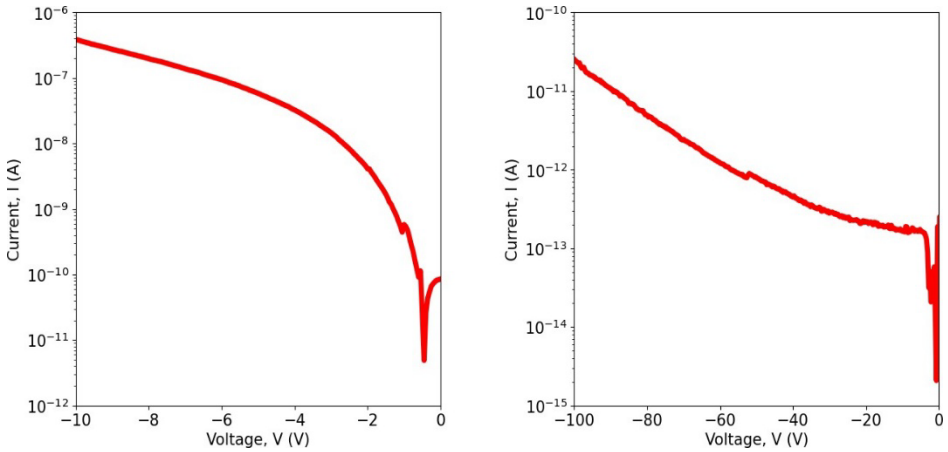

Fig. 5. Dark current of diodes passivated using left: only a PECVD oxide film and right: thermal oxidation and PECVD oxide film.

The total oxide thickness was measured using the SEM image shown in Fig. 4 in addition to a reflectivity measurement using a Filmetrics tool model LS-DT2. The total oxide thickness is 500 nm. The PECVD oxide is 450 nm resulting in a thermal oxide thickness of 50 nm.

The effectiveness of each passivation approach was evaluated by measuring the dark current of fabricated diodes. The resulting data is shown in Fig. 5. The dark current under a reverse bias of 10 V for a PECVD passivated device is hundreds of nA. However, the dark current for a device passivated with a thermal oxidation and subsequent PECVD oxide layer does not reach 0.1 nA at a reverse bias of 110 V. While the dark current shown here is larger than some 4H-SiC avalanching photodiodes (APDs) [15], it is comparable to others [7, 16]. Due to the reduced dark current, passivation via both thermal oxidation and PECVD SiO_2 are selected.

Low Resistivity Contacts

After selectively exposing the top of the mesa by RIE of the passivation layer, metal contacts are deposited using electron beam (e-beam) evaporation on both the back-side n^{++} substrate and top- side p^{++} contact layer. It is important to create ohmic contacts for LGADs in order to aid charge collection, as having a Schottky barrier will act as a current limiter by preventing charge carriers from travelling through the metal-semiconductor interface. While methods to create ohmic contacts differ in the literature, it has been found that Ni- and Al-based metal stacks are commonly used in creating ohmic contacts in n-type and p-type 4H-SiC, respectively [17, 18, 19]. In this process, Ti/Ni (10/100 nm) is deposited as the anode and Ti/Al (50/75 nm) as the cathode. The Ti on the anode promotes adhesion and uniform formation of a Ni_2Si layer during annealing [20] while the Ti in the cathode is used to create a Ti_3SiC_2 layer post-annealing [21], reducing the Schottky barrier height (SBH) at both interfaces. The Al will further reduce the SBH by diffusing towards the 4H-SiC surface during annealing and increasing the conductivity at the surface as Al is the p-type dopant of 4H-SiC [22]. The n-type and p-type contacts were simultaneously annealed at 1000 °C

for 5 min. in a N_2 environment. Afterwards, an Al (300 nm) layer and Ti/Ni/Au (30/50/50 nm) stack were deposited using e-beam evaporation as pad contacts for probing on the anode and cathode, respectively.

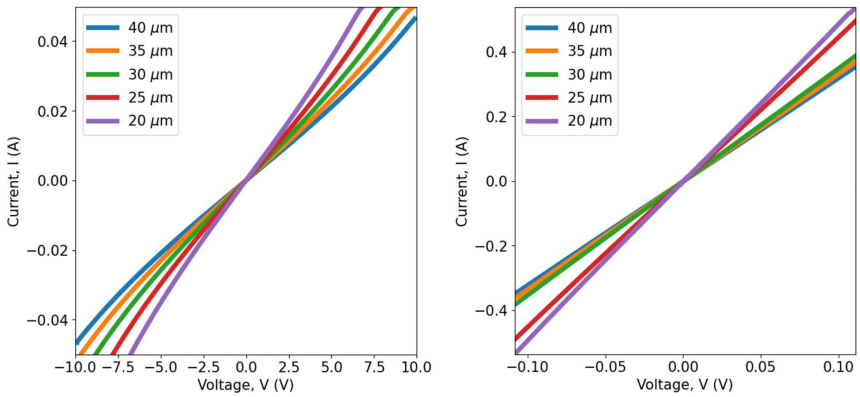

Fig. 6. Left: I-V characteristics of Ti/Al cTLMs for p-SiC anode annealed at 1000° for 5 min. in a N_2 environment. Right: I-V characteristics of Ti/Ni cTLMs for n-SiC cathode annealed at 1000° for 5 min. in a N_2 environment.

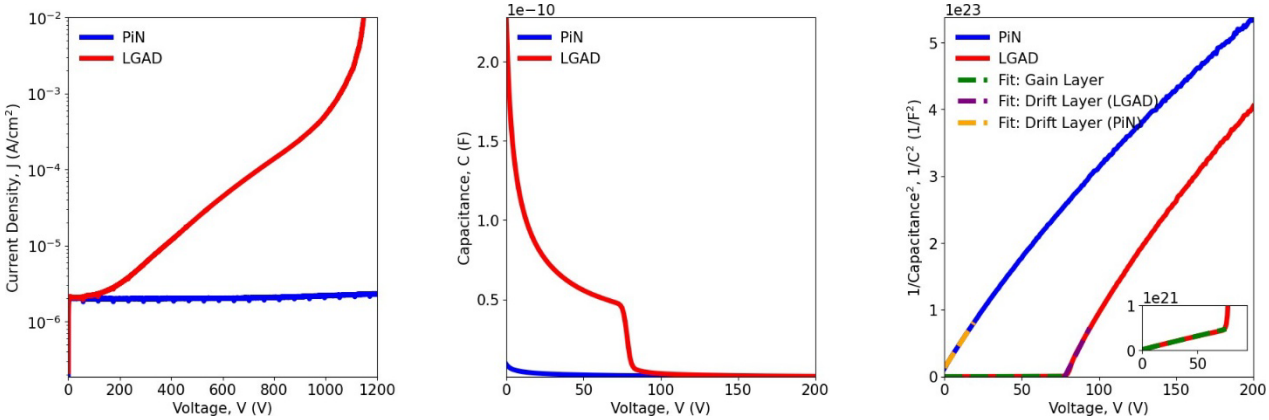

Fig. 7. Left: I-V characteristics of a 75 μm diameter 4H-SiC LGAD. Center: C-V and Right: Inverse C-V characteristics of a 600 μm diameter 4H-SiC LGAD. Figures adapted and modified from [5].

Circular transmission line measurement (cTLM) structures were fabricated on the n^{++} substrate and p^{++} contact layer to extract specific contact resistivity. The diameter of the inner circular pad of the cTLM is 185 μm and the spacing d between the adjacent contacts is 20μm, 25μm, 30μm, 35μm, and 40μm. The I-V characteristics of the cTLMs were measured using a Keithley 4200 semiconductor parameter analyzer. According to Fig. 6, the linear I-V curves indicate ohmic contact formation on the n^{++} substrate. The contacts on the p^{++} contact layer show a small Schottky barrier as seen by the slight non-linearity in the I-V curves in Fig. 6. For an LGAD that will be operating at high voltages between the full depletion voltage (voltage at which the entire device is depleted) and the breakdown voltage, this Schottky barrier does not pose any major issue. It should be noted that the I-V curves were approximated to be linear to calculate the specific contact resistivity for the p-type contact. Specific contact resistivities of 4.55×10^{-4} Ω-cm^2 and 8.64×10^{-7} Ω-cm^2 were calculated for the p- and n-type contacts, respectively.

Electrical Characterization

I-V and C-V characteristics of the devices were characterized using a Keithley 2657A high voltage SMU and Keithley 4200 semiconductor parameter analyzer, respectively. A breakdown voltage of 1160 V was measured in the LGAD. To fully deplete the gain and drift layers to ensure all electron- hole pairs generated by incoming MIPs are collected, this device must operate at a bias greater than 2 kV. The high depletion voltage required is due to the thick 75 μm drift region. The breakdown voltage can be increased by incorporating edge termination features in future studies.

The gain layer depletion voltage (V_{GL}) was measured to be 77 V as shown by the characteristic "step" feature in the C-V curve in Fig. 7. The doping levels of the gain and drift layers in the LGAD and PiN diode were calculated from the C-V data to be 2.84×10^{17} cm^{-3} (gain layer), 3.78×10^{14} cm^{-3} (LGAD drift layer), and 4.86×10^{14} cm^{-3} (PiN diode drift layer). Using an abrupt 1D diode model, the thickness of the gain layer was found to be 0.556 μm from the extracted V_{GL} and doping levels. The calculated doping levels and thicknesses are close to the target values.

Summary

Critical steps in a process flow for the fabrication of a 4H-SiC LGAD are discussed. The roughness pre- and post-RIE is shown to be similar through a comparison of AFM images. SEM confirms the etch depth, sidewall angle, and oxide thickness. The dark currents from two different passivation strategies are compared, with a thermal oxidation coupled with PECVD oxide demonstrating lower dark current which is beneficial to avoid breakdown during high voltage operation. The Ni and Al metal stacks form low resistivity contacts in n- and p-type 4H-SiC. Electrical characterization of the devices shows the ability to sustain high voltage as well as depletion of the gain layer to demonstrate low-gain charge carrier multiplication in the 4H-SiC LGAD structure. Radiation response testing using α particles corroborates the electrical characterization results on these same devices [5]. To test how 4H-SiC detectors withstand high radiation environments, electrical and α-particle irradiation response testing will be compared before and after exposure to high fluences of radiation. The use of ion implantation for JTEs and in place of epitaxial growth is being considered for future experiments.

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