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TDDB and HTGB Study of SiC MOSFET with Excessive Channel Leakage

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Keywords: Time-dependent dielectric breakdown (TDDB), high temperature gate bias stress (HTGB), channel leakage, subthreshold swing, positive bias temperature instability (PBTI), negative bias temperature instability (NBTI).

Abstract. We identify one type of outlier SiC MOSFET device from massive parametric test that shows excessive channel leakage and abnormal subthreshold swing ($S_{S\text{-}TH}$) at low V_G (<1 V) and low I_D (<100 nA). Time-dependent dielectric breakdown (TDDB) and high temperature gate bias stress (HTGB) tests have been performed on these outlier devices to check their reliability. TDDB lifetime is shorter for a device with a higher $S_{S\text{-}TH}$, but there is no indication that the $S_{S\text{-}TH}$ outliers would lead to an extrinsic failure. The post-PBTI I_D-V_G curve of the outlier device is overall shifted rightward and the off-state leakage at V_G=0 V is lower. The post-NBTI $S_{S\text{-}TH}$ is reduced at I_D<100 nA and the off-state leakage is almost unchanged.

Introduction

Silicon carbide (SiC) device market is achieving a compound annual growth rate of 26% driven specially by the rapid growth in the sales of electric vehicles [1]. Along with an accelerated expansion in production, SiC MOSFET manufacturing is still facing the issue of a relatively low yield compared to Si counterparts primarily due to defective substrate/epitaxy and a high interface trap density (D_{it}) at the gate oxide-SiC interface. A thorough device screening method after processing is essential for a manufacturer to deliver reliable chips especially for automotive applications [2]. In this paper, we identify one type of outlier MOSFET device that shows excessive channel leakage and abnormal subthreshold swing ($S_{S\text{-}TH}$) at low V_G (<1 V) and low I_D (<100 nA). Such devices are difficult to detect in large-volume parametric tests because low-current tests are normally omitted to maintain a high throughput. A reliability study on these outliers is necessary to determine whether they should be screened out. We perform TDDB and HTGB tests following JEDEC guidelines [3,4] on these outlier devices and compare the results to nominal ones. Pre- and post- stress DC test of individual device is shown to see the device degradation in threshold voltage (V_{TH}) and off-state leakage current.

Method

The device under test (DUT) in this paper are SiC MOSFET prototypes rated at 1.2 kV and encapsulated in TO-247 package. Room temperature DC characterizations, e.g. transfer I_D-V_G and off-state I_D-V_D, are tested by Keithley high power source measurement units (SMU).

TDDB Test (constant-voltage stress). The DUT is placed in a high temperature socket in a preheated oven. After loading the sample and the selected temperature is stabilized, a DC bias voltage supplied by Keithley SMU is applied on the DUT until the device fails abruptly (I_G reaching compliance). The time to failure is regarded as the TDDB lifetime of the device. A typical curve of I_G over time is shown in Fig. 1. TDDB test in this paper has two conditions: (1) 9 MV/cm (electrical field at gate oxide) at 25 ˚C and (2) 8.7 MV/cm at 175 ˚C.

HTGB Test. The test is accomplished by measure-stress-measure method (see Fig. 2) following the JEDEC guidelines to evaluate both positive (PBTI) and negative (NBTI) bias temperature instability. The electric field applied on the DUT is 5 MV/cm and -3 MV/cm for PBTI and NBTI respectively. The time interval of the bias stress is logarithmically increased. Threshold voltage (V_{TH}) of the DUT is extracted at I_D=10 mA from I_D-V_G sweep (V_G=V_D) tested in-situ between two intermediate stress biases. For PBTI, V_{TH} is tested by sweeping the voltage from high to low after positive conditioning while for NBTI it is inverted.

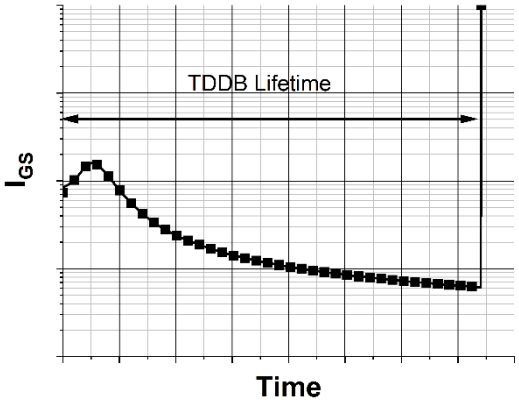

Fig. 1. A typical curve of gate leakage current (I_G) over time from a TDDB test.

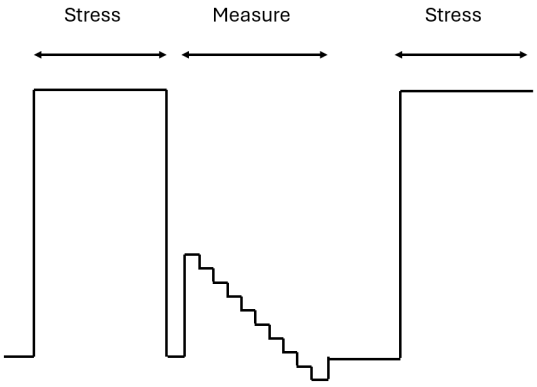

Fig. 2. Waveform of the HTGB voltage under measure-stress-measure method.

Results

The transfer I_D-V_G curve of a device with abnormal $S_{S\text{-}TH}$ is shown in Fig. 3 (red) together with a nominal one (black). The abnormal device has an excessive leakage current at low gate voltage (V_G<1 V) instead of having a constant subthreshold slope. This excessive leakage also affects the device at off-state at V_G=0 V, as shown in Fig. 4 (black solid). The outlier device shows two order of magnitude higher leakage current at V_D<800 V and V_G=0V. Note that this leakage current is caused by defects in the gate which is distinguishable from a leakage caused by defects in the drift region because it can be eliminated by a reverse gate bias as shown in Fig. 4 (red solid).

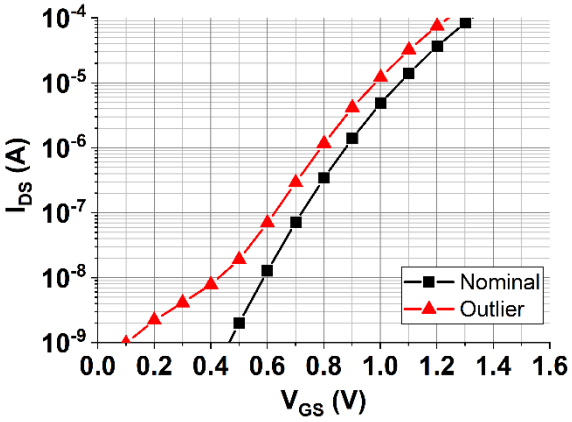

Fig. 3. Transfer I_D-V_G curves of a nominal device and a $S_{S\text{-}TH}$ outlier.

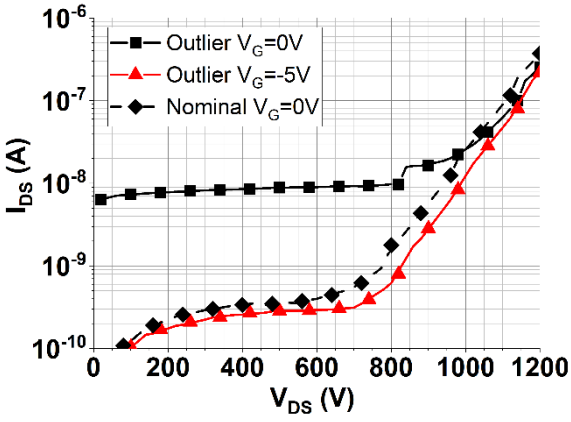

Fig. 4. Off-state I_D-V_D curves of a $S_{S\text{-}TH}$ outlier at V_G=0V/-5V and a nominal one at V_G=0V.

The subthreshold swing at I_D=10 nA~100 nA range is calculated by Eq. 1.

$$S_{S-TH} = \frac{V_G@I_D=100nA - V_G@I_D=10nA}{log_{10}(100nA) - log_{10}(10nA)} (mV/dec) \quad (1)$$

The nominal $S_{S\text{-}TH}$ value of our fabricated devices is 130 mV/dec. About 1.5% of the total number of our processed chips show much higher $S_{S\text{-}TH}$ (>200 mV/dec).

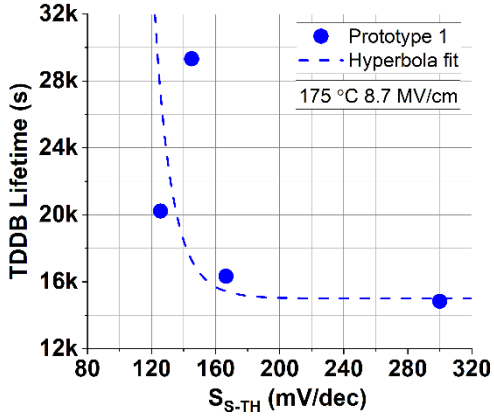

Fig. 5. TDDB (175˚C, 8.7 MV/cm) lifetime as a function of $S_{S\text{-}TH}$.

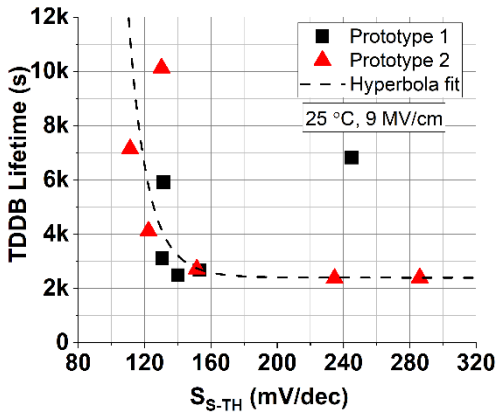

Fig. 6. TDDB (25˚C, 9MV/cm) lifetime as a function of $S_{S\text{-}TH}$.

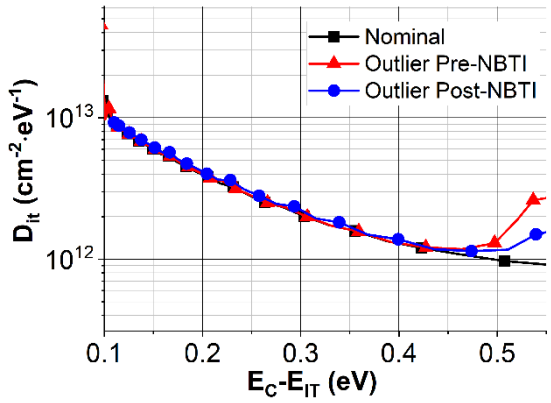

Fig. 7. D_{it} profile of the nominal device and the outlier device pre- and post-NBTI.

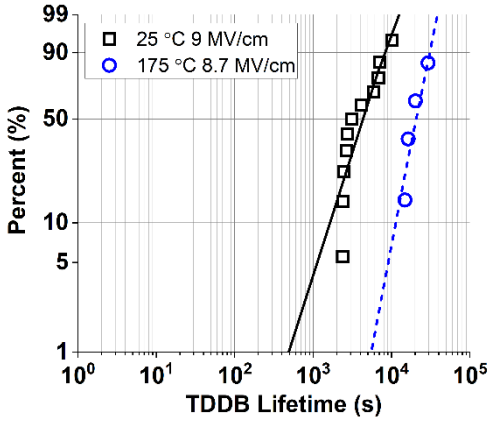

Fig. 8. Weibull plot of TDDB lifetime under two test conditions.

Devices with different values of $S_{S\text{-}TH}$ have been tested for TDDB. The TDDB lifetime is shorter for a device with a higher $S_{S\text{-}TH}$, as shown in Fig. 5 and Fig. 6 respectively, under both test conditions as described in Method. It is known that $S_{S\text{-}TH}$ is positively correlated with the D_{it} of SiC/oxide interface as described in Eq. 2 [5], where k is Boltzmann constant, T is temperature, q is electron charge, C_D is depletion capacitance, C_{OX} is oxide capacitance.

$$S_{S-th} = \frac{kT}{q} \cdot ln(10) \cdot (1 + \frac{C_D + q \cdot D_{it}}{C_{ox}}) \quad (2)$$

The extracted D_{it} profile of our devices is shown in Fig.7. The outlier device shows a higher D_{it} at high energy levels. There is no doubt that a higher D_{it} (in other word, a worse gate quality) leads to a shorter TDDB lifetime. However, the TDDB lifetime varies little for devices with either 20% or 130% higher $S_{S\text{-}TH}$ except only one outsider. The TDDB lifetime and $S_{S\text{-}TH}$ could be fitted by a hyperbola function (dash line in Fig. 5 and Fig. 6). Our interpretation is that higher $S_{S\text{-}TH}$ originates from the larger number of interface traps caused by material defects rather than processing defects. The former would have instant impact on TDDB lifetime. The Weibull plot of the TDDB lifetime of the two test conditions are shown in Fig. 8. All the TDDB failures should be classified as “intrinsic mode”.

Fig. 9 and Fig. 10 show the HTGB in-situ V_{TH} drift over time for PBTI and NBTI, respectively. ΔV_{TH} is only around 0.2 V and starts to remain stable from ~14 hours for PBTI whilst it is neglectable for NBTI for both types of devices. ΔV_{TH} of both NBTI and PBTI is well within the JEDEC qualification criterion (±20%). The little impact on V_{TH} by HTGB is as expected because V_{TH} is extracted at V_D=20mA and the D_{it} is similar for both nominal and outlier devices at low energy levels.

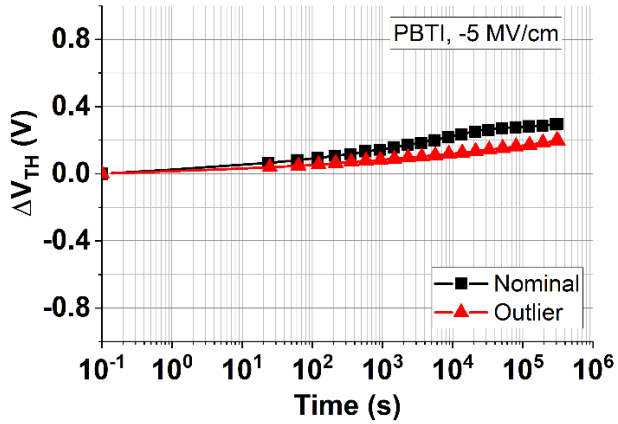

Fig. 9. In-situ V_{TH} drift over time of PBTI.

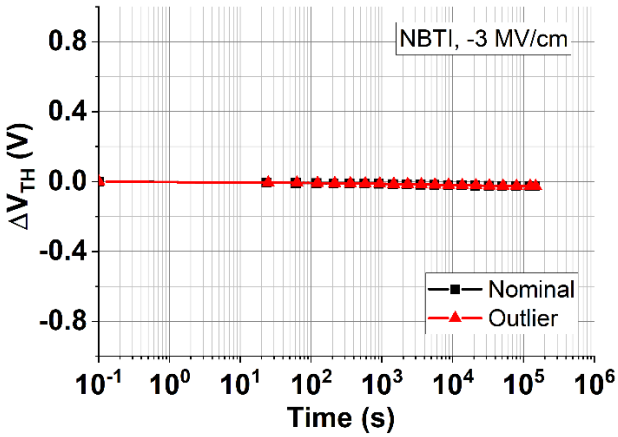

Fig. 10. In-situ V_{TH} drift over time of NBTI.

The pre-/post- HTGB I_D-V_G curve in the subthreshold region is shown in Fig. 11. The pre-/post-HTGB off-state leakage current at V_G=0 V and V_D=800 V is shown in Fig. 12. The post-PBTI I_D-V_G curve is overall shifted rightward and the off-state leakage at V_G=0 V is lower. On the other hand, the post-NBTI $S_{S\text{-}TH}$ is reduced at I_D<100 nA and the off-state leakage is almost unchanged. The reverse bias acted as a curing process that slightly improves the quality of MOS interface (see the post-NBTI D_{it} profile in Fig. 7, blue).

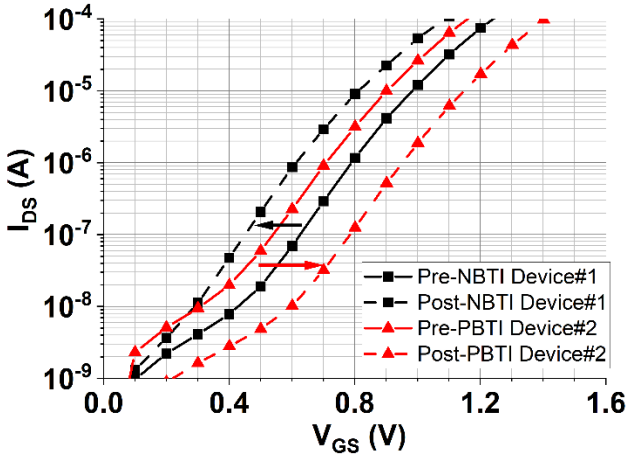

Fig. 11. Pre- and post- HTGB I_D-V_G curves of the $S_{S\text{-}TH}$ outliers.

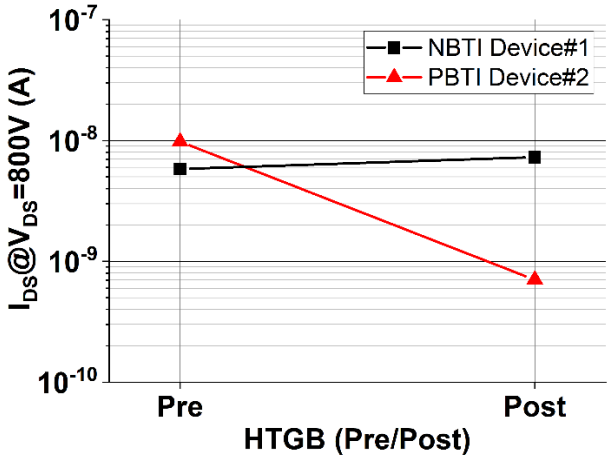

Fig. 12. Pre- and post- HTGB leakage current at V_D=800V and V_G=0V of the $S_{S\text{-}TH}$ outliers.

Summary

A high $S_{S\text{-}TH}$ value at low V_G is an indication of material defects that increase the interface trap density at high energy levels. The HTGB study shows that the devices with high $S_{S\text{-}TH}$ have a low risk in gate failure although a full 1000-hour stress is yet to be verified. There is no indication that the $S_{S\text{-}TH}$ outliers would generate extrinsic TDDB failures though a higher $S_{S\text{-}TH}$ value leads to a shorter TDDB lifetime. In case a high screening standard of TDDB lifetime is required, a critical (<1σ) upper specification limit of $S_{S\text{-}TH}$ should be introduced but this is not included in the JEDEC or AEC-Q101 standard [6] for automotive qualification.

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