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Peak Voltage and Switching Slope Dependency of Gate Switching Instability in SiC MOSFET

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Abstract. The pursuit of ever-higher system efficiency and power density in power electronic applications paves the way for an increased utilization of wide bandgap semiconductor devices such as silicon carbide (SiC) MOSFETs, due to reduced conduction and switching losses compared to silicon. For real-world application reliable operation along its lifetime is of utmost importance. To assure robust operation in electric drives and traction inverters SiC MOSFETs are switched bipolar to prevent parasitic turn on. Recently, it has been shown that not only bias temperature instability, but also gate-switching instability in bipolar switched applications has to be considered as a reliability concern for SiC MOSFET. While in gate switching stress tests usually only critically damped conditions are investigated irrespective of rise and fall times, in real-world applications gate voltage overshoots may occur and a broad variety of slew rates may be used depending on the individual power converter design. Therefore, this work investigates the influence of gate voltage overshoot and voltage slopes on threshold voltage aging using high frequencies and online degradation monitoring. It is shown that overshoots have a dominating impact on the overall degradation, while the gate voltage slope impacts minorly.

Introduction

Besides the ever-increasing demand for power density and high power efficiency, power electronic devices have to work reliably for twenty years, and more [1,2]. For this, several different lifetime tests were evaluated over recent years. Most lifetime tests were originally developed for Silicon devices and later on adapted for Silicon Carbide (SiC) devices. In this work, the focus is set on gate oxide reliability. Unlike Si devices, SiC devices have a more deficient gate oxide/semiconductor interface. Interface state densities of 10^{12} $eV^{-1}cm^{-2}$ are commonly achieved, about two orders of magnitude higher than for Si [3]. Residual carbon atoms near the interface can explain this elevated defect density. This challenging interface has multiple effects on the threshold voltage (V_{th}) characteristics. On the one hand, reversible trapping can be observed with a distinct difference whether a positive or negative gate-source voltage was applied beforehand [3]. Depending on the technology, this effect can include a change between 40 and 400 mV. Since this effect is fully reversible and is not impacted by aging, this effect is neglected for gate switching stress tests (GSS) [4]. On the other hand, significant degradation over the lifetime can be observed in two primary effects:

- Bias Temperature Instability (BTI), this effect can be explained by an accumulation of mobile oxide charges near the interface for longer stress durations [3,5]. This effect is commonly known in Si, but is more pronounced in SiC. BTI is testable with traditional high-temperature gate bias tests (HTGB), as this effect is highly temperature-dependent, and standards are already established [6].
- Gate Switching Instability (GSI) can be observed for bipolar switching from accumulation to strong inversion of SiC devices, a V_{th}-shift dependent on the number of switching cycles [7-13].

Unlike BTI, GSI is not dependent on the total test time, but on switching cycles. In recent years, further analysis on GSI has been done, and standards have been established [14]. Several different

influences such as temperature dependency, drain-source voltage (V_{ds}), positive and negative gate-source voltages (V_{gs+}, V_{gs-}), have been investigated [7-15]. It has been shown that the temperature has a negligible influence on GSI, indicating that known field-based tunneling effects like Fowler-Nordheim tunneling are not responsible for the observed degradation [14]. In [13], a recombination-enhanced defect model was developed explaining observed GSI by introducing a multi-step activation of defects, which have a small time constant and act charge-like in steady-state. In this work, a detailed analysis of GSI and its creation within one switching period is done. For this, experiments with different voltage slopes and overshoots have been carried out.

Method

In this work, a custom testbench for the characterization of gate-switching stress is used [4]. This testbench is capable of cycling up to twelve devices with different V_{gs+},V_{gs-} , junction temperature (T_j) , and swiching frequency (f_{sw}) of up to 10 MHz while monitoring in-situ V_{th} and $R_{ds,on}$ degradation. A distinguish measurement of $V_{th,up}$ and $V_{th,down}$ is done as specified by JEDEC JEP 184 [6]. Furthermore, variable external gate-resistance R_g can be used to adjust the gate voltage slew-rate. To further analyze the impact of voltage slope and gate overshoot on gate switching instability, we first consider the waveforms under switching operation. For this, the gate path is modelled as a simple RLC-circuit in which R_g is the total gate resistance, including the internal and external gate resistance ($R_{g,ext}$) as well as the driver resistance. Furthermore, the C consists of the input capacitance (C_{iss}) of the device under test and additional parasitics of the measurement board, and L_g is the parasitic gate-loop inductance. In this work, L_g is 25 nH from the parasitics of the testbench layout, and C_{iss} is approximately 1 nF for two different planar SiC MOSFET technologies with a comparable 63 mΩ, 1200 V planar SiC MOSFET. For the following considerations, we define a damping factor ζ as in Eq. 1:

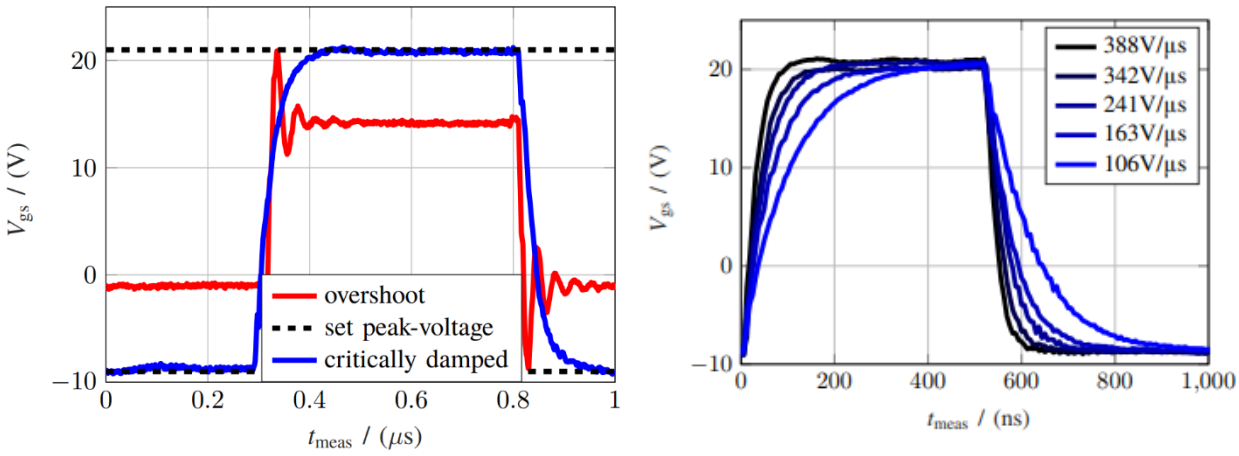
$$\zeta = \frac{R_g}{2} \cdot \sqrt{\frac{C_{iss}}{L_g}} \tag{1}$$

Only $R_{g,ext}$ can be changed in a practical matter to adapt ζ. To test the influence of voltage overshoot on gate-switching instability, several different V_{gs-} and V_{gs+} with matched peak voltages (V_{peak}) are used. These can be calculated with Eq. 2 and 3 for $\zeta < 1$, in which ΔV_{gs} is the total gate voltage difference between V_{gs+} and V_{gs-}.

$$V_{peak+} = V_{gs+} + \Delta V_{gs} \cdot (1 + e^{-\frac{\pi \cdot \zeta}{\sqrt{1-\zeta^2}}}) \tag{2}$$

$$V_{peak-} = V_{gs-} - \Delta V_{gs} \cdot (1 + e^{-\frac{\pi \cdot \zeta}{\sqrt{1-\zeta^2}}}) \tag{3}$$

The required ζ value is 0.544 and 0.236 for 18/−5 V and 14/−1 V, respectively. This is reached by changing the external gate resistor $R_{g,ext}$ to 4 Ω and 0 Ω, respectively. It should be noted that the external gate driver has a finite resistance, which adds to the gate path and is not equal for charging and discharging, hence a higher damping is reached during turn-on compared to turn-off. The waveform for an underdamped system of 14/−1 V and critically damped 21/−9 V is depicted in Figure 1a. It can be seen that the peak voltages are identical, while the steady-state voltages differ. To test the influence of the gate-voltage slew rate on GSI, different gate resistors were used under the constraint that both critical damping conditions are fulfilled and the maximum voltage is reached within 0.5 % at the end of the switching period. To achieve a high acceleration factor 1 MHz was chosen and the maximum $R_{g,ext}$ of 60 Ω was used yielding a ζ of 1.6. The waveforms for these critically damped conditions with voltage slopes ranging from 100 to 400 V/µs is depicted in Fig. 1b.



(a) Waveforms for critically damped V_{gs} of 21/-9 V and underdamped 14/−1 V at 1 MHz.

(b) Critically damped waveforms for V_{gs} of 21/-9 V for different R_g at 1 MHz.

Fig. 1. Measured GSS waveforms of underdamped (a) and different critically damped (b) conditions.

Results and Discussion

Frequency-Dependency.

In this section, the GSI-dependency of a planar 75 mΩ 1200 V SiC MOSFET from manufacturer B on f_{sw} is investigated. For this, all devices are critically damped with 10 Ω and are stressed with V_{gs} of 18/-9 V. The measurement is done with a preconditioning pulse of 10 ms at the same voltage as the stress voltage and with 10 mA of measurement current under shorted gate-drain conditions. f_{sw} is chosen as 5, 50, 500, 2500 kHz to cover a large range of application-close, and highly accelerated lifetimes. $V_{th,up}$ and $V_{th,down}$ are measured ten times per decade since no degradation of hysteresis is observed; only $V_{th,up}$ is depicted in Fig. 2a. It can be seen that very similar aging can be observed over cycles for all frequencies, hence suggesting that the observed failure mechanism is not time-dependent, but rather cycle-dependent.

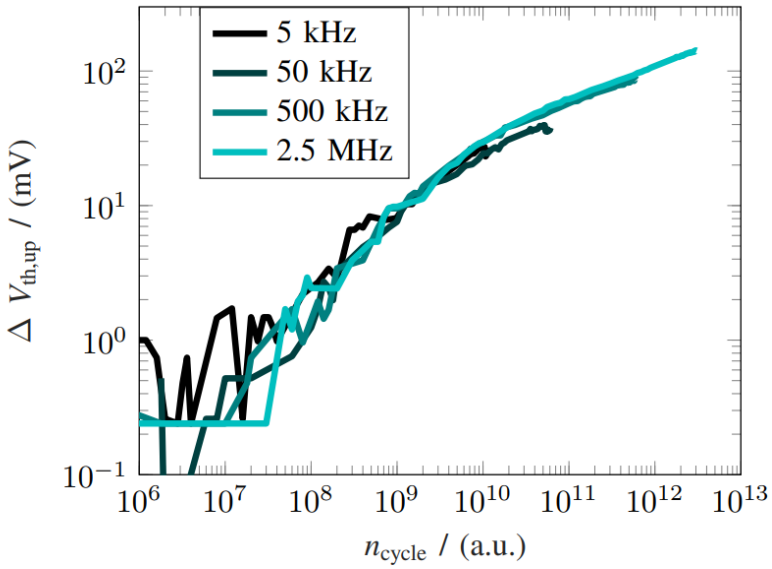
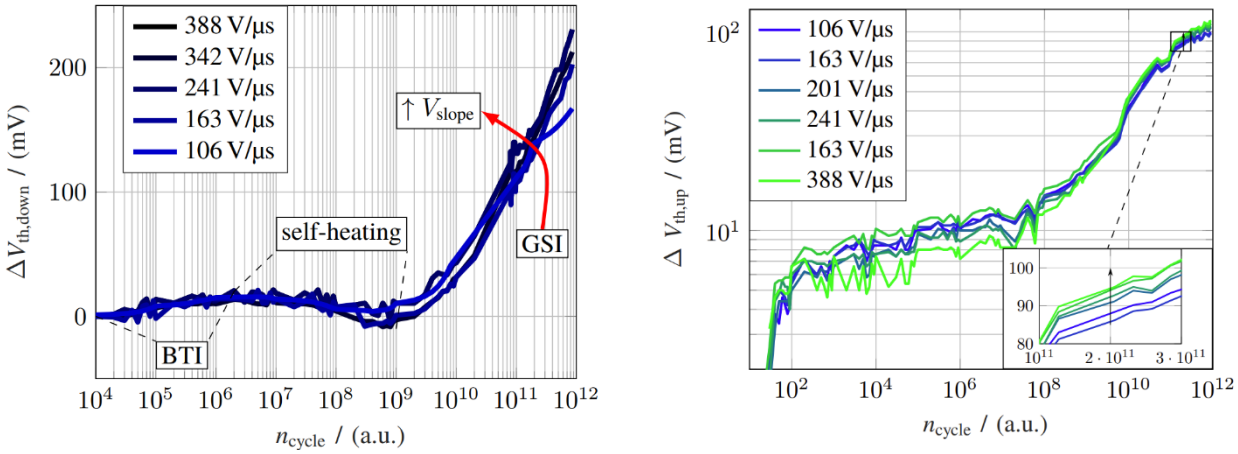


Fig. 2. Frequency-dependent GSI at V_{gs} of 18/-9 V and gate voltage slew-rate of 388 V/µs with a 1200 V 75 mΩ SiC MOSFET of manufacturer A.

Voltage-slope Dependency.

In this section, the influence of different voltage slopes is investigated. For this, the waveforms depicted in Fig. 1b are utilized for two different planar technologies with a stress frequency of 1 MHz. The results for this are depicted in Fig. 3a for manufacturer B and Fig. 3b for a 63 m Ω 1200 V planar SiC MOSFET of manufacturer A with the same measurement method as ascribed before. For both technologies, no aging in the hysteresis was observed; hence, only one is depicted. After an initial increase of roughly 20 mV, which can be explained by BTI. $V_{th,down}$ decreases until 10^9 cycles; this can be explained by the self-heating of the devices since V_{th} has a negative temperature coefficient. This effect is larger for high voltage slope DUTs since a larger share of the capacitive losses are dissipated in the DUT. For the second experiment, the cooldown time was increased, and the devices were measured at room temperature. Therefore, no self-heating is observed. However, the room temperature altered during the GSS-operating conditions, hence some additional dips are observed in Fig. 2b, especially at higher n_{cycles}. For both manufacturers, the trend is identical: for higher voltage slew rates, the GSI degradation increases as the voltage slope increases. This can be explained with an energy barrier that has to be overcome to activate the GSI- related defects. For higher switching speeds, higher energies are reached, therefore increasing the possibility of an activation over this recombination-enhanced reaction [11]. However, this effect is not dominating, and similar aging is observed for all devices under test and slew rates.



(a) V_{gs}-slope-dependency of manufacturer B at V_{gs} of 21/-9 V.

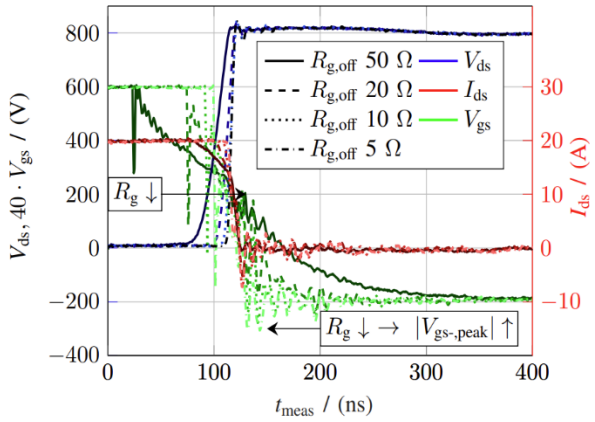
(b) V_{gs} -slope-dependency of manufacturer A at V_{gs} of 18/-9 V.

Fig. 3. Measured GSS stress degradation for two different manufacturers at f_{sw}=1 MHz.

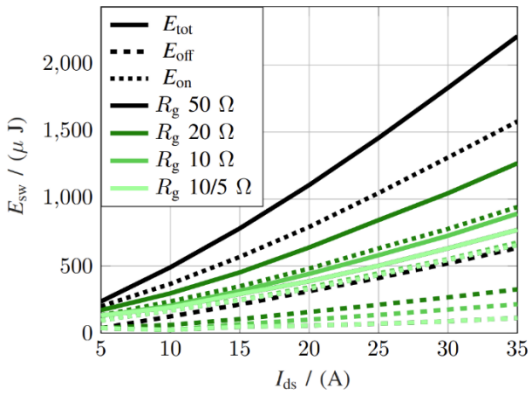
Peak-Voltage Dependency.

In this section, the influence of the peak gate voltage is discussed. The waveforms were discussed in detail in the previous section. The peak-voltage dependency is important since in switching transition, short-timed gate-voltage overshoots and especially undershoots may occur. This is especially the case if low R_g are utilized to reduce the overall switching losses. To show the influence of R_g, and the drain-source current (I_{ds}) on $V_{gs\text{-},peak}$ a custom double pulse test bench is used. A 75 mΩ 1200 V SiC MOSFET from manufacturer B is characterized for different I_{ds}, R_g and $V_{gs\text{-}}$ at 800 V and V_{gs+} of 15 V. For this, a commercial coaxial shunt with a high bandwidth up to 1 GHz for the current measurement and an isolated voltage probe with a bandwidth of 1 GHz for V_{gs} measurement is used [17]. In Figure 4a the turn-off transition at 800 V V_{ds}, 20 A I_{ds}, and 15 V V_{gs+} is shown for different turn-off gate resistances ($R_{g,off}$) it can be seen that the transition time reduces significantly and hence the switching energy (Esw) gets significantly lower as depicted separately in Fig. 4b. While for 50, and 20 Ω $R_{g,off}$ critically damped conditions are fulfilled, significant overshoots may occur at lower

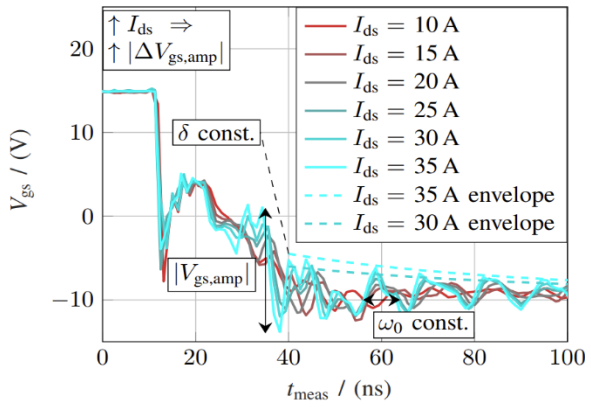
$R_{g,off}$ reaching V_{gs} peak values ($V_{gs\text{-},peak}$) of up to -14 V. Besides a dependency on R_g, which is an initial design choice. A dependency of I_{ds} can also be extracted; this is depicted in Fig. 4c.



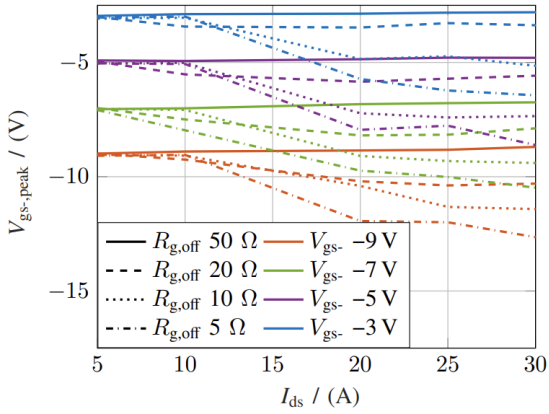
(a) Turn-off transition for different $R_{g,off}$ at V_{ds}=800 V, and I_{ds}= 20 A.



(b) Switching Energies for V_{gs} = 15/-5 V, and V_{ds} = 800 V



(c) Turn-off transition for $R_{g,off}$ = 5 Ω, at V_{ds} = 800 V, and V_{gs}= 15/-9 V.



(c) Negative peak voltage $V_{gs\text{-},peak}$ of different $R_{g,off}$, and I_{ds} at V_{ds} = 800 V, and V_{gs+} = 15 V.

Fig. 4. Double pulse tests for a 1200 V, 75 mΩ SiC MOSFET of manufacturer B for different $V_{gs\text{-}}$, $R_{g,off}$, and I_{ds}.

Here, $R_{g,off}$ of 5 Ω, V_{ds} of 800 V, and V_{gs} of 15/-9 V are used. It can be seen that the initial V_{gs} waveform looks identical until 25 ns after which a ringing effect arises. This ringing effect can be described by Eq. 4 in which $V_{gs,amp}$ is the current dependent ringing amplitude, ω_0 is the resonance frequency of the gate loop, consisting of L_g and the input capacitance (C_{iss}) ascribed in Eq. 5 and δ is the damping factor calculated with Eq. 6, in which $R_{g,int}$ is the internal gate resistance and $R_{g,ext}$ the external gate resistance [18,19]. Furthermore, $V_{gs,ideal}$ is the ideal discharge curve without any ringing. In this work, a TO-247-4 adapter is used to reach a L_g of 25nH comparable to the GSS measurements, which have similar parasitics. Therefore, the ringing phenomena is larger than in typical applications, however, if L_g is reduced, similar behaviour is observed for lower R_g.

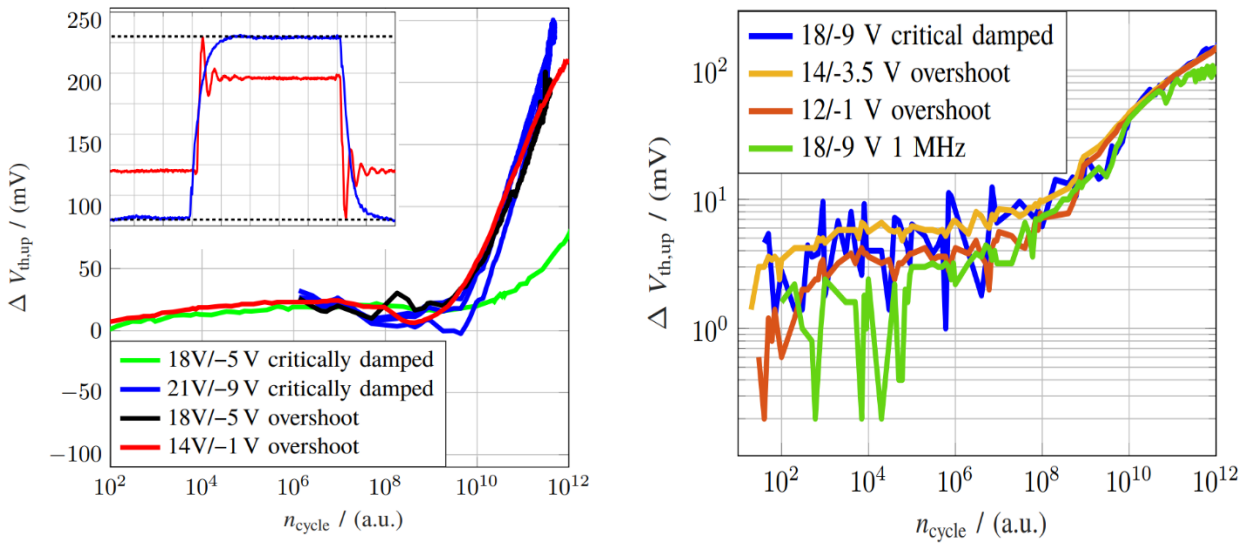
$$V_{gs}(t) = V_{gs,amp}(I_{ds}) \cdot \frac{\omega_0}{\sqrt{\omega_0^2-\delta^2}} \cdot e^{-\delta t} \cdot \cos(\sqrt{\omega_0^2 - \delta^2} \cdot t - \varphi) - V_{gs,ideal}(t) \quad (4)$$

$$\omega_0 = \frac{1}{\sqrt{L_g \cdot C_{iss}}} \quad (5)$$

$$\delta = \frac{(R_{g,int}+R_{g,ext})}{2\cdot(L_{par,g})} \quad (6)$$

In Fig. 4c, it can be seen that irrespective of I_{ds}, ω_0 and δ remain unchanged, but there is a distinct influence on $V_{gs,amp}$, hence higher I_{ds} increase $|V_{gs,peak-}|$. In Fig. 4d, solely $|V_{gs,peak-}|$ is depicted for different $R_{g,off}$, and I_{ds} in a first approximation, a square-root relationship can be observed for underdamped systems, as in $R_{g,off}$ of 5, and 10 Ω.

In the following, the influence of these observable overshoots in the nanosecond range should be investigated. For this, the identical GSS measurement method is used compared to the prior section. 5 MHz was used as stress frequency unless stated otherwise, with the underdamped waveforms depicted in Fig.1a. In Fig. 5a, the aging curve of $V_{th,down}$ over switching cycles for manufacturer B, is shown. Until 10^6 cycles, an increase in V_{th} can be observed due to BTI or some sort of charging effect. A slightly lower charging effect is observed for 18/−5 V as compared to 14/−1 V owing to the lower average voltage present [17]. It seems that there is a saturation of this charging effect for higher n_{cycle} than 10^6, for 14/-1 some additional self-heating related can be observed, due to insufficient cooldown time. For all samples with a peak voltage of 21/−9 V a sharp increase in V_{th} with an onset at 10^9 cycles due to GSI can be observed. In contrast, critically damped 18/−5 V onset of this GSI degradation increase is much later with an initially at $3\cdot 10^{11}$ cycles. This agrees with the literature that higher absolute V_{gs-} yield higher GSS- aging [13,17]. For this technology, it appears that the aging is irrespective of the set voltage, but rather on the peak voltage, even if the peak voltage lasts only a few nanoseconds. For comparison, a second planar technology from manufacturer A is investigated in Fig. 5b. Here, 18 V is chosen as peak voltage, and the voltage levels are set to 14/-3.5 V and 12/-1 V, respectively. To avoid the initial charging effect observed in Fig. 4a, the preconditioning voltage prior to each V_{th} measurement was set to 18/-9 V [17]. The stress frequency is 5 MHz for all devices except the green one, which is critically damped at the same voltage slew rate, but stressed with only 1 MHz. For this technology, similar aging for all overshoots or critically damped conditions is observed until 10^{12} cycles. The only observable difference is that if a lower frequency is utilized, some saturation in the GSI-related V_{th} can be seen after 10^{11} cycles. This indicates that the detrapping of GSI-related defects might be a function of the applied stress time, rather than the pure cycles. However, a clear conclusion regarding the detrapping of GSI-related defects is not possible from this measurement.



(a) Peak-voltage-dependency of manufacturer A.

(b) Peak-voltage-dependency of manufacturer B.

Fig. 5. Measured gate switching stress degradation for two different manufacturers at V_{gs} of 21/-9 V and f_{sw} of 1 MHz.

These findings suggest that the origin of GSI is mainly observed during the switching event, and it depends rather on the peak voltage than the respective time it requires to get to the individual peak voltages, since a few-nanoseconds transition time is already sufficient to create GSI related defects. This concludes that the time-constants related to GSI-defect generation have small time constants, and even undervoltage peaks as short as 4 ns are sufficient to dominate the observed GSI behavior. Since GSI-related aging is mostly related to V_{gs-} and hence $V_{gs-,peak}$, low $L_{par,g}$ has to be pursued to achieve low switching energy, while reducing the influence of GSI-related trapping [13,17].

Conclusion

In this work, the influence of frequency, gate voltage slope, and gate voltage overshoot on GSI was investigated. It has been shown that the switching frequency has no impact on GSI, while higher gate voltage slopes, and therefore lower rise and fall times, expose a slightly larger GSI degradation compared to slower switching transition. Additionally, the peak voltage was investigated, as it has a dominant impact on device degradation. The results show that matched undamped peak voltages and critically damped waveforms lead to nearly identical degradation levels. This suggests that the switching transition- and specifically the associated negative gate voltage - drives GSI with a time constant so short that, in practical applications, voltage undershoots must be considered in order to accurately approximate GSI-related V_{th} degradation. Consequently, minimizing the gate inductance should be a design priority. At the same time, a careful balance must be struck between reducing turn-off losses and limiting gate-voltage undershoot.

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