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Power Cycle Failure Modes of 10 kV SiC-MOSFET Power Modules with Different Wire Bond Layouts

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Abstract. 10 kV SiC-MOSFET power modules are being developed for medium-voltage applications, but their reliability has not yet been fully verified. This study demonstrates the power cycle test (PCT) on 10 kV SiC-MOSFET power modules with different wire bond layout designs to investigate the influence on their failure points. The 10 kV SiC-MOSFET is 8.1 mm square in size and 20 A/die. Only four source wire bonds are needed, which provides enough flexibility for the wire bond layout. The wire bonds are placed on the edge of each source pad to reduce the wire heating ΔT_{wire} by 6.2% compared to the conventional central wire bond placement from the 3D simulation. These differences were verified in the PCT on ΔT_{diemax} : $104-108\,^{o}$C. As a result, it was observed that samples with the modified layout, which achieved a lower ΔT_{wire}, exhibited a shift in failure mode from wire lift-off to solder failure, while maintaining a similar lifetime under higher die temperatures.

Introduction

The 10 kV silicon carbide metal-oxide-semiconductor field effect transistors (SiC-MOSFETs) have the potential for the next generation power electronics due to their superior performance at medium-voltage applications more than 6.5 kV [1]. To operate in this voltage range, 10 kV SiC-MOSFET dies have a larger edge area than lower voltage ones. This edge structure mitigates the concentration of electric fields at the edge of the die. Previous research [2] shows that the wide edge area of 10 kV SiC-MOSFETs makes the temperature gradient greater from the hot spot in the center of the die to the edge. Fig. 1 compares the die model of the 10 kV SiC MOSFET (Wolfspeed, samples under development) with a modelled 1.2 kV SiC-MOSFET, both having the same die size. The 1.2kV SiC-MOSFET is a hypothetical die with the same edge width and die thickness as the commercial product [20]. An optical microscope and micrometer measured the edge lengths and die thickness. The edge area ratio is the percentage of the edge region relative to all die surface area. Comparison of die surface temperature as line profiles using 3D finite element method (FEM) in [2] is also shown.

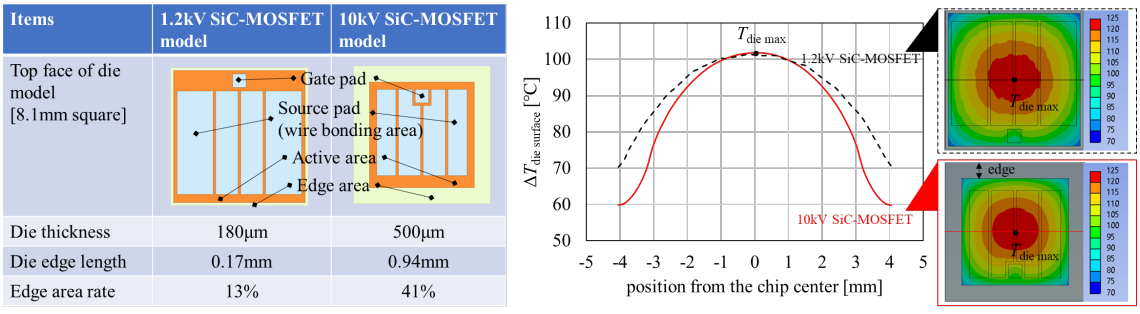


Fig. 1: Die structural comparison and the die surface temperature profile [2].

The edge area ratio of a 10 kV SiC MOSFET is greater than that of a 1.2 kV SiC-MOSFET. Temperature simulations show that the $\Delta T_{diesurface}$ at the die edge is about 10 ^{o}C larger for the 10 kV SiC-MOSFETs. In addition, a 10 kV SiC-MOSFET has a relatively large on-resistance, such as 340 mΩ [6, 7], with a small current rating, 20 A/die at room temperature. Due to their low current rating,

the number of source wires on the 10 kV SiC-MOSFETs is reduced. It has been reported that wire bond heating can be suppressed by optimizing the wire bond configuration on the die surface [8]. Thus, it will be a valuable design indicator if the structural weak points of the 10 kV SiC-MOSFET power module are the wire bond connections. A major approach to reliability investigation is the power cycle (PC) curve-based investigation [15]. This allows for their lifetime prediction. The main failure modes in power cycle test (PCT) are wire bond lift-off and solder failure in conventional Si and SiC devices [13, 14]. However, no investigation has been performed on the impact of 10 kV SiC-MOSFET thermal performance on PC failure points. Therefore, evaluating the dominating failure mode on 10 kV SiC-MOSFETs is the first step. The evaluation of failure points using PC curves requires a large number of samples, which is challenging for 10 kV SiC-MOSFETs because it is currently difficult to obtain sufficient samples. They are currently under development, and only a few engineering samples are available. Power module designers who do not manufacture devices in-house cannot access sufficient samples to evaluate reliability using the conventional PC curve method. This problem will be faced when developing all new innovative samples, not only 10 kV SiC-MOSFETs. Digital design using 3D modeling effectively solves this situation, especially in the early design phase when sufficient samples are unavailable [16]. The 3D temperature simulation suggests that improving the wire bond layout on the 10 kV SiC-MOSFET can suppress the wire heating temperature [3]. Since no PCTs have been performed on 10 kV SiC-MOSFET power modules, the literature has not yet discussed the influence of wire layout design on wire heating and its impact on reliability.

This study demonstrates the wire bond layout design of 10 kV SiC-MOSFET power modules based on 3D FEM temperature simulations as an initial investigation with minimal physical prototypes. 3D FEM calculates the wire bond temperature, and the layout that can suppress the wire bond temperature swing is investigated. Thus, the validity of these digital designs is demonstrated by evaluating the actual PCTs with physical prototypes of 10 kV SiC-MOSFET power modules that have two designs (conventional and modified).

Temperature Modeling of 10 kV SiC-MOSFET with Different Wire Bond Layouts

The wire bond layouts with reduced wire heating were designed using a 3D temperature simulation of a 10 kV SiC-MOSFET power module model. In this research, half-bridge power modules with 10 kV SiC-MOSFETs were manufactured [5]. This is the same as the module used in Fig. 1. A 3D model

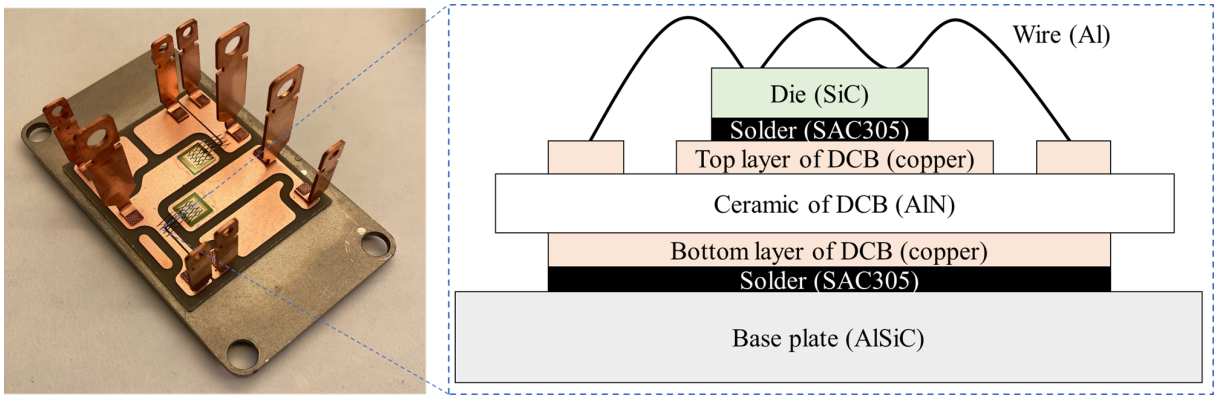


Fig. 2: 10 kV SiC-MOSFET power module structures in this research

with the same structure as this module was created, and a temperature simulation was performed using ANSYS Mechanical. In this modeling, the SiC-MOSFET die is 4H-SiC only for simplicity, and the metalization layer is not considered. Other structures and physical properties were reused from those shown in [2]. For simulation, this module model was fixed on a 10 mm-thick aluminum heat sink, and the bottom temperature of the heat sink was kept $T_0 = 70\ ^o$C as a boundary condition. The turn-on pulse width t_W was 5 seconds. The die surface maximum temperature was heated to $T_{diemax} = 175$

^{o}C by applying the power P_W. Two wire bond layouts on the 10 kV SiC-MOSFETs were prepared: a conventional layout (typical wire bonding at the center of each source pad) and a modified layout (wire placement at the edge of each source pad, which is a lower temperature place). Fig. 3 shows the respective wire bond layouts, sample photographs, and the simulated temperature of the interface between wire bonds and the die, maximum wire bond heating temperatures $\Delta T_{wiremax}$.

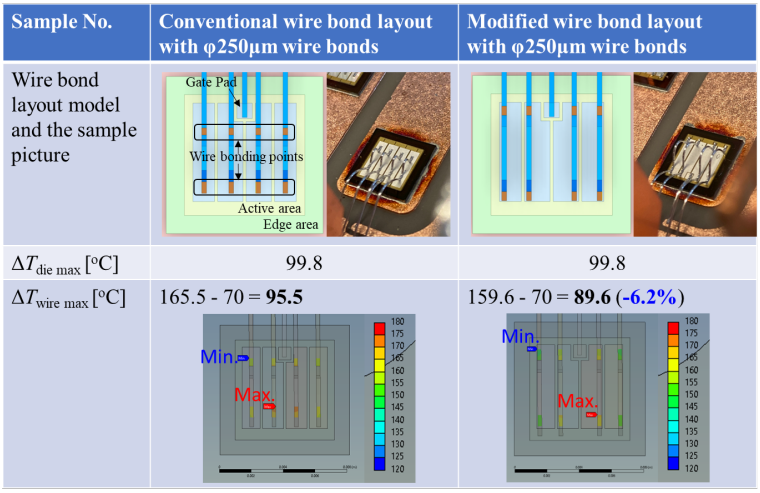


Fig. 3: Two different wire bond layouts and their temperature simulation results.

The simulation results showed that the modified wire bond layout has 6.2 % lower $\Delta T_{wiremax}$ than the conventional one. This is because the center of the die, where the surface temperature is higher, is physically avoided as a wire bond location.

Actual PCT Evaluation

Test setup and conditions. As an evaluation of their reliability performance, actual PCTs are used to confirm the influence of the wire bond layout in Fig. 3. The test setup photograph and its circuit diagram are shown in Fig. 4.

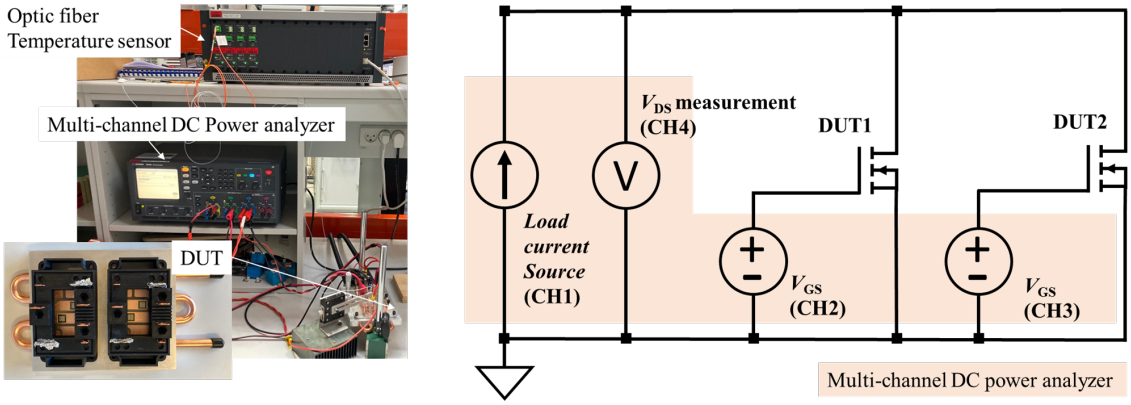


Fig. 4: Power cycle test setup and a circuit diagram.

These power module samples were mounted on an aluminum heat sink and kept at a constant temperature throughout the test with liquid cooling using Julabo 1000F. The temperature of the heat sink was T_h = 60 or 70 ^{o}C to reach the target maximum temperature. Although the resulting die temperature slightly varied among samples, the number of cycles to failure N_f is considered to be predominantly governed by the temperature swing within this experimental range, as is often the case in PCTs. The target maximum die surface temperature was T_{diemax} = 175 ^{o}C. This T_{diemax} was

Table 1: All sample PCT results

Sample No.	Wire bond layout	T_{diemax} [^{o}C]	ΔT_{diemax} [^{o}C]	N_f [cycles]	Failure mode
A	Conventional	176.2	104.2	32757	Wire bond lift-off
B	Conventional	185.4	113.4	19998	Wire bond lift-off
C	Conventional	157.0	95.0	67975	Solder failure
D	Modified	180.0	108.0	32002	Solder failure
E	Modified	175.8	113.8	38024	Solder failure
F	Modified	173.7	111.7	24212	Solder failure

measured using the fiber optic sensor from Opsens Solutions Coresens [4] to match the simulated physical temperature. A multichannel DC power analyzer, Keysight N6705C DC, supplied the gate and central power, which are V_{GS}=17.5 V and I_D=15 A. Two samples were tested simultaneously and alternately switched. That is, when one device was turned on, the other device was turned off. This test circuit supplies constant DC from the power supply by alternating between the samples under test. When the first sample broke, it was replaced by another sample, and the test continued. The on and off times were 5 seconds each. The power module's on-voltage, as the drain-source voltage $V_{DS(on)}$, was monitored using the same equipment. A sample failure criterion is usually established for measuring the N_f, defining failure as an increase in the $V_{DS(on)}$ of 5% relative to the initial value.

Lifetime measurement results. Fig. 5 shows the monitoring results of $V_{DS(on)}$ measured during the PCTs. All PCT results are summarized in the Table. 1 showing the N_f values and observed failure modes.

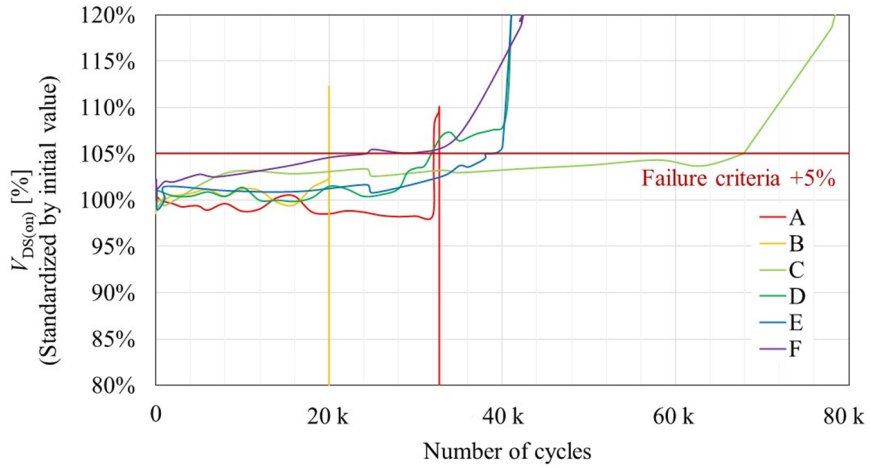


Fig. 5: $V_{DS(on)}$ monitoring results for all samples during PCTs.

As shown in the Table. 1, all samples have different T_{diemax}, which is thought to be due to variations in the on-resistance of each die. In Sample A and B with conventional layouts, a sharp drop in on-voltage was observed after the rapid increase in Fig. 5. This is expected because the wire cracks spread to the wire bond-die interface and deteriorated the electrical connectivity, resulting in a temporary increase $V_{DS(on)}$. This was followed by a complete wire bond lift-off from the die surface, resulting in a disconnection state and a sudden drop in the measured on-state voltage. The $V_{DS(on)}$ value of Sample C-F reached the failure criteria. From these results, the N_f was calculated. Next, to confirm the cause of the changes in $V_{DS(on)}$, various evaluations of each sample before and after PCT were performed.

Failure mode analysis. The failure mode of all six samples in Table. 1 was verified. The $I_D - V_{DS}$ characteristics of the MOSFETs as electrical characteristics are compared before and after the PCT using a curve tracer. In addition, the transient thermal impedance $Z_{th(diemax-h)}$ was calculated from

the die surface temperature measurement to compare a Sample D after PCT and a reference 10 kV SiC-MOSFET power module that has not undergone any PCTs. The measurement setup used the same setup as in Fig. 4 and an optical fiber. The $Z_{th(diemax-h)}$ was calculated by the equation;

$$Z_{th(diemax-h)} = (T_{diemax} - T_h) \div (V_{DS} \times I_D) \quad (1)$$

Constant DC was applied to these two modules for 5 seconds under the same conditions as the PCT. Baseplate temperatures were also kept 70 ^{o}C by a water-cooled aluminum heat sink. Fig. 6 shows the $I_D - V_{DS}$ characteristics of the MOSFETs before and after the PCTs and the transient thermal impedance measurements results on Sample D.

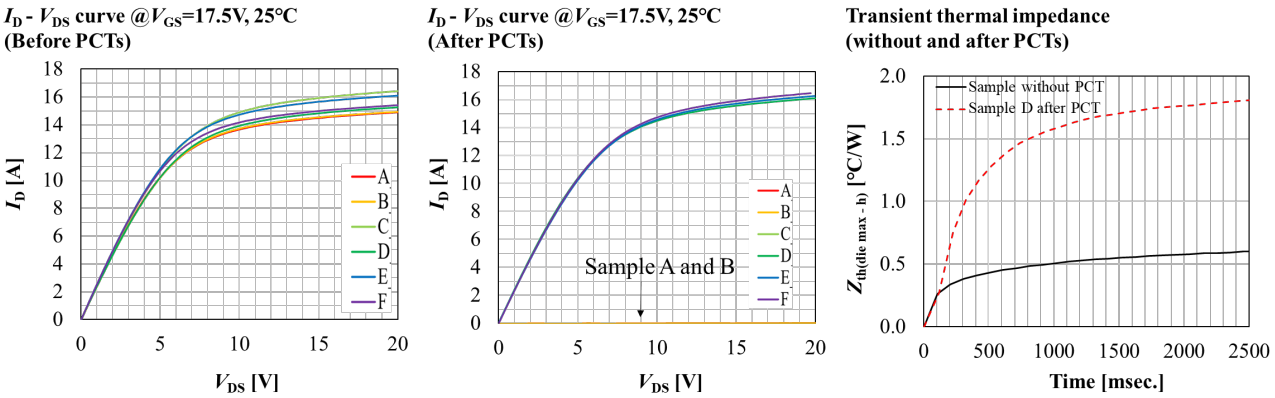


Fig. 6: Sample evaluation before and after PCTs; $I_D - V_{DS}$, and Thermal impedance.

Samples A and B did not show any difference between the drain-source, even though the gate voltage was applied. This suggests that the circuit between the gate-source is non-destructive, while the circuit between the drain-source may have been broken. This will be confirmed later by the microscopic observation of the failure points in the sample. Sample C-F showed no changes in I-V characteristics after PCTs. This could be due to increased thermal resistance without changing the module's package resistance, which could have caused the sharp rise in on-voltage seen in Fig. 5. Such an increase in on-voltage due to an enlargement in thermal resistance is known to be caused by the degradation of the solder layer under the die [17]. Sample D after the PCT increases $Z_{th(diemax-h)}$ after 100 ms compared with the reference sample. At 2,000 ms (2 seconds), the thermal resistance of Sample D is more than three times that of the reference. The results show that the rise in on-voltage on Sample D, as seen in Fig. 5, is due to higher T_{diemax} with increasing thermal resistance. As a direct comparison, the differences in failure points were observed in Sample A and Sample D. They are similar T_{diemax} and ΔT_{diemax}, may indicate different failure modes. Those hypotheses were verified by direct observation using an optical microscope. Each of the failure points is shown in Fig. 7.

It was also observed that the failure points changed from wire bond lift-off in Sample A to solder degradation (cracking) in Sample D. In Sample A, wire bonds and the die surface were disconnected during the PCT, resulting in a lost measurement signal, as seen in Fig. 5. In Sample D, the PCT did not noticeably change the internal connection caused by the wire bond failure, but the thermal resistance increased due to the solder failure. Fig. 5 shows the rapid increase in on-voltage caused by the rising die temperatures during the PCT. The N_f of Sample A was 32,757 cycles, and Sample D was 32,002 cycles. The change in the wire bond layout on Sample D showed a similar N_f with different failure modes.

Discussion

The results are summarized in Fig. 8 as the PC curve with N_f and ΔT_{diemax}. Their wire bond layouts and failure modes differentiated each plot.

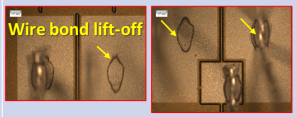
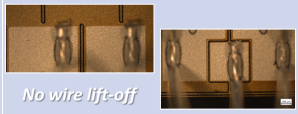
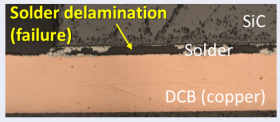
Items	Sample A (Conventional wire bond layout)	Sample D (Modified wire bond layout)
T_{diemax}, $\Delta T_{die\ max}$	176.2°C, 104.2°C	180.0°C, 108.0°C
N_f	32,757 cycles	32,002 cycles
Wire bond picture		
Photograph of the failure points		
Failure mode	**Wire bond lift-off**	**Solder failure**

Fig. 7: Failure point observation results for Sample A and D

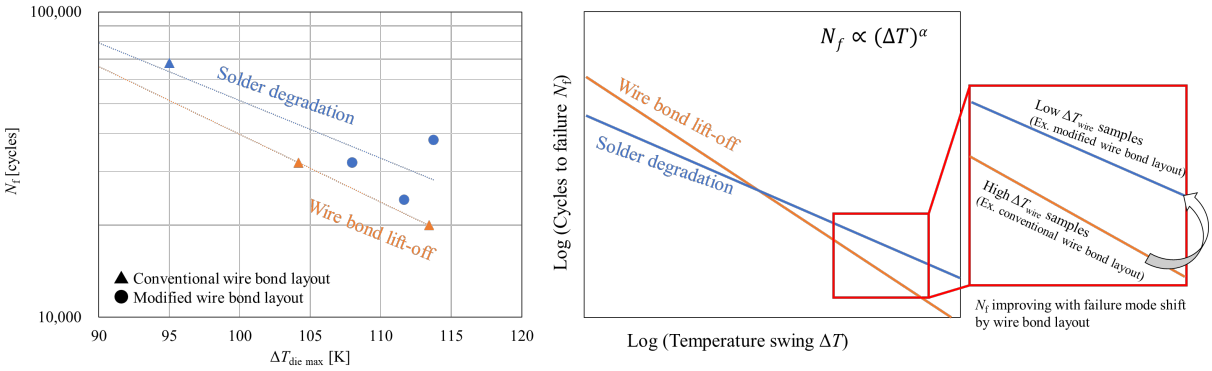


Fig. 8: PC curve with failure mode difference and the description of the failure mode shift.

Furthermore, the PC curves were classified into two lines according to the failure mode. The PC curve of wire bond lift-off in Samples A and B is lower than that of solder failure. Samples A and B are also conventional wire bond layouts. On the other hand, Sample C, along with the other conventional layout, was in solder failure mode under low ΔT_{diemax} test conditions. All samples with a modified layout (Sample D-F) were also in solder failure mode with a higher N_f PC curve line. Previous research estimated the N_f on PCT by the following equation (2) [19]. The model is generally formulated by fitting the N_f with different die temperature swings ΔT.

$$N_f = A \times \Delta T^{\alpha} \times \exp(\beta / T_{jmean}) \tag{2}$$

where A, α, and β are constants from the measured data fittings. Then, these values are determined by the design, such as die area, die thickness, and bond wire diameters [19]. These models from references contain a mixture of two failure modes: wire bond lift-off and solder degradation. In particular, in $N_f(\Delta T)$, which is a function of ΔT, the constant α is a factor that determines the slope of PC curves. The experimental results show that the slope α of the PC curve differs depending on the failure mode of power modules [12, 18]. The slope value α is larger in the wire bond lift-off failure mode than in solder degradation in the reference [12]. As a result, under high temperature swing ΔT conditions, wire bond lift-off is the dominant failure mode, and the failure mode at low ΔT shifts to the solder layer. Under lower ΔT conditions, the solder failure mode is predicted to be the main failure factor, as shown in Fig. 8. This may explain why a solder failure mode was identified in Sample C. On the other hand, at high ΔT conditions, the solder lifetime at the same temperature swing is higher than the wire bond lift-off lifetime. This explains why sample D-F (modified layout) with solder failure has a higher N_f than sample A-B (conventional layout) with wire lift-off in the PCT at the same ΔT. Comparing Sample A and D, both have about the same ΔT test conditions with different ΔT_{wire} shown in Fig 3. For example, 6.2% lower ΔT_{wire} caused a shift in the failure mode. This suggests that the suppression

of wire heating ΔT_{wire} increased the wire bond lifetime, and the shift of the failure mode from wire bond lift-off to solder failure occurred at the higher ΔT condition. Wire bond lift-off in PCT is due to shear stress. It has been reported that the driving force of this shear stress is the self-expansion of the wire during heat generation [11]. In this case, a large wire heating ΔT_{wire} causes a larger self-expansion of the wire. Therefore, suppressing ΔT_{wire} reduces the shear stress at the wire-die interface and improves the wire bond lift-off lifetime. As a result, it is considered that the solder degradation was observed in Sample D-F, where the wire bond lifetime was higher than the solder layer lifetime. Although only two data points were obtained for wire bond lift-off in the PCTs, the steeper slope is consistent with previously reported findings [12], which indicate a stronger dependency of wire bond lift-off on ΔT compared to solder degradation.

These were the two PC failure modes on 10 kV SiC-MOSFETs: wire bond lift-off and solder failure. The changes in failure modes can also be used to assess the optimization of the wire bond design. For example, if the wire bond layout minimizes ΔT_{wire} and the PC failure mode is solder failure, the wire design can be assessed as sufficiently optimized. Thus, changes in failure modes may be sensitive to the wire bond layout design, especially for dies with small wire bond density, such as 10 kV SiC-MOSFETs. Therefore, the validity of the design can be evaluated by considering the presence or absence of wire bond lift-off as a design parameter in the wire bonding layout design optimization method. This research presents a structural optimization method for improving their wire bond reliability. The wire bond layout with the lowest ΔT_{wire} in the simulation has the maximum PC lifetime to wire lift-off failure mode for 10 kV SiC-MOSFET power modules. This wire bond design strategy is superior because it is technically the simplest and can be implemented without additional cost. This discussion does not aim to improve the reliability of the solder layer. To extend the PC lifetime, structural design against solder degradation is necessary, and increasing the number of wire bonds is meaningless because the failure mode shifts from wire bonds to the solder layer. The identification of structural weak points obtained through this demonstration provides essential knowledge for designing more reliable power module structures.

Conclusion

For 10 kV SiC-MOSFET power modules, the effect of changing the wire bond layout on PC failure modes was demonstrated. The large edge area of the 10 kV SiC-MOSFET results in a significant temperature gradient on the die. However, the low current density of the die provides the high flexibility of the wire bond layout. These unique factors of 10 kV SiC-MOSFETs enabled the improvement of N_f through a modified wire bond layout by suppressing the ΔT_{wire}. The result revealed that the wire bond layout modification with ΔT_{wire} reduced by 6.2% in the simulation changed the failure point from wire bonds to solder layers. This failure mode shift was expected to a higher N_f from the statistical understanding based on the PC curve. The results show that wire bonds can be optimized by layout design using the 3D temperature simulation and a minimum number of prototypes. In other words, this study demonstrated an efficient design method to improve the reliability of 10 kV SiC-MOSFET power modules using 3D simulations.

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