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Low-Inductance Packaging Design for SiC Power MOSFET Modules

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Abstract. With the continuous advancement of SiC device design and manufacturing processes, devices of the same ratings are achieving higher turn-on speeds and smaller chip areas. These improvements enhance the speed and power density of power electronic systems but also pose greater challenges for thermal management and the parasitic parameters of packaging. To address these issues, this paper proposes a multi-chip SiC power module packaging structure based on a multilayer ceramic substrate. Compared to a conventional single-layer DBC substrate, the multilayer substrate structure incorporates an additional intermediate copper layer, which serves as a current return path. Due to the close proximity between this return path and the upper copper layer, the overall loop area is reduced, thereby lowering the parasitic loop inductance. Simulation results show that the designed 800 V, 50 kW SiC power module achieves a parasitic loop inductance of around 3.22 nH at 10 MHz. In addition, traditional multilayer DBC structures are typically formed by soldering two separate DBC substrates together. Such soldered interfaces are often mechanically unstable, and electrical continuity between the upper and intermediate copper layers is not established. The structure proposed in this work adopts a monolithic substrate, in which a single 300 μm thick copper layer is embedded without the use of additional solder. Compared to conventional multilayer substrates, this configuration offers improved thermal conduction by eliminating solder interfaces and enhancing heat flow.

Introduction

The advancement of silicon carbide (SiC) power devices demands innovative packaging solutions that can fully exploit their superior electrical, thermal, and switching performance. Traditional silicon-based packaging techniques often fall short in meeting the high-temperature operation, fast switching speeds, and reduced parasitics that SiC devices enable [1]. As a result, novel packaging approaches are being developed to address these challenges [2, 3]. These include double-sided cooling configurations [4, 5], the use of advanced substrates such as silicon nitride (Si_3N_4) and aluminum nitride (AlN) for improved thermal conductivity and mechanical reliability [6], and the integration of 3D packaging structures [7]. Additionally, low-inductance interconnections using wide metal clips or embedded die technology are gaining traction, aiming to minimize loop inductance and enable high-speed switching with reduced voltage overshoot and oscillations which could have serious reliability consequences [8].

More recently, high-temperature capable materials, such as sintered silver (Ag) die attach and high-temperature polymers, are being explored to increase the thermal and mechanical robustness of SiC modules [9]. The shift toward fully lead-free, high-reliability interconnects also aligns with global sustainability goals and regulatory standards. Embedded passive components, integrated sensors, and advanced thermal interface materials are being incorporated to enable smart, compact, and more efficient power modules. These packaging innovations are not only essential for leveraging the benefits of SiC devices, but they also represent a critical step toward achieving higher power density, longer lifetime, and lower system cost in next-generation power electronics.

The aim of this paper is to investigate a low-parasitic, high-reliability multi-chip power module packaging structure for Wolfspeed Gen 3+ SiC MOSFETs. In this context, a multilayer ceramic substrate for the power module is designed. The fabricated module employs silver sintering for die attachment and wire bonding for electrical interconnection. Furthermore, the simulations are conducted using COMSOL to analyze the thermal, parasitic inductance, and electric field distributions within the multilayer substrate-based power module.

Design Approach

Module development.

Fig.1 shows the proposed multilayer power module structure. The monolithic substrate consists of three copper layers. Apart from the top and bottom layers, which are similar to a standard DBC design, an additional middle layer serves as the return path for the current. The DC pattern fills the entire middle layer and connects it to the top layer. This substrate structure enables a shorter distance between the DC+ and DC- patterns, thereby increasing the mutual inductance between them and reducing the overall loop inductance.

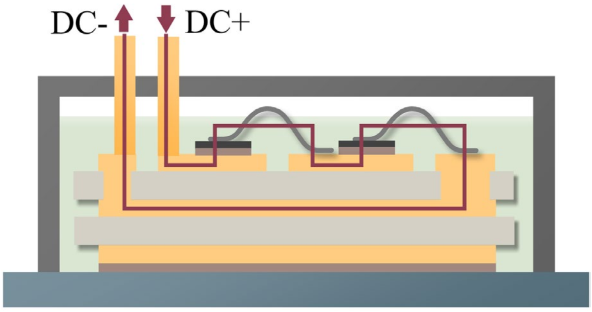


Fig. 1. Schematic diagram of multilayer substrate power module. The middle layer copper works as the current return loop.

Based on the multilayer substrate, a 1200V, 50kW SiC half-bridge power module is designed, as shown in Fig.2(b). Two parallel Wolfspeed EPM3-1200-R013D SiC MOSFET dies are used for each half-phase leg to ensure a 200A rated current. Laminated DC+ and DC- busbars are chosen to further reduce loop inductance. The module integrates a hybrid PCB as the current loop for the gate signal. A Kelvin connection is used for the gate signal design to ensure the separation of the power loop and the drive loop. For comparison, a conventional power module is designed, as shown in Fig.2(a).

For the proposed multi-chip SiC power module structure, the design is also well-suited for scaling the number of chips, for example, from two in parallel to four or even six in parallel. Such scaling can be achieved while maintaining the module's symmetrical layout and ensuring current sharing among individual chips. Moreover, although the width of the overall power loop increases with scaling, its length remains unchanged, which is beneficial for reducing loop inductance. In contrast, for the conventional chip layout shown in Fig. 2(a), it is difficult to expand the number of chips while preserving both compact module design and low loop inductance.

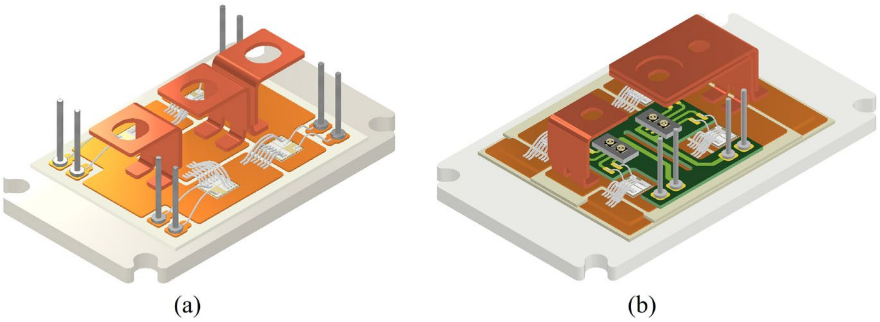


Fig. 2. (a) Conventional power module structure. (b) Multi-chip power module packaging with multilayer ceramic substrate.

Fig. 3 illustrates the assembly process of the power module. The primary difference in the proposed structure lies in the use of a multilayer ceramic substrate. Aside from the substrate, the assembly process remains similar to that of a conventional module. The process begins with the preparation of the multilayer ceramic substrate. Subsequently, the power semiconductor dies are attached to the substrate, followed by bonding of the substrate to the baseplate. The PCB for the gate drive loop is then mounted onto the substrate. This step is followed by wire bonding and the installation of current sensors on the PCB. Next, the external terminals and pins are soldered to the module. Finally, the case is installed, and encapsulation is carried out to complete the assembly.

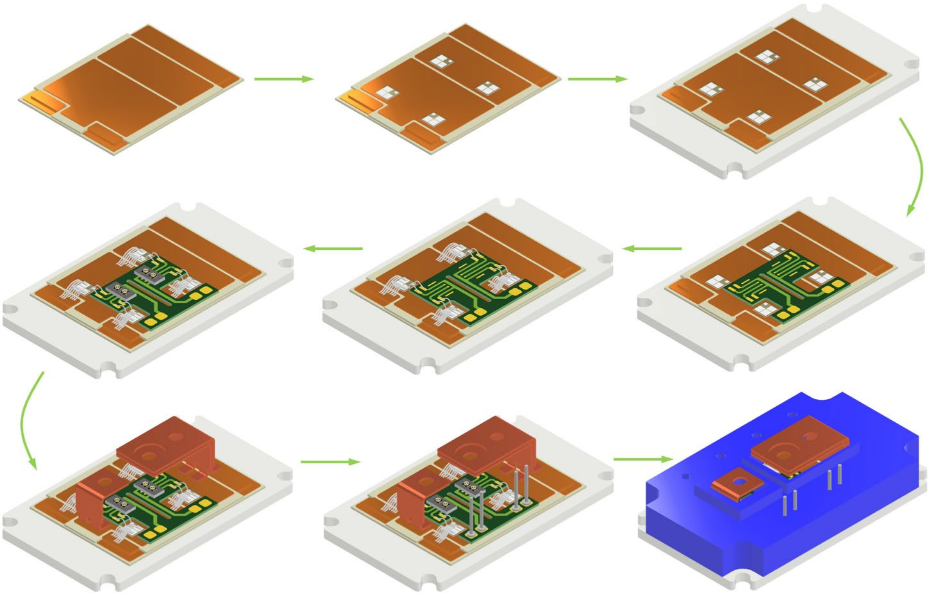


Fig. 3. Manufacturing process of a novel SiC Module.

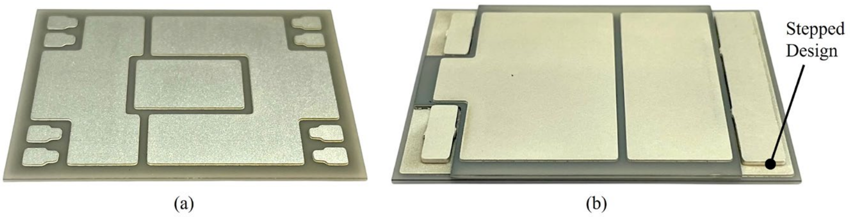
Modeling and Simulation.

To verify the thermal performance and measure the loop inductance of the module, a COMSOL Multiphysics model is developed. The module employs liquid cooling for heat dissipation. To simulate forced convection liquid cooling, a thermal convection coefficient of 15000W/m2K is applied to the bottom surface of the baseplate [10]. The coolant temperature is set to 24°C, and the power dissipation of each die is specified as 150 W.

Results and Discussion

Fig. 4 illustrates both the single-layer and multilayer substrate structures. In the case of the multilayer substrate, the electrical connection between the upper and lower copper layers results in a thicker overall copper structure, which can cause significant mechanical stress at the bonding interface near the ceramic edge. This stress concentration may lead to cracking of the ceramic. To mitigate this issue, a stepped design is applied at the edge of the interconnected copper layers, effectively reducing the localized stress in that region.

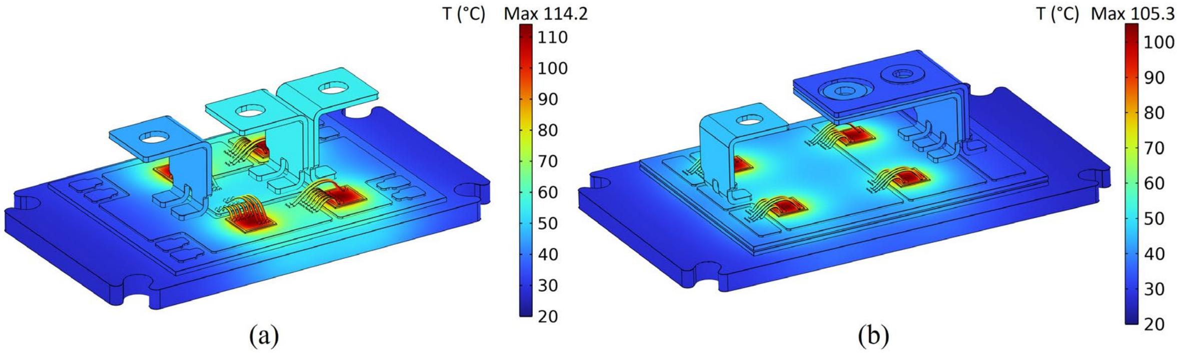
For the substrate, the copper layer has a thickness of 300 μm, and its surface is plated with silver to facilitate the silver sintering process during die attachment. Aluminum nitride (AlN) is used as the ceramic material, providing a high thermal conductivity of approximately 180 W/m·K.



(a) (b)

Fig. 4. The fabricated substrates for the modules. (a) Single-layer substrate. (b) Multilayer substrate.

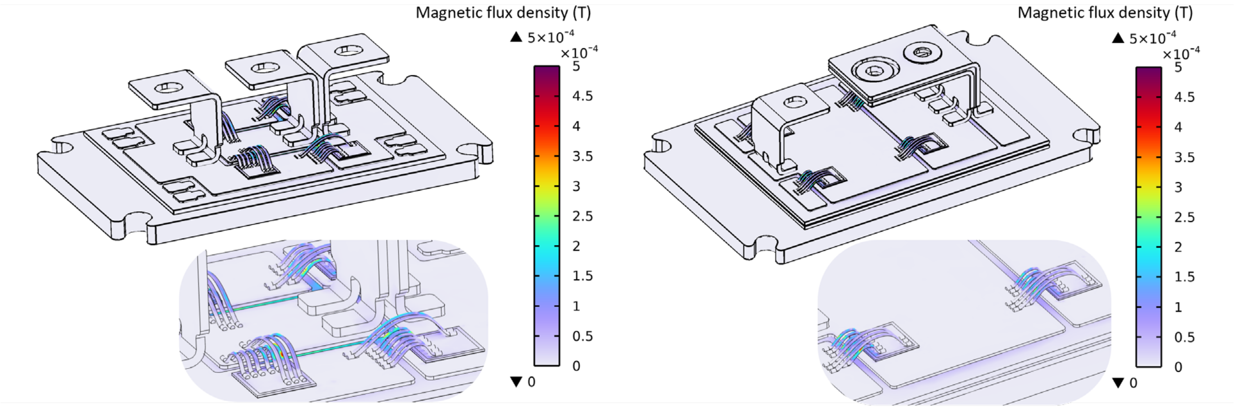
The temperature field of the module is shown in Fig.5. The results indicate that the maximum junction temperatures of conventional packaging and multilayer substrate packaging are 114.2°C and 105.3°C, respectively. For the multilayer substrate module, the average device temperatures are in the range of 90.5°C to 91.2°C, indicating a relatively uniform current and temperature distribution during operation. The maximum junction temperature also corresponds to a favorable operating point for the package. The thermal resistances from junction to coolant for the conventional module and the multilayer power module are 0.150 K/W and 0.136 K/W, respectively. These results demonstrate that, although the substrate thickness increases due to the additional layers, the thermal performance can still be improved through an optimized module layout.



(a) (b)

Fig. 5. Modelled temperature field of module with (a) conventional & (b) multilayer ceramic substrate.

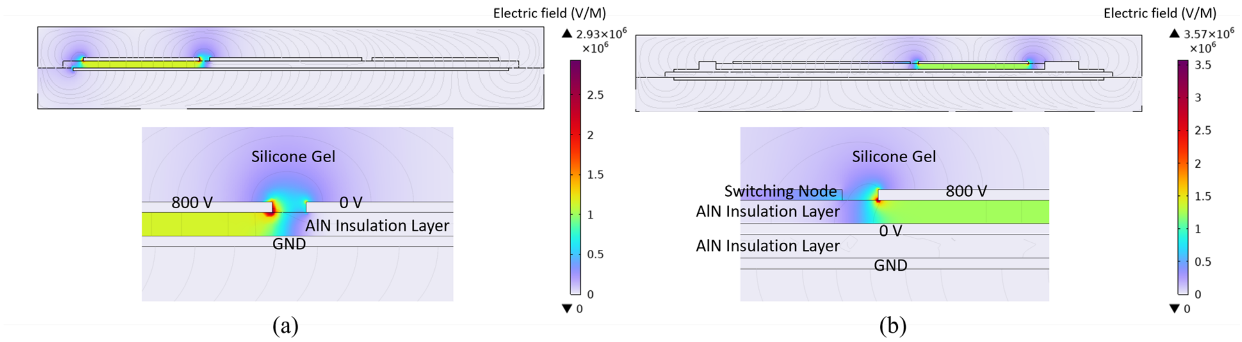
The simulated loop inductances of the conventional power module and the multilayer power module are 4.82 nH and 3.22 nH at 10 MHz, respectively, demonstrating the improved performance of the proposed design in minimizing parasitic inductance [11]. Fig. 6 illustrates the magnetic flux density distribution of the conventional and multilayer substrate power modules.



(a) (b)

Fig. 6. Magnetic flux density distribution of (a) conventional and (b) multilayer substrate module.

Fig. 7 illustrates the simulated electric field distribution of the modules. The strongest electric fields appear at the triple-point regions of each module. In this case, the results actually indicated a slightly higher electric field in the multilayer substrate 1.2 kV module compared with the conventional design, albeit with small margin. This is likely due to the reduced spacing between the 800 V and 0 V nodes in the multilayer configuration. Nevertheless, for low voltage SiC power modules (with operating voltage below 2 kV), the overall electric field strength remains significantly lower than that in medium voltage power modules [2, 3]. Consequently, the risk of partial discharge failure is extremely low, and the increase in electric field strength introduced by the multilayer substrate technology remains well within the safety margin.



(a) (b)

Fig. 7. Electrical field distribution in (a) single-layer packaging and (b) multilayer packaging.

Summary

A SiC power module with a multilayer substrate is designed and evaluated using COMSOL Multiphysics. The module incorporates four SiC MOSFETs, with two parallel-connected devices used for the high side and the other two for the low side. Simulation results indicate that the proposed multilayer substrate design outperforms the conventional module in terms of thermal performance and loop inductance, demonstrating the potential of the proposed structure for improved power module performance.

Acknowledgement

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