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A Multi-Manufacturer Test Campaign to Assess the Power Cycling Capability of Silicon Carbide MOSFETs in TO-247 Packages

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Abstract. In this work, the power cycling capability of discrete SiC MOSFETs of seven manufacturers is investigated. The results show that even nominally similar devices can exhibit substantially different power cycling capabilities. The differences among the tested devices involve the scaling factor and the slope of the lifetime curves, but also the dependence of the baseline temperature. Furthermore, some devices exhibit a considerable increase in power cycling performance towards lower temperature swings, which cannot be characterized properly by power cycling tests at typical test conditions with much larger temperature swings. Thus for a proper assessment of the power cycling performance, multiple tests at suitable test conditions are necessary to obtain meaningful results.

Introduction

Today, discrete SiC MOSFET devices, particularly devices in TO packages such as the TO-247 family, are increasingly used for demanding applications. As a consequence of the mission profiles, particularly in terms of load cycling, the power cycling capability becomes increasingly relevant. While the research on thermo-mechanical ruggedness used to be mainly focused on power modules, more and more research related to power cycling is performed on discrete devices [1, 2]. The TO-247 package is a standard package and devices with similar primary electrical parameters are available from a variety of different manufacturers. Due to the different background of the different manufacturers, the landscape of devices in terms of device technology and packaging aspects is quite diverse. While the variability in power cycling lifetime of SiC MOSFETs was already reported in [1], no systematic comparison on a large scale has been performed so far. In this work, the power cycling capability of nominally similar SiC MOSFETs of different manufacturers is investigated to assess the variability in power cycling capability of different device designs on a larger scale.

Devices Under Test

This investigation includes seven different SiC MOSFET designs from different manufacturers. All tested devices feature a nominal blocking capability of 1200 V and a similar $R_{\mathrm{DS,on}}$ between 70 mΩ to 90 mΩ. Both trench and planar designs were tested. While their primary electrical parameters are comparable, other design aspects and packaging parameters are different. The range of some relevant design and packaging parameters of the different designs is summarized in table 1. The parameters are normalized to the respective minimum of the considered designs. Even though all devices feature a similar $R_{\mathrm{DS,on}}$ and are packaged in similar housings, the number and diameter of bond wires is considerably different. Even though all devices feature a relatively similar drain current rating I_{D}, the total bond wire cross-section, which is directly correlated with the bond loop resistance assuming equal bond wire length, varies substantially by a factor of 3.1.

Besides the packaging related parameters, the device dimensions differ considerably. The device characteristics also reveal the strong correlation between chip thickness and required chip are to achieve the same $\mathrm{R}_{\mathrm{DS,on}}$. Since the substrate resistance is reduced for thinned chips, the total chip area can be smaller. This correlation is visible through the even larger spread in chip volume. Besides

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Table 1: Relevant design parameters, normalized to the respective minium value of all designs.

Properties	Parameter variation of all designs (normalized)	
	min	max
No. of bond wires	1	4
No of stitches per bond wire	1	2
Bond wire diameter	1	2.8
Total bond wire cross-section	1	3.1
Chip area	1	2.1
Chip thickness	1	3.2
Chip volume	1	6.7
Chip aspect ratio	1	2.0
$R_{th,js}$ (measured)	1	1.2

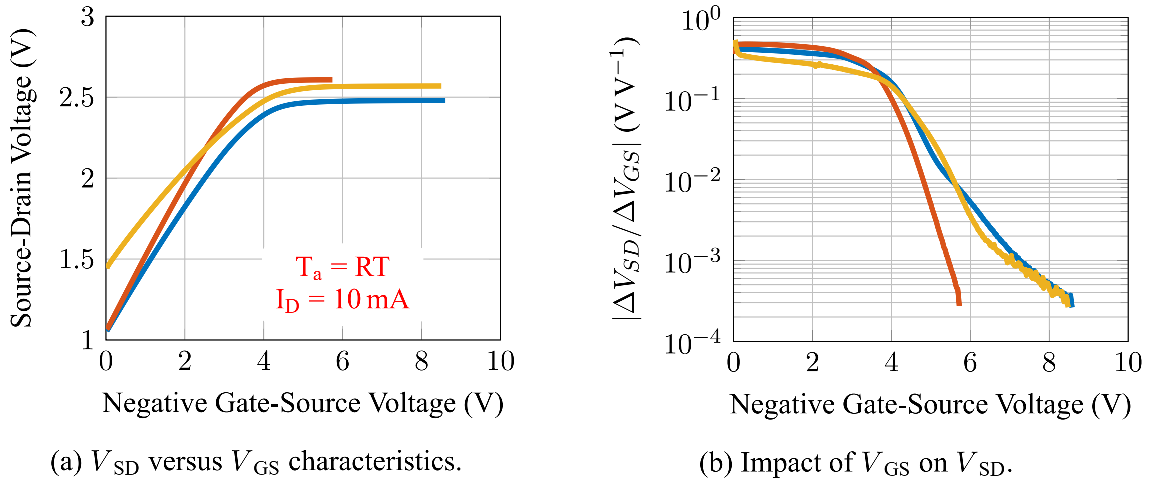
Table 2: Summary of the test conditions of all test runs at target $T_{vj,min} = 50\,°C$.

Design	$\Delta T_{vj} = 60\,K$		$\Delta T_{vj} = 80\,K$		$\Delta T_{vj} = 100\,K$		$\Delta T_{vj} = 120\,K$	
	run #	I_{load}	run #	I_{load}	run #	I_{load}	run #	I_{load}
A	1	22.3	2	24.1	3	26.0	4	27.5
B	5	19.0	6	22.0	-	-	7	23.5
C	8	19.9	9	21.9	10	23.9	-	-
D	11	17.8	12	19.8	13	20.3	14	20.8
E	15	16.3	16	16.8	17	17.5	-	-
F	18	21.6	19	23.3	20	24.6	-	-
G	21	21.3	22	22.3	23	23.5	-	-
	$T_{air} = 39\,°C$		$T_{air} = 33\,°C$		$T_{air} = 29\,°C$		$T_{air} = 26\,°C$	
	$t_{on} = 3\,s$, $t_{off} = 6\,s$							

the parameters given in table 1, other packaging properties, such as the mold compound and the solder composition, are also different among the tested devices, but could not be quantified in this work.

Test Setup and Test Conditions

The PCTs were performed in a test bench with forced air cooling and with each DUT mounted on a separate heat-sink with controlled air inlet temperature (cf. [3]). Each considered device design is tested at least at three different target temperature swings ΔT_{vj} between 60 K to 120 K. For all tests and all designs the target minimum temperature were kept constant at $T_{vj,min} = 50\,°C$. The heating and cooling times (t_{on} and t_{off}) were kept constant for all test runs and the target ΔT_{vj} was set by adjusting the load current I_{load} accordingly. $T_{vj,min}$ was set by adjusting the air inlet temperature T_{air}. The test conditions and the deployed I_{load} for all test runs are summarized in table 2. While all devices were tested at target ΔT_{vj} of 60 K and 80 K, design B had not been tested at 100 K and only three designs (A, B and D) were tested at a target ΔT_{vj} of 120 K due to individual agreements with the manufacturers. For each run a total of 16 devices was tested. Test run 2 was performed twice to assess reproducibility and thus, a total of 384 devices had been tested. It is visible that even though the devices feature a similar nominal $R_{DS,on}$, the required I_{load} to achieve the same temperature swing differs considerably. To achieve a ΔT_{vj} of 80 K, design A require an I_{load} of 24.1 A, while design E only requires 16.8 A. This cannot be fully attributed to the differences in $R_{DS,on}$ and thus, indicates a



(a) V_{SD} versus V_{GS} characteristics.

(b) Impact of V_{GS} on V_{SD}.

Fig. 1: Impact of the gate voltage on the third quadrant characteristics.

different $R_{\mathrm{DS,on}}$ temperature dependence for the different designs. The $R_{\mathrm{DS,on}}$ increase factor between 50 °C and 130 °C of the different designs is in the range of 1.4 to 2.4. Also, it can be observed that the difference in I_{load} between the test runs at ΔT_{vj} of 60 K and 120 K differs among the different designs. The increase in I_{load} between the two ΔT_{vj} is only ca. 7 % for design E, while is is 20 % for design C. Due to the test bench topology, all DUTs of the same test run were subject to the same I_{load}, t_{on}, t_{off} and T_{air}. To mitigate inevitable differences in ΔT_{vj} due to parameter spread among the test lots, the gate voltage V_{GS} was slightly adjusted for each DUT individually to achieve roughly the same ΔT_{vj}.

Junction Temperature Estimation by $\mathrm{V_{SD}}$-Method. The virtual junction temperature was estimated by deploying the $\mathrm{V_{SD}}$-Method. The sensing current was determined for each device design based on the ideality factor, as described in [4]. Since the $\mathrm{V_{SD}}$-Method relies on the voltage drop of the body-diode, it is important to make sure that the channel is completely closed. Since the required negative gate voltage $V_{\mathrm{GS,off}}$ varies considerably for different device designs, it must be determined for each design. For this investigation, the required $V_{\mathrm{GS,off}}$ was determined by considering the differential of V_{GS} versus V_{SD} as quality gauge. An illustration of the principle behind this method with samples outside the scope of this test campaign is shown in Fig. 1. The V_{GS} versus V_{SD} characteristics in Fig. 1a shows that all devices exhibit a significant impact of V_{GS} on V_{SD} above −4 V, which rapidly decreases for more negative V_{GS}. However, the V_{GS} at which its impact decreases is not the same for all devices. The differential of the The V_{GS} versus V_{SD} characteristics, which can be calculated by

$$\left|\frac{\Delta V_{\mathrm{SD}}}{\Delta V_{\mathrm{GS}}}(k)\right| = \left|\frac{V_{\mathrm{SD}}(k) - V_{\mathrm{SD}}(k-1)}{V_{\mathrm{GS}}(k) - V_{\mathrm{GS}}(k-1)}\right|, \tag{1}$$

can be used as a gauge for the minimum required V_{GS}, where k is the index of the associated data point. The resulting characteristics is shown in Fig. 1b, whereas the y-axis is in log scale. Initially, the slope is relatively shallow and similar for all designs, but rapidly decreased below −3 V to −4 V. For more negative V_{GS} the differences among the designs increase. In this work, a threshold of 0.1 % (1 mV/V) was deployed to determine a suitable $V_{\mathrm{GS,off}}$. The accuracy of the temperature estimation by the $\mathrm{V_{SD}}$-Method was assessed by the methods presented in [5] and the T_{vj} reading, where applicable, was corrected accordingly. However, this was only necessary for a very small number of designs and the vast majority of designs yield a good accuracy of the $\mathrm{V_{SD}}$-Method with optimized measurement parameters according to the aforementioned considerations and the method presented in [4].

Test Results

The prevalent failure mechanism of all test runs was bond wire failures, which is consistent with previous reports [6, 2, 7]. As a failure criterion, a step-increase in V_{DS}, which could not be attributed

Table 3: Summary of the test results of all test runs at target $T_{\mathrm{vj,min}} = 50$ K.

#	Des-ign	No. of DUTs		Cycles to failure ($\times 10^3$ cycles)			ΔT_{vj} (K)		$T_{\mathrm{vj,min}}$ (°C)
		Con	Cens.	Weibull Scale	Std. dev.	Weibull shape	Mean value	Std. dev.	
1	A	11	5	298.6	44.4	7.5	59.5	0.3	52.3
2	A	27	5	82.2	9.6	9.8	79.0	0.6	51.9
3	A	11	5	42.3	4.9	9.9	99.2	0.8	51.3
4	A	15	1	27.0	2.4	13.1	119.3	0.8	49.8
5	B	9	7	1257	150.7	9.5	59.5	0.5	51.9
6	B	11	5	109.4	21.6	5.4	79.0	1.1	50.5
7	B	11	5	18.1	2.6	7.7	119.3	1.1	52.5
8	C	14	2	200.2	55.2	3.6	59.4	0.5	51.8
9	C	11	5	57.3	9.7	6.4	78.6	1.2	51.4
10	C	12	4	23.2	5.3	4.6	97.4	3.1	53.1
11	D	11	5	192.6	18.5	12.1	59.9	0.4	50.1
12	D	16	0	110.3	18.4	6.5	77.5	0.8	48.7
13	D	13	3	64.1	9.3	7.7	99.5	1.2	51.5
14	D	16	0	41	10.8	3.8	116.2	1.8	50.3
15	E	11	5	170.7	13.4	15.1	59.0	0.5	51.6
16	E	13	3	42.4	6.2	7.6	80.3	0.6	51.8
17	E	13	3	16.8	2.3	8.1	99.8	0.9	51.2
18	F	11	5	270.2	49.7	4.6	60.2	0.3	52.7
19	F	13	3	78.3	10.7	8.2	80.6	1.8	52.1
20	F	13	3	28.9	3.5	5.6	99.8	0.8	52.0
21	G	15	1	118	26.7	4.6	59.2	0.8	53.2
22	G	15	1	42	6.6	7	79.2	0.6	52.3
23	G	15	1	16.3	3.2	5.4	97.9	1.8	52.1

to external causes, was considered. During this test campaign none of the DUTs exhibited clear signs of chip solder degradation. However, some DUTs exhibited other signs of degradation of the thermal path, i.e. thermal interface material (TIM). For the statistical analysis only DUTs with clear bond wire failures were considered. Furthermore, DUTs with an outlier $R_{\mathrm{DS,on}}$ that could not be homogenized by adjusting V_{GS} within a reasonable range, as well as individual DUTs with a substantially different lifetime compared to the majority of DUTs of the same test run, were disregarded. Even though no systematic impact of V_{th} drift effects on the PCT results could be observed for any design, some DUTs exhibited a non-package related parameter drift and thus, were also not considered for the statistical evaluation. For further information and illustrations refer to [3]. During this test campaign, on average 3 out of 16 DUTs had been disregarded per test run.

Lifetime Modeling The test results of all test runs with the respective test parameters and number of cycles to failure N_f are summarized in table 3. For the lifetime modeling, the Weibull scale parameters, corresponding to the number of cycles to failure of 63.2 % of the test population, are used. For each design, a lifetime model is derived by fitting the test data for the respective design to the Coffin-Manson equation:

$$N_{\mathrm{f}} = K \cdot \Delta T_{\mathrm{vj}}{}^{\beta_1}. \qquad (2)$$

The data points and the resulting lifetime models are shown in Fig. 2, whereas the error bars indicate the standard deviation of ΔT_{vj} (along x-axis) and for the Weibull scale parameter (along y-axis).

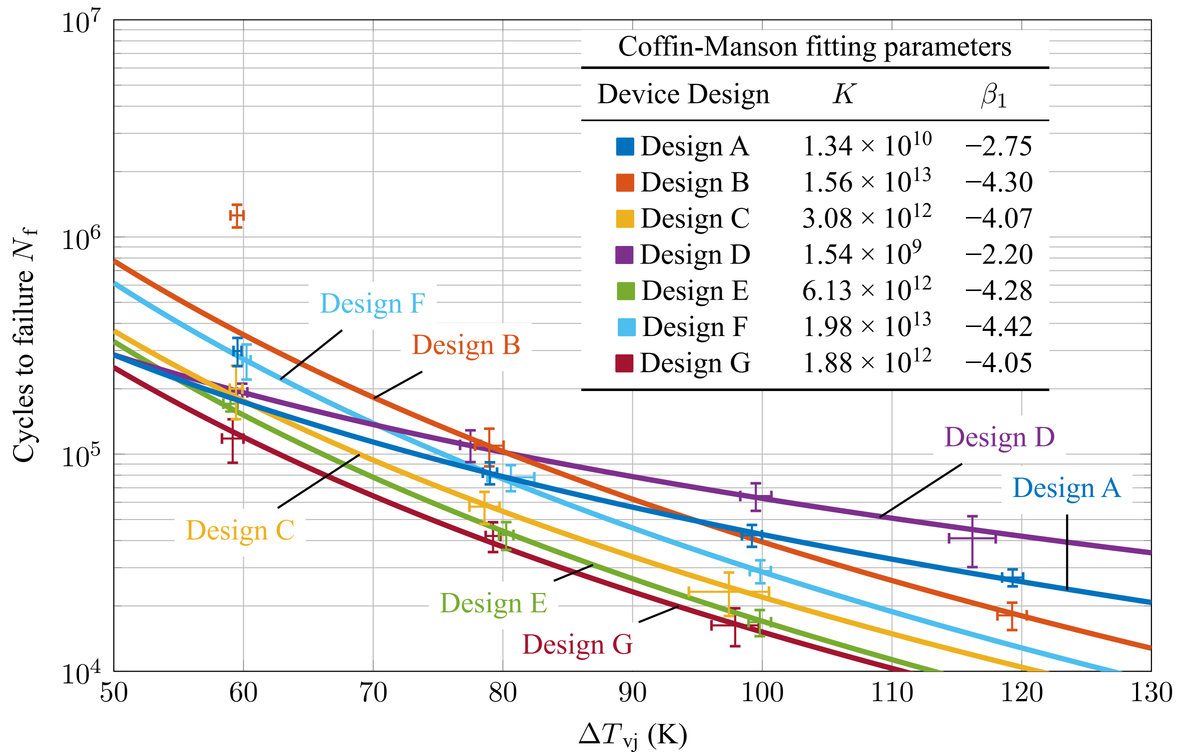
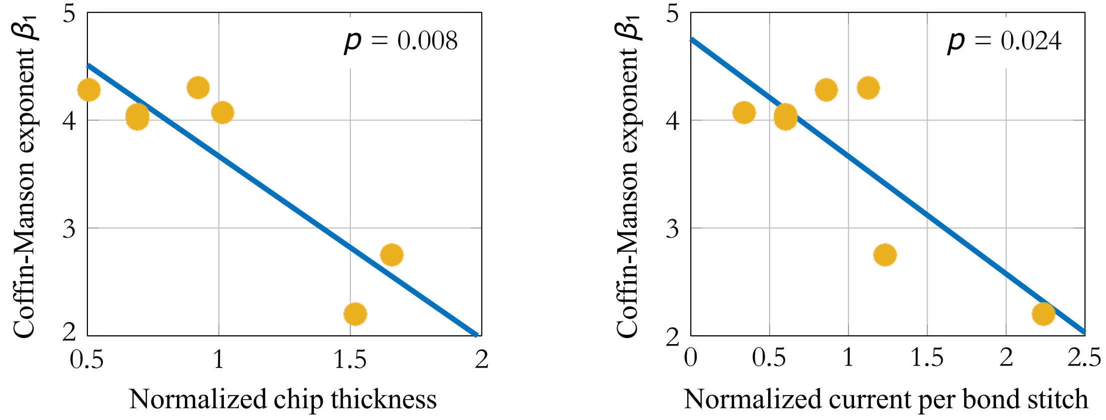


Fig. 2: Lifetime plots according to the Coffin-Manson equation, based on the fit to the test data (Weibull scale parameter) between ΔT_{vj} = 80 K to 120 K and with constant $T_{\mathrm{vj,min}}$ = 50 °C for all designs. The inset table summarizes the respective fitting parameters.

The respective Coffin-Manson fitting parameters are given in the inset table in Fig. 2. The lifetime model fits were obtained by considering the test data between ΔT_{vj} = 80 K to 120 K, which is the range of typical test conditions for PCTs. The data points at ΔT_{vj} = 60 K is used for verification. The results show that even though all designs exhibit very similar primary electrical ratings, their power cycling capability is substantially different. The scaling factor K varies by 4 orders of magnitude and considering the model fits at ΔT_{vj} = 100 K, the resulting lifetime varies by a factor of 4.1. Due to the variation in β_1, the variation at ΔT_{vj} = 80 K is around 2.8 and as high as 5.8 at ΔT_{vj} = 120 K. While designs B, C, E, F and G feature a comparable Coffin-Manson exponent β_1 in the range of 4 to 4.5, which is comparable to the CIPS08 model, (ca. 4.4), a substantially lower β_1 was found for designs A and D with 2.75 and 2.2, respectively. As previously presented [3, 8], the model fits for design A and B yield a significant underestimation of the lifetime by a factor of ca. 1.68 for design A and 3.42 for design B. In contrast, the model fit to the data in the range of ΔT_{vj} = 80 K to 120 K exhibit a very good agreement with the test data at all ΔT_{vj} for designs C, D, E, F and G.

Hence, based on the results of this work, the investigated designs differ in three aspects, namely difference in scaling factors K for all designs, different β_1 parameters with 5 out of 7 designs exhibiting a β_1 comparable to the CIPS08 model, and a significant underestimation of the lifetime by the Coffin-Manson fit for ΔT_{vj} = 60 K for 2 out of 7 designs.

The deployed lifetime model only considers the impact of ΔT_{vj} to avoid ambiguous fitting results, since the majority of devices had only been tested at three different test conditions, i.e. at different ΔT_{vj}. Some more elaborate lifetime models consider additional test related parameters such as $T_{\mathrm{vj,min}}$, t_{on} and I_{load} [9, 10]. While $T_{\mathrm{vj,min}}$ and t_{on} have been held constant for these tests, I_{load} was used to achieve the respective target ΔT_{vj} for each run and thus, varied among the different designs and for the respective ΔT_{vj}, which leads to a strong correlation between ΔT_{vj} and I_{load}. Additionally, device and packaging related parameters such as the bond wire diameter D and voltage class, i.e. device thickness V, are considered in the mentioned lifetime models.



(a) Regression plot for β_1 versus chip thickness.

(b) Regression plot for β_1 versus current per bond stitch I_{bw} at ΔT_{vj} = 80 K.

Fig. 3: Regression analyses for chip thickness and current per bond stitch versus β_1

To assess if known parameters could explain the differences among the different designs, regression analyses were performed for multiple parameters such as chip thickness, bond wire diameter, bond wire aspect ratio, total bond wire cross-section and current per bond stitch I_{bw}, i.e. current per bond wire divided by the number of bonds attached to the chip per wire [9]. It is worth noting that a regression analysis was only performed to assess whether the respective parameter could possibly explain the differences between the designs, not how the respective parameter correlates with the lifetime in general. The results of these regression analyses only yield positive signal, i.e. a p-value below 0.05, for the chip thickness and I_{bw}. The associated regression plots are shown in Fig. 3. The result suggests that the chip thickness impacts the β_1 parameter, i.e. the slope of the lifetime curve with respect to ΔT_{vj}, whereas thinner chips exhibit a steeper slope, i.e. a larger β_1. This is in agreement with previous reports on different SiC MOSFETs in SOT-227 package [11]. Additionally, the results indicate a correlation between I_{bw} and β_1, whereas a lower I_{bw} leads to a larger β_1. This is in agreement with the CIPS08 model and previous reports on discrete silicon IGBTs, which suggest a strong impact of the current per bond stitch [2, 12]. While these reports suggests a relationship described by a power term I_{bw}^{α} and not an impact on the Coffin-Manson exponent β_1, this could be explained by the strong correlation between I_{load} and ΔT_{vj}. However, it must be considered that in this work, the correlation could also be the result of the pronounced link between I_{load} and ΔT_{vj}. While the differences in β_1 and K could be explained at least to some extend by the aforementioned considerations, the substantial gain in lifetime towards lower ΔT_{vj}, observed for the designs A and B, could not be elucidated.

Impact of the Minimum Temperature To assess the impact of the minimum temperature $T_{vj,min}$, two designs (A and C) were also tested at three ΔT_{vj} but at an elevated $T_{vj,min}$ of 80 °C. The results were fitted to the equation

$$N_f = K \cdot \Delta T_{vj}^{\beta_1} \cdot e^{\frac{\beta_2}{T_{vj,min}}}, \quad (3)$$

consisting of the Coffin-Manson term according to eq. (2) and extended by an Arrhenius term, which is commonly used to include the baseline temperature [9, 10]. Equation (3) is commonly referred to as LESIT model. The resulting lifetime plots are shown in Fig. 4 and the respective parameters are summarized in the inset table in Fig. 4. For both designs the β_1 parameters are consistent for the two $T_{vj,min}$ and the differences in β_1 between the two designs could be confirmed. Additionally, the discrepancy between the fitted model and the data point at ΔT_{vj} = 60 K for design A is visible for both $T_{vj,min}$. The model underestimates the lifetime by a factor of 1.68 at $T_{vj,min}$ = 50 °C and 1.45 at $T_{vj,min}$ = 80 °C. However, the $T_{vj,min}$ dependency is considerably different for both designs. While the fitted β_2 factor is 774 for design A, is is substantially larger with 2598 for design B. By comparison, the CIPS08 model used a β_2 of 1285 while for discrete silicon IGBTs a value of around 1950 was

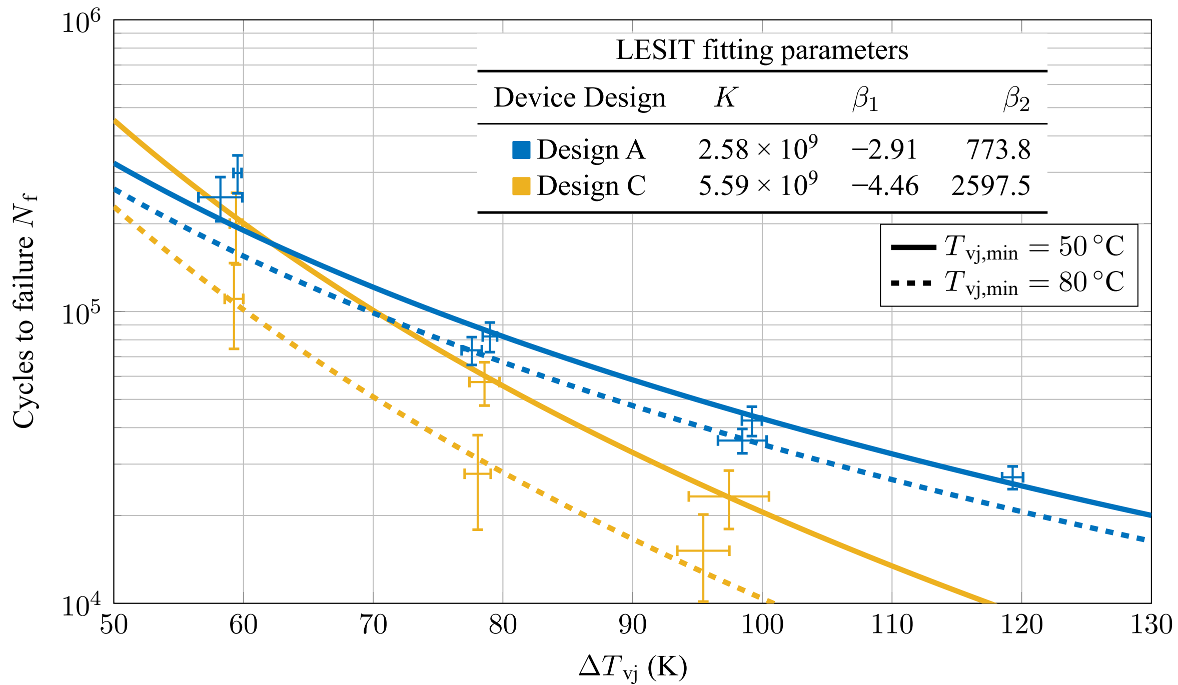


Fig. 4: Lifetime plots according to the LESIT equation with $T_{\mathrm{vj,min}}$ as baseline temperature for all designs. The test data (Weibull scale parameter) is fitted between ΔT_{vj} = 80 K to 120 K and for $T_{\mathrm{vj,min}}$ = 50 °C and 80 °C. The inset table summarizes the respective fitting parameters.

proposed [2]. Though the root cause for the different $T_{\mathrm{vj,min}}$ dependency could not be elucidated, the results clearly show that besides differences in scaling factor K, Coffin-Manson parameter β_1, as well as the deviation from the model fit towards lower ΔT_{vj}, the power cycling capability of SiC MOSFETs can also exhibit a substantially different dependence on the baseline temperature. Thus, it is important to thoroughly assess the power cycling capability for each device design individually and similarities should be assessed carefully, when experiences from other designs are incorporated.

Summary and Conclusion

In this work, the power cycling capability of different SiC MOSFET designs in TO-247 packages was investigated. For that purpose a power cycling test campaign with seven different device designs and a total of 384 DUTs was performed. The results were used for lifetime modeling and the power cycling results and fitted lifetime model parameter were assessed. The results indicate that seemingly comparable SiC MOSFETs can exhibit vastly different power cycling performances and fitting parameters for lifetime models. Furthermore, the results suggest a considerable impact by the chip itself, whereas the chip thickness seems to impact the slope of the lifetime curve through the Coffin-Manson exponent β_1. While some designs exhibit similar Coffin-Manson parameters β_1, i.e. dependency of the lifetime on ΔT_{vj}, others show a considerably different β_1. Additionally, further tests at a higher $T_{\mathrm{vj,min}}$ indicate a substantially different dependency on the baseline temperature for different designs. Furthermore, two designs exhibit a substantially increased lifetime at ΔT_{vj} = 60 K and below, which is not reflected by the power cycling test results at typically deployed power cycling test conditions, i.e. ΔT_{vj} of 80 K to 120 K. Therefore, testing at a single ΔT_{vj} is insufficient to characterize the power cycling performance of SiC MOSFETs and comparative tests of different designs at high ΔT_{vj} do not necessarily reflect their performances under field conditions. Consequently, for a proper estimation of the power cycling performance under field operation it is necessary to perform multiple tests under suitable test conditions. Furthermore, for comparative tests of different designs the potential variability in lifetime influencing factors should be considered to avoid misinterpretation of the test results.

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