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Temperature Dependence of the AC-BTI in SiC MOSFETs

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Abstract. The reliability of silicon carbide (SiC) MOSFETs under alternating current bias temperature instability (AC-BTI) is a critical issue for power electronics. Previous studies show inconsistent temperature dependence of threshold voltage drift (ΔV_{th}) induced by AC-BTI and have not conducted tests at temperatures below room temperature. In this study, ΔV_{th} was measured in four commercially available SiC MOSFETs across a wide temperature range (-40°C to 150°C) under bipolar AC stress up to 10^{11} cycles. Most devices showed larger ΔV_{th} at lower temperatures, while one device exhibited increased ΔV_{th} also at high temperatures. These results may be explained by interface recombination mechanisms, with the device-dependent behavior possibly attributable to structural differences. The findings suggest the need for sub-room temperature testing to identify worst-case degradation scenarios in SiC MOSFETs.

Introduction

SiC MOSFETs are widely adopted in the power electronics field as highly efficient devices compared to Si-based devices. However, these devices are known to exhibit inherent degradation modes, one of which is alternating current bias temperature instability (AC-BTI). It has been reported that applying bipolar AC stress (alternating positive and negative voltages) to the gate of a SiC MOSFET induces a drift of threshold voltage (V_{th}) [1-7]. The magnitude of V_{th} drift (ΔV_{th}) is known to depend on the test temperature; however, previous studies show inconsistent results regarding the temperature dependence of ΔV_{th}. While one study reports that ΔV_{th} increases with rising temperature [1], another study reports a decrease in ΔV_{th} with rising temperature [2]. These inconsistencies suggest that temperature dependence of ΔV_{th} varies with specific characteristics of the device. Nevertheless, previous studies have only evaluated this phenomenon at temperatures above room temperature. This study investigated temperature dependence of ΔV_{th} in SiC MOSFETs through AC-BTI tests across a wide temperature range, including both below and above room temperature.

Experimental

AC-BTI tests were performed using a newly developed AC-BTI test system, in which the devices were placed inside a temperature chamber (Fig. 1(a)). This system automatically switches between AC stress application and V_{th} measurement through a relay matrix switch, enabling highly reproducible testing conditions. Fig. 1(b) shows the test circuit diagram of V_{th} measurement and AC stress application.

In these experiments, the application of AC stress (+20 V/-10 V at 500 kHz) and the measurement of the threshold voltage (V_{th}) were alternately conducted at several specified temperatures. Notably, the test conditions included not only higher temperatures but also temperatures significantly below room temperature (−40°C and −10°C), allowing for a detailed investigation of device behavior under low-temperature environments, which have not been reported in previous studies.

The number of AC stress cycles was set at 10^{11}, which is specified as the minimum test cycle in AQG 324 [8] and is also used as a benchmark for automotive inverters in JEITA EDR 4713 Amend.1 [9]. This number is regarded as an important benchmark for long-term reliability evaluation.

V_{th} was measured using the triple sense protocol [8] (Fig. 2), and the values of V_{th_Up} were used to compare ΔV_{th} across different test conditions.

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Prior to each V_{th} measurement, a thermal stabilization interval of five minutes was established. This interval was essential because the application of AC stress leads to repeated charging and discharging at the gate, causing the device under test (DUT) to heat up. By allowing the DUT to cool down and return to the ambient temperature of the chamber during this interval, the influence of temperature variations on the measured V_{th} was eliminated. As a result, changes in ΔV_{th} could be accurately compared, without interference from temperature-dependent fluctuations.

Tests were conducted on four commercially available SiC MOSFETs (Table 1).

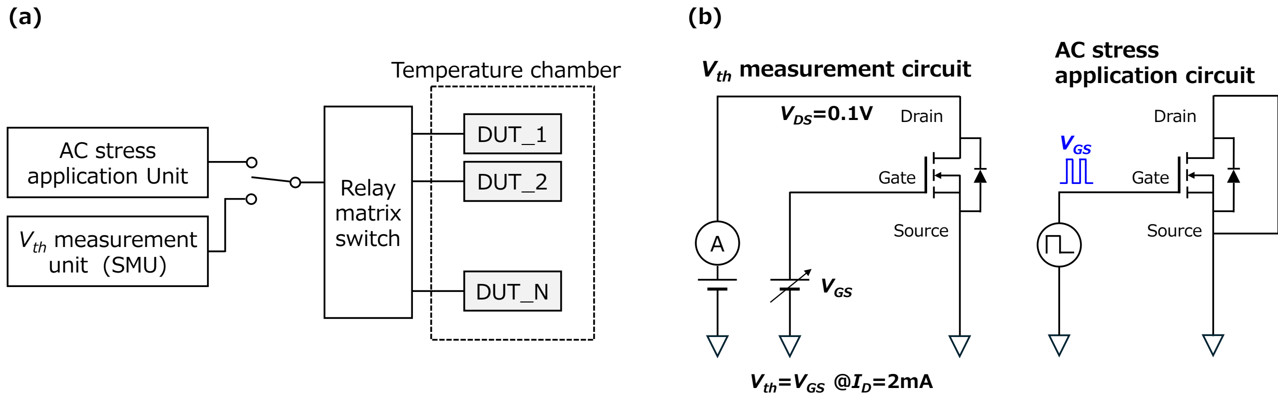

Fig. 1. (a) Schematic of AC-BTI test system. The DUT is placed inside a temperature chamber, and both AC stress application and V_{th} measurement are automatically switched and conducted via a relay matrix switch during the test. (b) Test circuit diagram of V_{th} measurement and AC stress application.

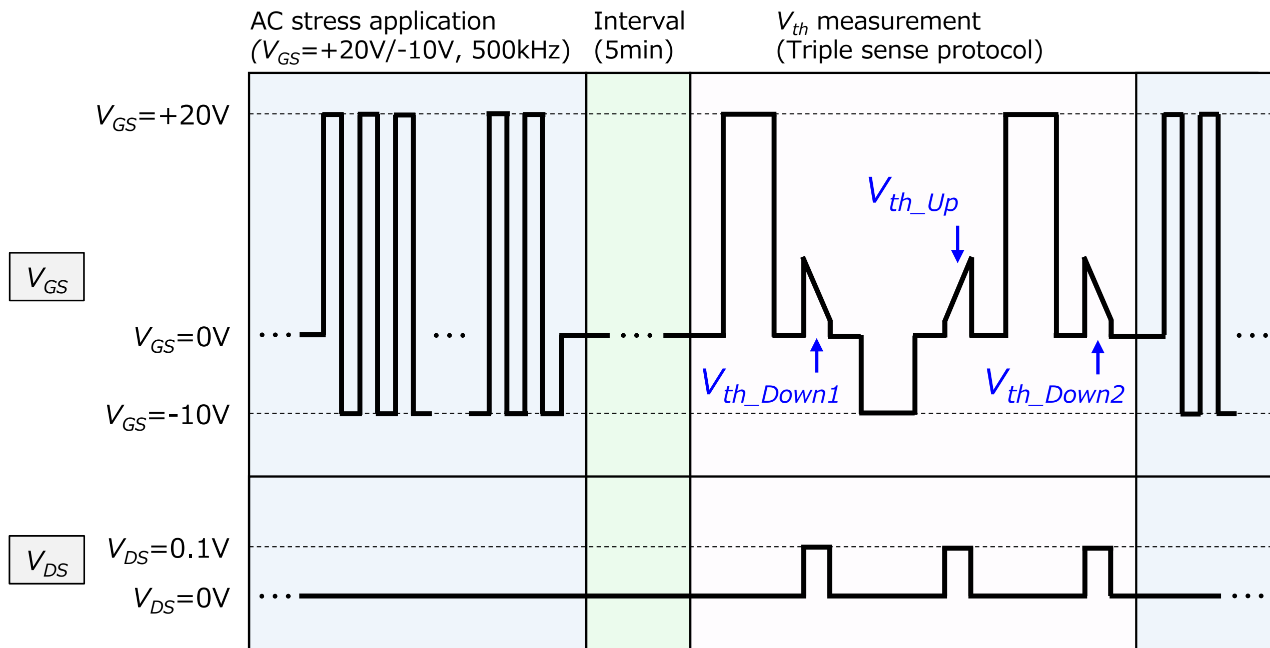

Fig. 2. Schematic waveforms of V_{GS} and V_{DS} in the AC-BTI test. An interval is provided between the AC stress application and the V_{th} measurement to allow the heated DUT to return to the ambient temperature.

Table 1. SiC MOSFETs employed for testing.

DUT	Gate structure	Rated V_{GS} [V]	Sample size
DUT_A	Trench	-5/+23	2
DUT_B	Trench	-4/+21	3
DUT_C	Planar	-8/+19	3
DUT_D	Planar	-10/+22	3

Results and Discussion

Fig. 3 shows the results of AC-BTI tests conducted under various temperature conditions. In all cases, ΔV_{th} increased as the number of AC stress cycles increased. Fig. 3(c) illustrates the relationship between ΔV_{th} at the end of the test (1×10^{11} cycles) and the test temperature. For DUT-B, C, and D, ΔV_{th} became larger as the test temperature decreased. On the other hand, DUT-A exhibited an increase in ΔV_{th} toward lower temperatures, as seen in the other devices, but uniquely also showed an increase in ΔV_{th} at higher temperatures.

The V_{th} drift caused by AC-BTI may be explained using two main mechanisms: the Photon-Assisted Electron Injection model (Model A) [3-4] and the Recombination Enhanced Defect Reaction model (Model B) [5-7].

Both models attribute the origin of ΔV_{th} to the recombination of electrons and holes via SiC/SiO_2 interface traps that occurs during gate switching (from accumulation to inversion). However, they differ in the proposed energy transfer process: Model A attributes the effect to photons generated during recombination, while Model B considers the role of phonons produced in these reactions.

According to these models, the larger ΔV_{th} observed at lower temperatures in this study can be explained by the longer release time of holes trapped at the interface, reducing the number of holes released before recombination with electrons. This leads to more recombination events and, consequently, more electrons with sufficient energy to exceed the conduction band offset are injected into the gate oxide, where they are captured by oxide traps, resulting in a greater ΔV_{th}, as described in Model A. Since photon generation is essentially temperature-independent, this behavior is consistent with the photon-assisted mechanism in Model A. On the other hand, the notable increase in ΔV_{th} at higher temperatures, observed in DUT-A, may be better explained by Model B, in which enhanced phonon generation at high temperatures promotes the formation of additional interface defects, resulting in the increased ΔV_{th}.

Importantly, it is possible that both photon-assisted and phonon-assisted mechanisms are influencing ΔV_{th} simultaneously, with their relative contributions varying according to temperature. At lower temperatures, the photon-related process may dominate, consistent with the observed increase in ΔV_{th} across most devices in the low temperature range. In contrast, at higher temperatures, the increased presence of phonons may enhance the recombination enhanced defect reaction, leading to additional degradation in devices such as DUT-A.

Furthermore, the extent to which each mechanism contributes to device degradation appears to depend on the specific device, likely due to variations in structure, processing conditions, or interface state densities among the tested MOSFETs. As a result, the relative impact of photon- and phonon-related mechanisms—and consequently, the temperature dependence of ΔV_{th} —can vary depending on both the device and the temperature range. Since our study did not specifically separate the effects of device structure, this hypothesis remains under consideration and will require further research to be fully validated. These results thus highlight the unique interplay between these processes in the tested devices under the experimental conditions, emphasizing the necessity of evaluating AC-BTI reliability in SiC MOSFETs across both low and high temperature environments.

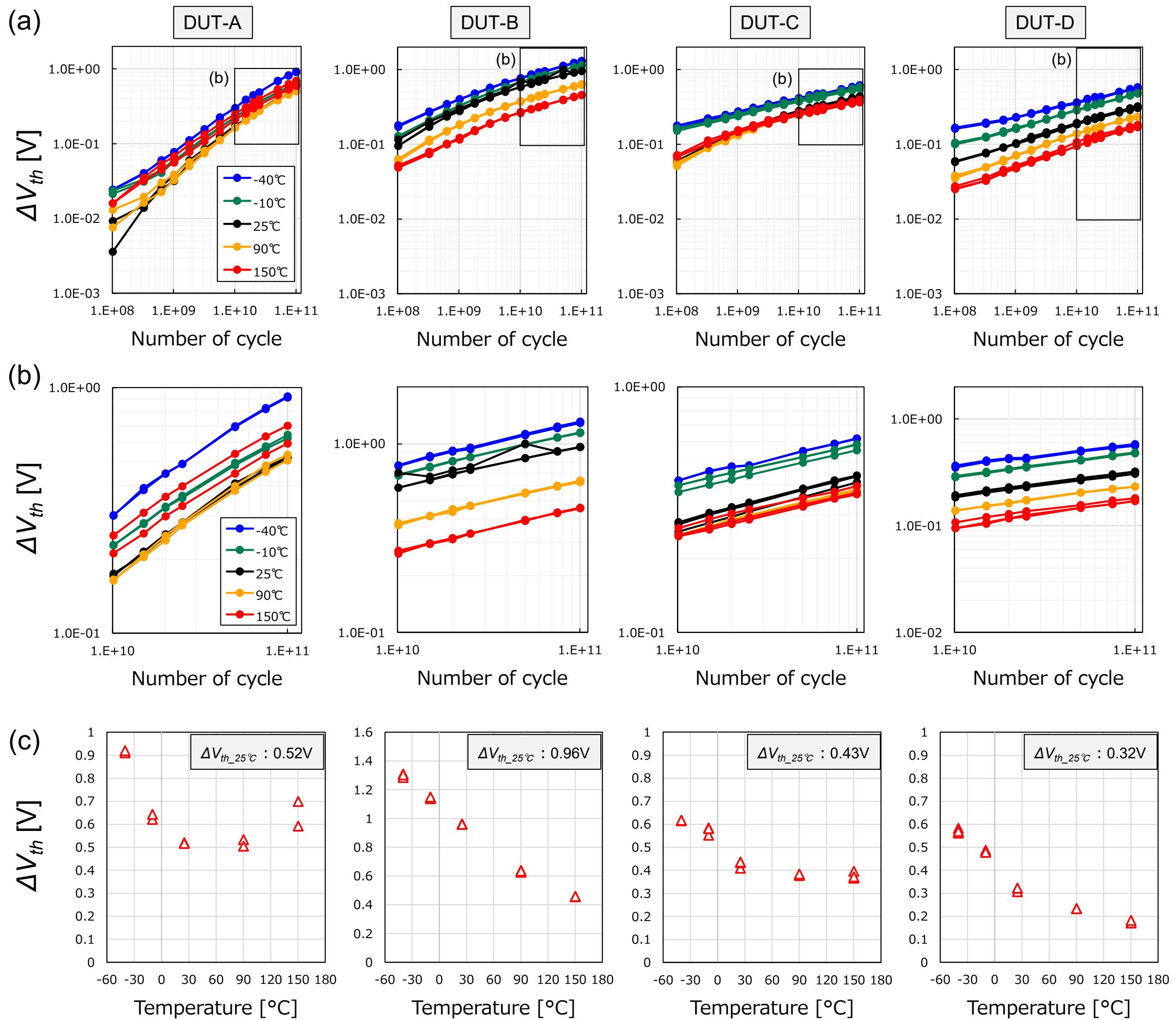

Fig. 3. AC-BTI test results at various temperatures for each DUT. (a) ΔV_{th} as a function of number of AC stress cycle. (b) Zoomed-in image of the region highlighted by the square in (a). (c) Relationship between ΔV_{th} at the end of the test (1×10^{11} cycles) and the test temperature. The value indicated in the figure represents the mean ΔV_{th} tested at 25°C.

Conclusions

In this study, the temperature dependence of ΔV_{th} caused by AC-BTI was investigated for four commercially available SiC MOSFETs over a wide temperature range, including sub-room temperatures. Most devices exhibited larger ΔV_{th} at lower temperatures, while one device showed increased drift also at high temperatures, indicating that the ΔV_{th} behavior is device-dependent and likely influenced by intrinsic factors such as structural and interface characteristics.

The results highlight that limiting reliability testing to temperatures above room temperature may overlook worst-case degradation scenarios, as significant drift can occur at lower temperatures. These findings emphasize the importance of conducting AC-BTI tests covering a broad temperature range to ensure accurate assessment of SiC MOSFET reliability in practical applications.

The measurement variability of V_{th} in this study was within 10mV, indicating good repeatability under controlled measurement protocol and temperature conditions. However, as the number of tested devices was limited (N = 2 or 3), a broader evaluation of device-to-device variation will be addressed in future studies.

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