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Reliability Challenges of SiC MOSFETs under Continuous Dual-Bias Stress in EV Applications

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Abstract. This study investigated the reliability challenges of SiC MOSFETs under continuous dual-bias stress conditions in electric vehicle (EV) applications. Accelerated dual-bias time-dependent dielectric breakdown (DB-TDDB) tests were performed on 1.2kV SiC MOSFETs by applying a negative gate-source voltage and a high drain-source voltage simultaneously. Experimental analysis and TCAD simulations revealed a nonlinear coupling effect between gate and drain biases, leading to a spatial relocation of the maximum gate oxide electric field under dual-bias conditions. An improved dual-acceleration-factor E-model was proposed to characterize this behavior. Based on this model, the projected lifetime at 1 ppm failure rate is 5.11×10^{13} hours, exceeding the 20-year automotive standard (AEC-Q101) by several orders of magnitude. Furthermore, failure analysis identified edge-thinning and JFET-region effects as two primary degradation mechanisms affecting gate oxide reliability, and corresponding process and design optimizations are proposed to mitigate this vulnerability. The findings offer critical insights for improving the reliability of SiC MOSFETs in EV applications under prolonged dual-bias stress.

Introduction

Silicon carbide metal-oxide-semiconductor field-effect transistors (SiC MOSFETs) have become the preferred choice for electric vehicle (EV) traction inverters owing to their exceptional electrical and thermal properties [1, 2]. High temperature reverse bias (HTRB), high temperature gate bias (HTGB), and constant-voltage time-dependent dielectric breakdown (TDDB) testing represent standard methodologies for assessing the reliability and lifetime of SiC MOSFETs. However, these conventional approaches typically evaluate individual stress factors in isolation, critically failing to account for the simultaneous application of drain-source and gate-source bias voltages that SiC MOSFETs experience during the switching-off duration in traction inverter applications. The conventional methodologies neglect the coupled effects arising from the simultaneous application of gate and drain biases, leading to a significant gap in understanding degradation mechanisms and accurate lifetime modeling under combined electrical stress conditions.

Furthermore, in practical applications such as the sentry mode of some EVs, SiC MOSFETs are required to endure prolonged periods blocking high bus voltages while parked. This significantly extends the device's actual operational duration. Consequently, it is imperative to reassess SiC MOSFET reliability and lifetime predictions based on these actual operational conditions in EVs.

In this study, the lifetime characteristics of 1.2 kV SiC MOSFETs (Fig. 1(a)) were investigated through dual-bias time-dependent dielectric breakdown (DB-TDDB) testing. By integrating experimental results with TCAD simulations, an improved dual-acceleration-factor E-model was established for lifetime prediction under dual-bias conditions. Failure analysis further identified distinct gate oxide failure locations that correlated with different real-time monitored drain-source leakage current (I_{DSS}) trends, significantly advancing the understanding of degradation mechanisms under dual-bias stresses.

Experiments and Results

The devices used in this study are 1.2 kV/16 mΩ rated planar MOSFETs packaged in TO-247. The fabrication process and device structure, previously reported in literature [6], are illustrated in Fig. 1(a). To investigate dual-bias stress mechanisms, reverse drain-source bias and negative gate voltage were applied to the device under test (DUT). The DB-TDDB test configuration is shown in Fig. 1(b). Prior to the main experiment, gate oxide V-ramp characterization was performed to determine the negative gate breakdown voltage which was -50 V at a leakage current threshold of 1 mA, as shown in Fig. 2(a). Accordingly, 90% of this value (-45 V) was selected as the aging condition. During testing, a negative gate-source voltage (V_{GS} = -45 V) was applied to the DUT while maintaining V_{DS} at 880 V (matching the actual bus voltage in EV traction inverters) at 175 °C. Device failure was identified by monitoring the drain leakage current (I_{DSS}) behavior, which was characterized by either a sudden increase or a drop to zero (indicating fuse burnout).

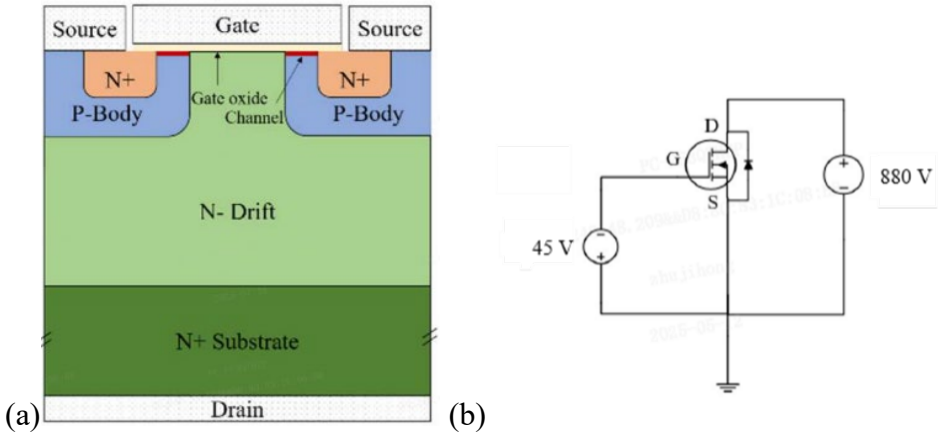


Fig. 1. (a) Structure of SiC MOSFET. (b)Test circuit for dual-bias TDDB test.

Complementary TDDB characterization was also conducted under identical gate bias condition (V_{GS} = -45 V, T_j = 175 °C) for comparison. The results clearly demonstrate that the single-stress TDDB lifetime is significantly longer than that under DB-TDDB, confirming that the dual-stress condition (with additional reverse bias voltage applied) accelerates device degradation. To determine the temperature acceleration factor, constant-voltage TDDB tests (V_{GS} = +45 V) were performed at different temperatures (T_j = 125 °C, 150 °C, and 175 °C). The Weibull distributions of the time-to-breakdown (t_{BD}) are shown in Fig. 2(b). Each test group comprised 60 samples, and testing continued until a cumulative failure rate of at least 63% was reached (corresponding to failure in 38 devices).

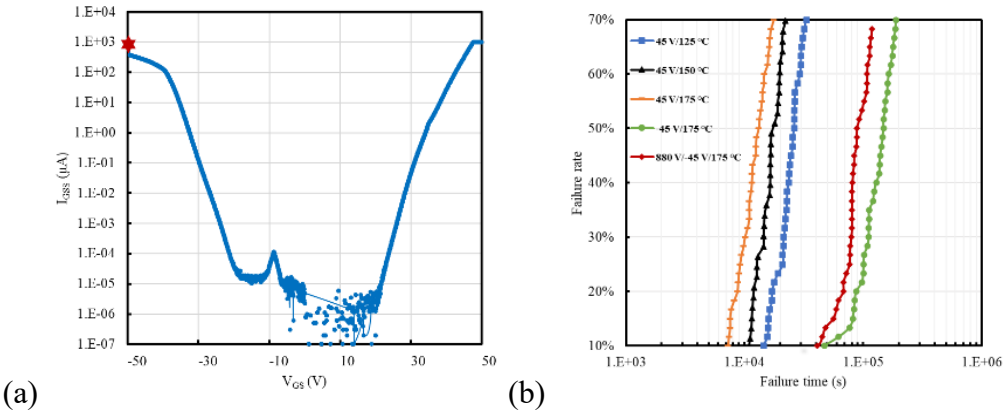


Fig. 2. (a)The gate oxide breakdown characteristics. (b)Weibull distributions of t_{BD} under accelerated stress conditions.

TCAD Simulation and Lifetime Modeling

To characterize gate oxide stress states under various accelerated conditions, Silvaco TCAD simulations were performed to analyze the gate oxide electric field distribution under different V_{GS} and V_{DS} combinations. The simulations revealed two distinct patterns: (1) Under standard reverse bias conditions, the maximum gate oxide electric field (E_{max}) was localized in the JFET region; (2) When applying the proposed DB-TDDB stress framework, E_{max} spatially shifted to the source region, as quantitatively demonstrated in Fig. 3.

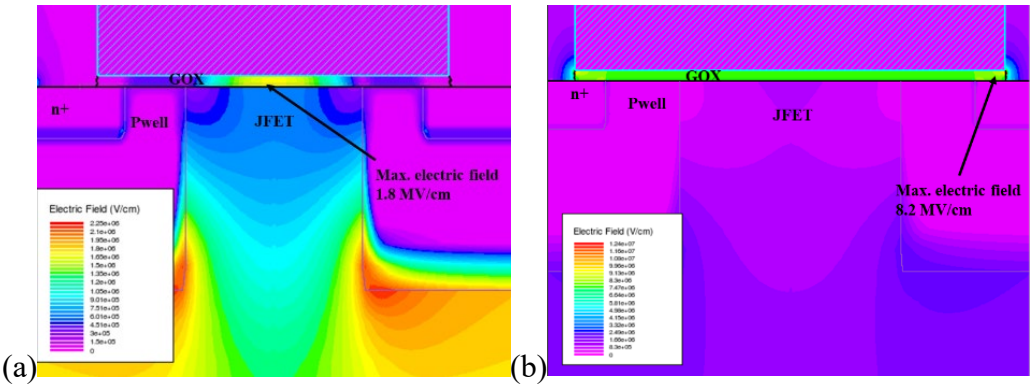


Fig. 3. Simulation of the gate oxide field distribution under (a) standard reverse bias situation (V_{DS} = 880 V) and (b) dual-bias condition (V_{DS} = 880 V, V_{GS} = -45 V).

This spatial redistribution of E_{max} indicates that dual-bias operation induces a nonlinear field-coupling effect between the gate and drain voltages. To account for this interaction, we developed a dual-acceleration-factor E-model:

$$\mathrm{TTF} = A_0 * \exp\left(\frac{E_a}{\mathrm{kT}}\right) * \exp(-\gamma_1 E_{ox}) * \exp(-\gamma_2 V_{DC}) \,. \tag{1}$$

Given the computational complexity of directly deriving the gate oxide electric field from drain voltage, an empirical approach was adopted to quantify the voltage acceleration factor. In this model, A_0 is a constant, while E_a represents the temperature acceleration factor. The parameters γ_1 and γ_2 correspond to the acceleration factors for gate-voltage and drain-bias, respectively. Notably, the activation energy depends on the bond dissociation energy of the gate oxide under standard Boltzmann thermal process, so we obtained E_a using TDDB tests at different temperatures [7]. Acceleration coefficients were quantified through both single and dual-bias TDDB tests:

- Activation energy: E_a = 0.532 eV
- Gate-voltage acceleration factor: γ_1 = 3.9 cm/MV
- Drain-voltage acceleration factor: γ_2 = 0.5 kV^{-1}

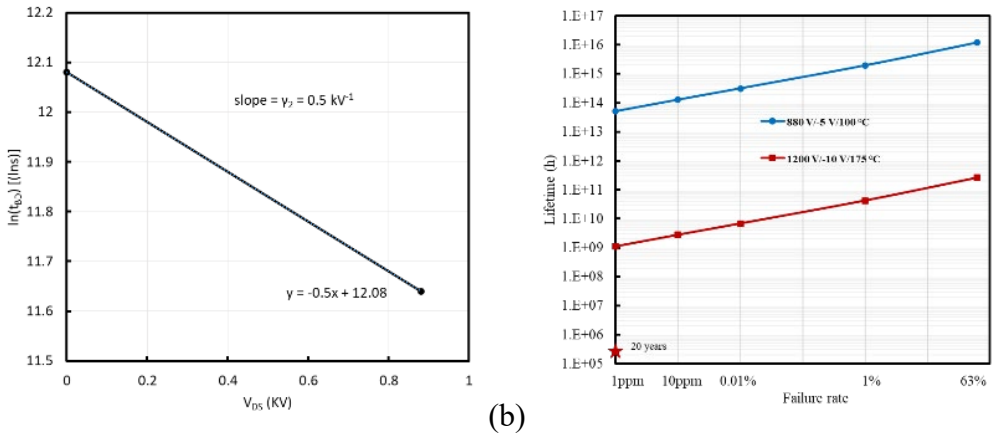
Weibull analysis (shape parameter β = 2.52) enabled lifetime extrapolation:

$$\frac{t_q}{t_p} = \left[\frac{\ln(1-F(t_q))}{\ln(1-F(t_p))}\right]^{\frac{1}{\beta}}. \tag{2}$$

This study primarily focused on two critical operational scenarios: the actual operating equivalent condition (V_{DS} = 880 V, V_{GS} = –5 V, T_j = 100 °C) and the maximum rating condition (V_{DS} = 1200 V, V_{GS} = –10 V, T_j = 175 °C), as summarized in Table 1. Notably, even under the maximum rating scenario, the predicted lifetime at the 1 ppm failure level (1.1 × 10^9 hours) substantially exceeds the 20-year service life requirement specified in the AEC-Q101 Rev-H qualification standard for automotive power electronics. The complete experimental matrix, including the extracted time-to-failure (TTF) at 63% failure level and corresponding fitting results, is comprehensively summarized in Table 1 and graphically represented in Fig. 4.

Table 1. The test matrix and fitting results.

Groups	Test conditions	T63 [h]	T1% [h]	T0.01% [h]	T10 ppm [h]	T1 ppm [h]
A	V_{DS} = 880 V, V_{GS} = -40.5 V, T_j = 175 ℃	31.5	/	/	/	/
B	V_{DS} = 0 V, V_{GS} = -40.5V, T_j = 175 ℃	49.3	/	/	/	/
C(fitting)	V_{DS} = 880 V, V_{GS} = -5V, T_j = 100 ℃	1.2×10^{16}	2.0×10^{15}	3.2×10^{14}	1.3×10^{14}	5.1×10^{13}
D(fitting)	V_{DS} = 1200 V, V_{GS} = -10V, T_j = 175 ℃	2.6×10^{11}	4.32×10^{10}	6.8×10^{9}	2.8×10^{9}	1.1×10^{9}



(a) (b)

Fig. 4. (a) Field-accelerated lifetime extrapolation based on the V_{DS}. (b) Cumulative failure rates corresponding to operation lifetime.

Failure Mechanism Analysis

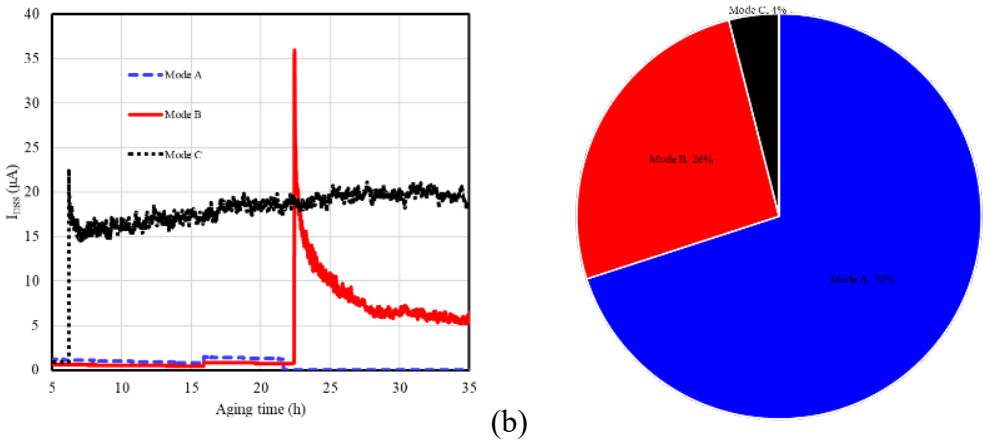
During the dual-bias testing, the real-time I_{DSS} of each DUT was continuously monitored with three distinct failure modes identified:

Mode A: The I_{DSS} abruptly drops to zero.

Mode B: The I_{DSS} exhibits a sharp increase followed by a gradual decline.

Mode C: The I_{DSS} shows a progressive increase without recovery.

Representative real-time I_{DSS} characteristics for each failure mode are illustrated in Fig. 5(a). Statistical analysis of the failure distribution revealed that Mode A accounted for 70% of cases (35 out of 50), Mode B for 26% (13 out of 50), and Mode C for 4% (2 out of 50), as summarized in Fig. 5(b).



(a) (b)

Fig. 5. (a) Inline I_{DSS} current with different failure modes. (b) The proportions of different failure modes.

To elucidate the underlying failure mechanisms associated with each mode, comprehensive failure analysis was conducted on all three failure types. This established a clear correlation between the observed electrical characteristics and distinct physical failure locations within the gate oxide. For the dominant Mode A (70% occurrence), failures are located at the edge of the active area, confirming this region as a primary reliability weakness in the chip structure. Cross-sectional TEM imaging was performed to further investigate the physical origin of this phenomenon. Quantitative analysis revealed a gate oxide thickness of 47.1 nm at the active area edge, significantly thinner than the 50 nm measured in the center region (Fig. 6). This thickness variation directly correlates with local electric field enhancement in the edge region, accounting for breakdown more often here. These findings are consistent with the established edge effect in power devices [8], wherein field crowding at structural discontinuities amplifies local electric fields.

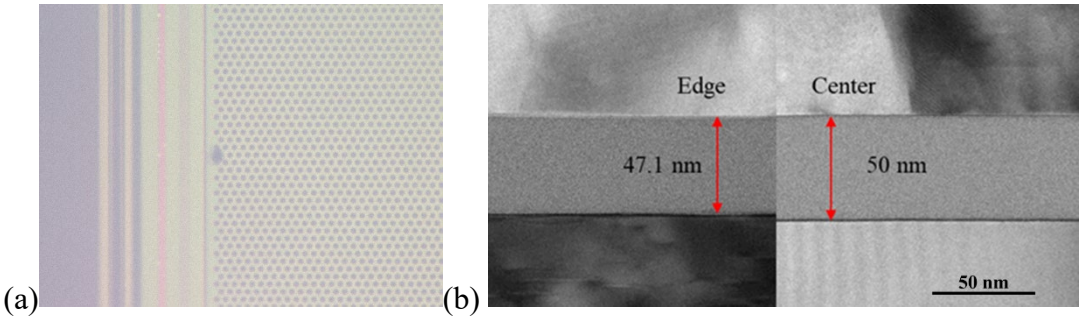


Fig. 6. (a)The failure location of Mode A. (b)TEM image of the gate oxide at the edge and the center of the active area.

For Mode B and Mode C, each occurred in distinct regions that matched their electrical behaviors. Mode B failures occurred in the JFET region, while Mode C failures originated in the channel, as schematically depicted in Fig. 7.

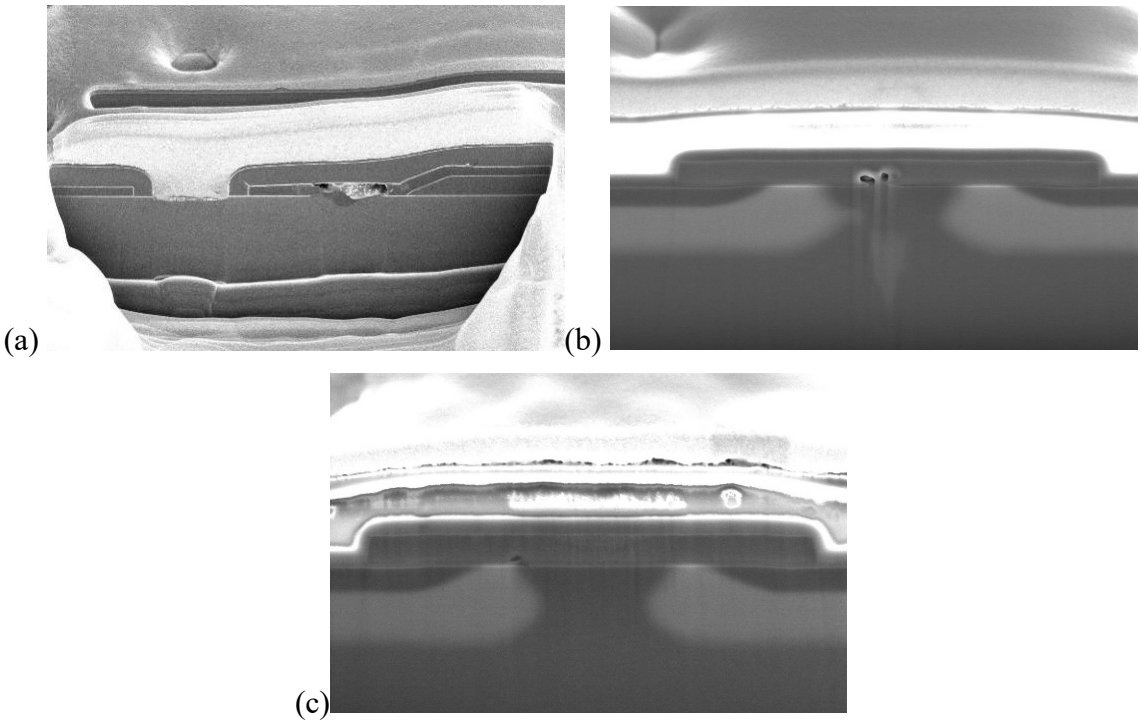


Fig. 7. Image of the failure locations of (a) Mode A (b) Mode B and (c) Mode C.

The electrical characteristics of gate oxide failures exhibit location-dependent mechanisms governed by fundamental physical processes. Under dual bias conditions, hole tunneling occurs at the semiconductor-oxide interface. This creates distinct operational regimes: A very thin inversion

layer in the n-type SiC JFET region contains only a small number of holes, whereas majority carrier holes accumulate at the P-well/SiO_2 interface in the channel region, as shown in Fig. 8. This physical asymmetry therefore leads to contrasting failure manifestations. Breakdown in the channel region (Mode C) exhibits a continuously increasing current characteristic due to the abundance of majority carriers. Conversely, in the JFET region (Mode B), the absence of holes creates a non-replenishable charge condition at the n-SiC/SiO_2 interface, resulting in the observed gradual leakage current decay following breakdown.

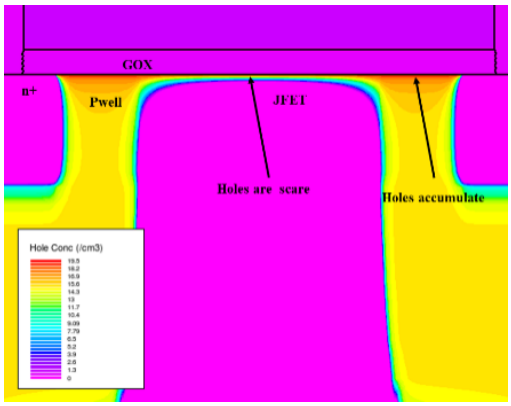


Fig. 8. Holes distribution in a cell under dual stress conditions.

For failure Mode A (active area edge breakdown), analysis identified a primary cause: gate oxide thickness non-uniformity resulting from pattern-dependent oxidation rate variations during thermal oxidation. Process improvements aimed at improving oxidation uniformity, including optimized temperature ramping rates and ambient gas flow dynamics, could reduce Mode A occurrence by enhancing gate oxide thickness homogeneity. In contrast, failure Mode B (JFET region breakdown) originates mainly from inherent electric field crowding in the highly doped JFET region, where simultaneous drain stress and gate bias cause localized field enhancement. Design optimizations such as doping profile adjustments and gate structure modifications can effectively mitigate field crowding, thereby reducing peak field strength. Experimental validation has demonstrated that combining both process and design optimizations can collectively address 96% of the identified reliability weaknesses. Future work will focus on:

- Advanced oxidation process control for sub-nanometer-level gate oxide uniformity.
- TCAD-guided design optimization of JFET structures.

Conclusion

In conclusion, this study established an enhanced DB-TDDB methodology that incorporates both negative gate-voltage effects and reverse-bias coupling stresses under actual operational conditions. Through comprehensive gate oxide lifetime testing using this framework, key acceleration factors were quantitatively extracted (γ_1 = 3.9 cm/MV for gate voltage, γ_2 = 0.5 kV^{-1} for drain bias). Multivariable stress analysis yielded a projected operational lifetime under combined electrothermal stress conditions. Failure mode analysis revealed distinct spatial distributions of degradation mechanisms: the predominant failure mode (70% occurrence) localized at the active area edge, while 26% failures occurred in the JFET region. These reliability limitations can be addressed via process optimization and design improvements. The proposed methodology and associated findings provide critical insights for developing more reliable SiC power devices for automotive applications.

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