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Gate Oxide Stability and Degradation Modes of Next Generation SiC MOSFETs

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Abstract. The long-term reliability of silicon carbide MOSFETs is critically influenced by the stability of the gate oxide, which is susceptible to degradation due to high defect densities at the oxide-semiconductor interface. This work presents a comprehensive investigation of gate oxide degradation in next-generation SiC MOSFETs, comparing planar and trench device topologies under both static and dynamic stress conditions. Time-dependent dielectric breakdown measurements reveal degradation phases that are strongly dependent on device topology. Comparative analysis of various gate stress methodologies shows that dynamic switching stress exerts a more pronounced impact on trench devices than on planar devices. Thus, highlighting the need of tailoring reliability test protocols to the specific device topology, rather than adopting a generalized approach.

Introduction

Silicon Carbide (SiC) MOSFETs have emerged as vital components in high-power and high-temperature applications, offering significant advantages over traditional silicon-based devices [1]. Particularly, their superior material properties, including higher breakdown voltage, lower on-resistance, and enhanced thermal conductivity, enable efficient operation under high voltage, high temperature, and fast switching conditions [2], [3]. These characteristics make SiC MOSFETs particularly attractive for demanding applications such as electric vehicles, renewable energy systems, and industrial power conversion. Despite its performance benefits, the long-term reliability of SiC MOSFETs remains a critical concern, specifically regarding gate oxide stability. The gate oxide in SiC devices are inherently more prone to degradation due to the high defect density at the SiC/SiO_2 interface compared to their silicon counterparts [4]. This susceptibility leads to threshold voltage (V_{th}) instability and gate oxide degradation, resulting in increased conduction losses, elevated leakage currents, parasitic turn-on events, and even premature dielectric breakdown, which ultimately compromising device performance, reliability, and system safety. The reliability of SiC MOSFETs is governed by both static and dynamic stresses acting on the gate oxide. Static stresses, such as those applied during time-dependent dielectric breakdown (TDDB) and high-temperature gate bias (HTGB) tests, accelerate intrinsic dielectric degradation and charge trapping under constant high electric fields and elevated temperatures, ultimately determining oxide lifetime and early failure risk. Additionally, dynamic stresses during real switching operation introduce degradation mechanisms that static stress tests cannot capture, most notably bias temperature instability (BTI) and gate switching instability (GSI). These mechanisms drive progressive threshold voltage drift through defect charging and recombination-enhanced reactions [5], [6], [7]. Recent studies have shown that BTI and GSI are the dominant mechanisms contributing to V_{th} drift in SiC MOSFETs. BTI occurs under prolonged DC gate bias at elevated temperatures and involves charge trapping at the SiC/SiO_2 interface and near-interface oxide traps. Both positive (PBTI) and negative (NBTI) stress conditions have been investigated, revealing that SiC devices exhibit larger V_{th} shifts compared to silicon MOSFETs due to higher defect densities and carbon-related traps [8], [9]. In contrast, GSI is a dynamic degradation mode observed during high-frequency bipolar gate switching, where alternating electron and hole injection triggers recombination-enhanced defect reactions (REDRs), leading to progressive and sometimes partially reversible V_{th} shifts [10], [11]. Although both BTI and GSI contribute to threshold voltage shift during

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dynamic stress testing, GSI fundamentally differs from BTI in that it is primarily governed by the cumulative number of switching events and exhibits only a weak dependence on temperature. Together with static stress effects, these dynamic phenomena critically influence the long-term reliability of SiC MOSFETs, underscoring the need for integrated assessment approaches to ensure accurate lifetime prediction and robust device design. This work investigates the degradation behavior of SiC MOSFETs under both static and dynamic stress conditions. The study encompasses planar and trench device topologies, providing a comparative analysis that highlights key similarities and differences in their stress responses.

Experimental Details

In this study, two distinct SiC MOSFET topologies were investigated: planar- and trench-type devices. An overview of the tested SiC MOSFETs is provided in Table 1. The experimental methodology incorporates both static and dynamic stress techniques to comprehensively assess gate oxide reliability. Static stress tests include TDDB and HTGB, whereas dynamic stress tests consist of dynamic gate switching (DGS). This approach enables the assessment of both intrinsic gate oxide degradation mechanisms and threshold voltage instabilities that are relevant under practical operating conditions.

Table 1. Overview of tested commercial SiC MOSFETs.

Device Type	Current Rating	Typical V_{th}	$R_{DS,ON}$
Planar	160 A	2.4 V	9 – 15 mΩ
Trench	150 A	4.4 V	8.4 – 17.6 mΩ

The devices were configured in a discrete TO-247-4L package. For each static test, 10 DUTs were allocated per device type and stress conditions. TDDB and HTGB measurements were performed using a high-temperature PCB test board equipped with multiple TO-247 sockets. This board was housed within a temperature-controlled oven to ensure stable thermal conditions during stress testing. While the setup supports the optional application of drain-source voltage, all static tests conducted in this study were performed with the drain and source terminals shorted. The modular design of the setup allows for simultaneous operation of multiple test boards, each with independently controlled voltage parameters. The DAQ system consisted of a LabJack unit interfaced with a custom measurement card populated with shunt and protection resistors. Each device was connected in parallel, with gate voltage applied through a voltage divider comprising a shunt resistor and a protection resistor. The voltage drop across shunt resistor is used to calculate the leakage current, while protection resistor limits the input voltage to the LabJack in case of dielectric failure.

For dynamic stress tests a commercial setup was used, equipped with pulsed width modulation and power stage for stress generation [12]. Here 40 DUTs were allocated per device type and stress conditions. Switching frequency was set to 300 kHz with a duty cycle of 50%. Gate-source on-state voltage ($V_{GS,ON}$) and gate-source off-state voltage ($V_{GS,OFF}$) were set according to the device data sheet recommended maximum and minimum gate voltage limit. A gate resistor of 3.9 Ω was used to ensure no over- and undershoot of the gate-source voltage. The drain was shorted to source during the stress cycle. The readout circuit measures the V_{th} followed by the drain-source on resistance ($R_{DS,ON}$). Prior to V_{th} measurement, a preconditioning sequence is applied. This begins with a 100 ms positive preconditioning pulse at the device-specific $V_{GS,ON}$, followed by a down-slope transition from 9.5 V to 0 V to determine the down-slope threshold voltage ($V_{th,down}$), during which the drain current is maintained at 10 mA. Subsequently, a 100 ms negative preconditioning pulse at the device-specific $V_{GS,OFF}$ is applied. This is followed by an up-slope transition from 0 V to 9.5 V to determine the up-slope threshold voltage ($V_{th,up}$), with a drain current of 10 mA. Finally, the on-state resistance ($R_{DS,ON}$) is measured using a drain pulse current of 10 A and the corresponding $V_{GS,ON}$ for the device.

Results and Discussion

As part of device pre-characterization, gate leakage current (I_G) measurements were performed at 175 °C until device failure, and threshold voltage values were extracted across a range of temperatures. These preliminary evaluations are essential for establishing appropriate stress conditions for subsequent long-term tests. Fig. 1(a) shows the gate leakage current obtained from planar- and trench-type devices; the trench-type SiC MOSFETs exhibit lower leakage current at the same voltage compared to planar type. This is primarily due to the lower effective electric field in trench devices, which is a result of the thicker oxide layer typically used in trench-type devices [13]. Additionally, the threshold voltages of the devices were determined prior to conducting stress tests. The transfer characteristics for both device types are plotted in Fig. 1(b), both devices show an expected negative temperature coefficient for V_{th} and a nominal hysteresis of 80 – 100 mV.

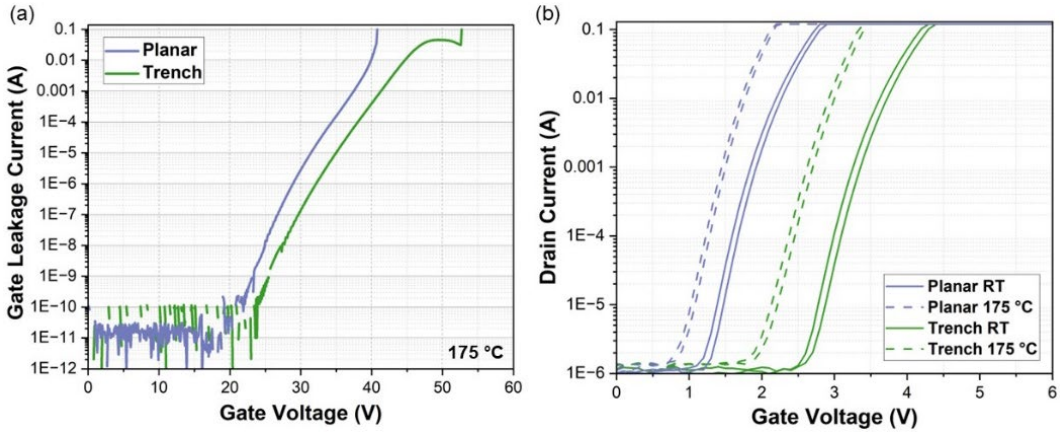

Fig. 1. (a) Gate current-voltage characteristics, and (b) Transfer characteristics, obtained from planar and trench devices.

For TDDB measurements, three distinct bias conditions were applied to each device topology, while the test temperature was consistently maintained at 175 °C. The bias conditions applied to planar-type devices were 35 V, 34 V, and 33 V, while higher biases of 45 V, 44 V, and 43 V were applied to the trench-type devices. The devices were stressed until failure, with gate leakage current continuously monitored throughout the stress duration. The oxide breakdown is characterized by an abrupt change in the measured current across each device, which corresponds to the typical time-to-failure for the device. Fig. 2(a) and Fig. 2(c) show the gate leakage current as function of time (I_G-t) for all individual MOSFETs stressed at different bias conditions for the planar- and trench-type devices, respectively. For all the stress conditions the leakage current decreases with time till the device fails. The leakage current shows a sharper decline for the higher bias values. For the planar-type devices the average time to failure shows a gradual decrease with increase in bias values. In contrast, the trench-type devices demonstrate an abrupt reduction in oxide lifetime at the highest stress condition. This behavior could suggest the activation of an additional degradation mode, which is triggered at highest applied bias value at 175 °C. Fig. 2(b) and Fig. 2(d) depict the I_G-t plot in log-log scale for planar- and trench-type devices, respectively. It is clear that there are two distinct degradation phases for both trench- and planar-types of devices. The first phase that is depicted till t_0 shows no significant change in the measured leakage current, this phase is characterized by minimal charge trapping that causes the slight decrease in the measured leakage current, and it is reported to have negligeable influence on the V_{th} and $R_{SD,ON}$ [14]. The second phase starts at the end of t_0 and lasts till the device fails (t_f), this phase is known as the 'wear-out' phase [14]. During the 'wear-out' phase the gate leakage current drops significantly, indicating a high-degree of charge trapping during this phase. This drop in the gate leakage current has been previously attributed to the build-up of electrons, which in turn results in an increase in the threshold voltage [15]. The 'wear-out' phase of the trench-type devices is notably different than the planar-type devices, it shows a significantly higher and longer decrease in leakage current until device failure. This is mainly attributed to a larger number of electron trap sites at the interface or in the dielectric layer [13], [16].

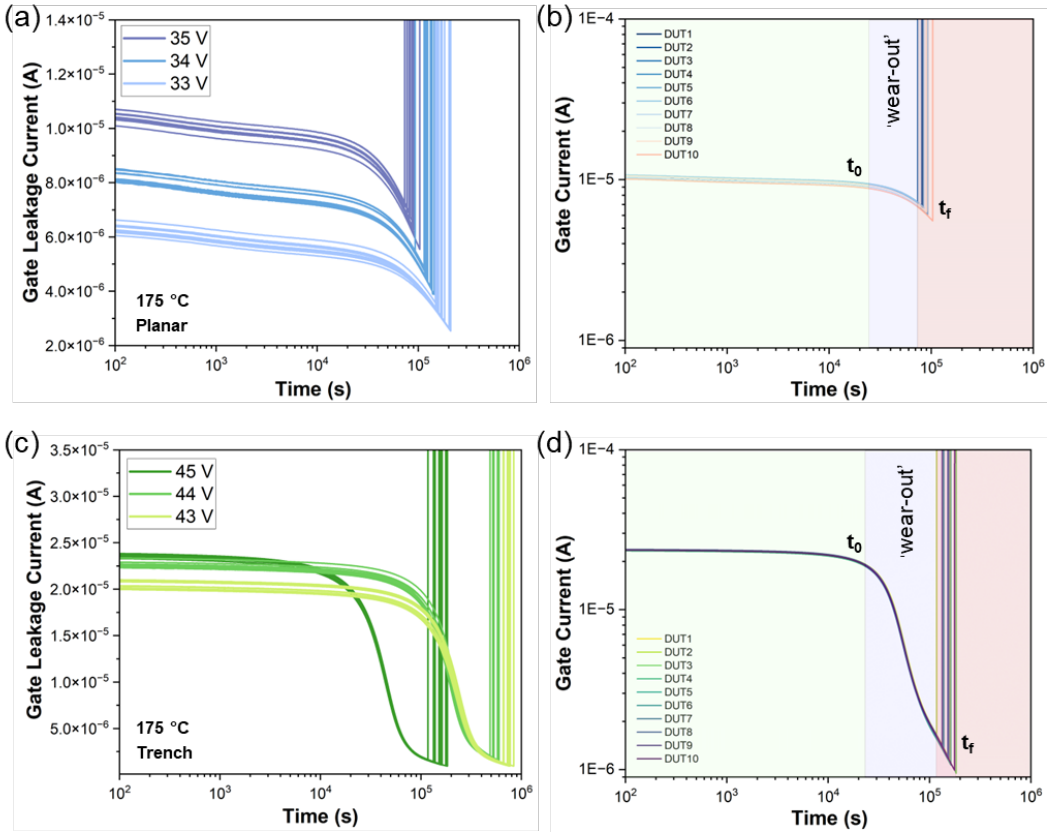

Fig. 2. Evolution of gate leakage current obtained from constant voltage TDDB at 175 °C for, (a) planar devices under different stress conditions, (b) planar device depicted in double-logarithmic plot at 35 V bias condition, (c) trench devices under different stress conditions, (b) trench device depicted in double-logarithmic plot at 45 V bias condition.

The measured time-to-failure is used to construct the Weibull plot for each bias condition. A two-parameter Weibull distribution has the cumulative density function of the following form:

$$F(t) = 1 - exp\left[-\left(\frac{t}{\eta}\right)^{\beta}\right] \tag{1}$$

This can be alternatively expressed as:

$$ln\left[-ln\left(1 - F(t)\right)\right] = \beta\, ln(t) - \beta ln(\eta) \tag{2}$$

where, b and h are the shape parameter and characteristic lifetime of the Weibull distribution [15]. A Weibull plot is obtained by plotting ln(-ln(1-F(t))) as function of time in log scale. The slope of this plot corresponds to b, while the intercept provides h. Alternatively, h is also defined as the time at which 63% of the devices fail for the given stress condition. The Weibull plot obtained from planar- and trench-type devices is shown in Fig. 3(a) and Fig. 3(c), respectively. The shape parameters from the Weibull distributions obtained from both types of devices are greater than 1, indicating the main reason for failure is aging related. The slight variations in the shape parameters across the different stress conditions could stem from the limited sample size. However, a large shift in the shape parameter that is observed for the highest stress condition for the trench-type devices could indicate a failure mode transition, as previously highlighted in the I_G-t plot for the same device type (see Fig. 2(c)). It has been previously reported that trench-type SiC MOSFET may experience accelerated failure under high bias due to localized field enhancements and trap-assisted tunneling effect [13], [17]. Further, the lifetime estimation plots are shown in Fig. 3(b) and Fig. 3(d) for planar- and trench-type devices, respectively. By plotting the h for each bias condition, a linear fit can be obtained. This fit is then used to extrapolate the intrinsic gate oxide lifetime of the devices at lower operating oxide fields. The estimated lifetime under operational stress is significantly higher for trench-type devices compared

to planar-type devices; however, this may be an overestimation caused by a failure mode transition at the highest applied bias conditions. Previous report on TDDB performed on commercially available devices highlighted the importance of not over stressing the gate oxide as this might lead to a modified failure modes that can influence the lifetime estimation [15].

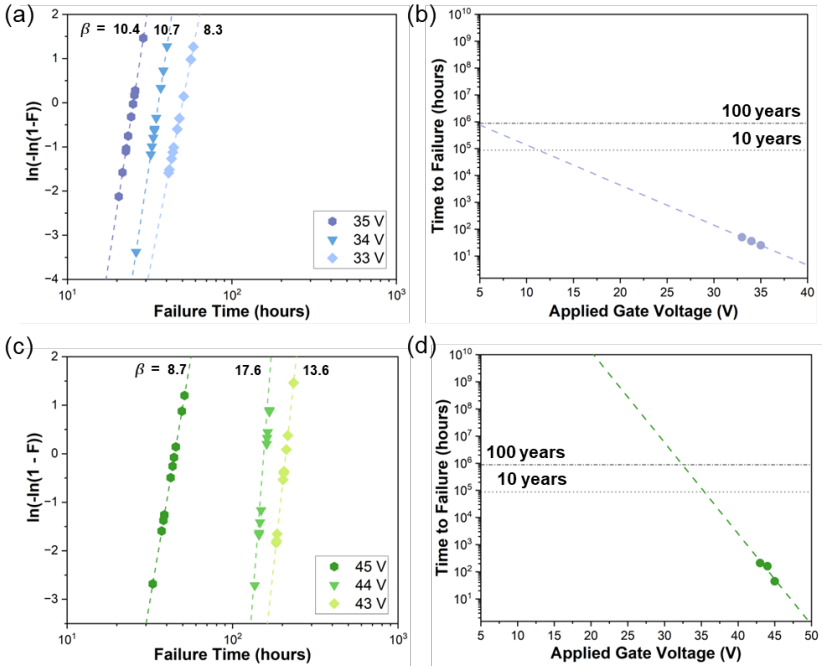

Fig. 3. (a) and (b) Weibull distribution and projected time to failure with $t_{63\%}$ for planar devices. (c) and (d) Weibull distribution and projected time to failure with $t_{63\%}$ for trench devices.

The static HTGB test was conducted to evaluate the V_{th} stability under prolonged positive gate bias stress. A constant gate bias of 25 V was applied under a temperature condition of 175 °C for a total duration of 1000 hours. The V_{th} was recorded at three intervals: prior to stress application (pre-stress), at the midpoint (500 hours), and at the end (1000 hours). Threshold voltage at 175 °C is plotted as a function of stress duration for the planar- and trench-type devices in Fig. 4(a) and Fig. 4(b), respectively. Typically, under positive gate bias stress, the V_{th} is expected to drift to higher values due to electron trapping in the gate oxide or at the SiC/SiO_2 interface [18], [19], [20]. Electrons can be trapped in pre-existing or stress-induced trap sites. It is evident from Fig. 4(a) that the planar-type devices exhibit a more pronounced V_{th} shift, with a total drift of 1.45 V over 1000 hours of stress. In contrast, the trench-type devices show a moderate V_{th} shift of 0.5 V over the same stress period. It should be noted that given both the types of devices were subjected to same gate bias, the effective electric field for planar-type device is much higher due to the thinner oxide layer. Making the planar-type device more susceptible to electron injection and trapping, thereby accelerating the V_{th} drift.

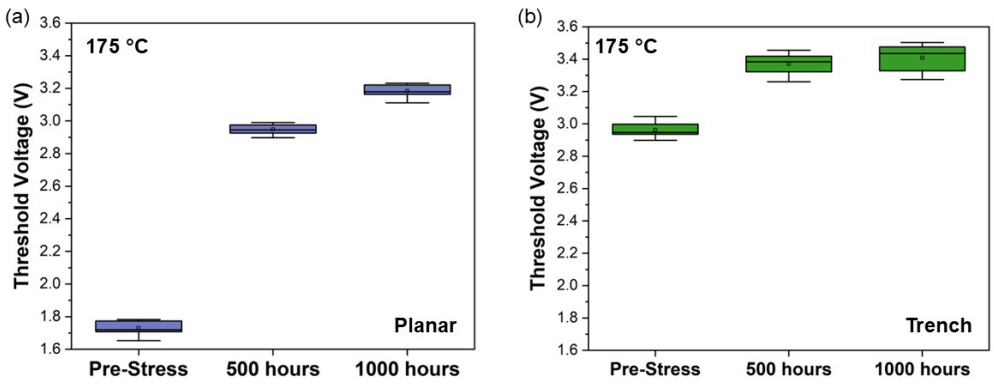

Fig. 4. Threshold voltage measured before and after static HTGB for (a) planar, and (b) trench devices.

Following static stress methods, which evaluate gate oxide reliability under constant bias conditions, it is equally important to assess device behavior under dynamic stress. In practical applications, SiC MOSFETs experience repetitive gate voltage transitions rather than steady-state bias. DGS was used to capture degradation mechanisms that are pertinent to dynamic stress.

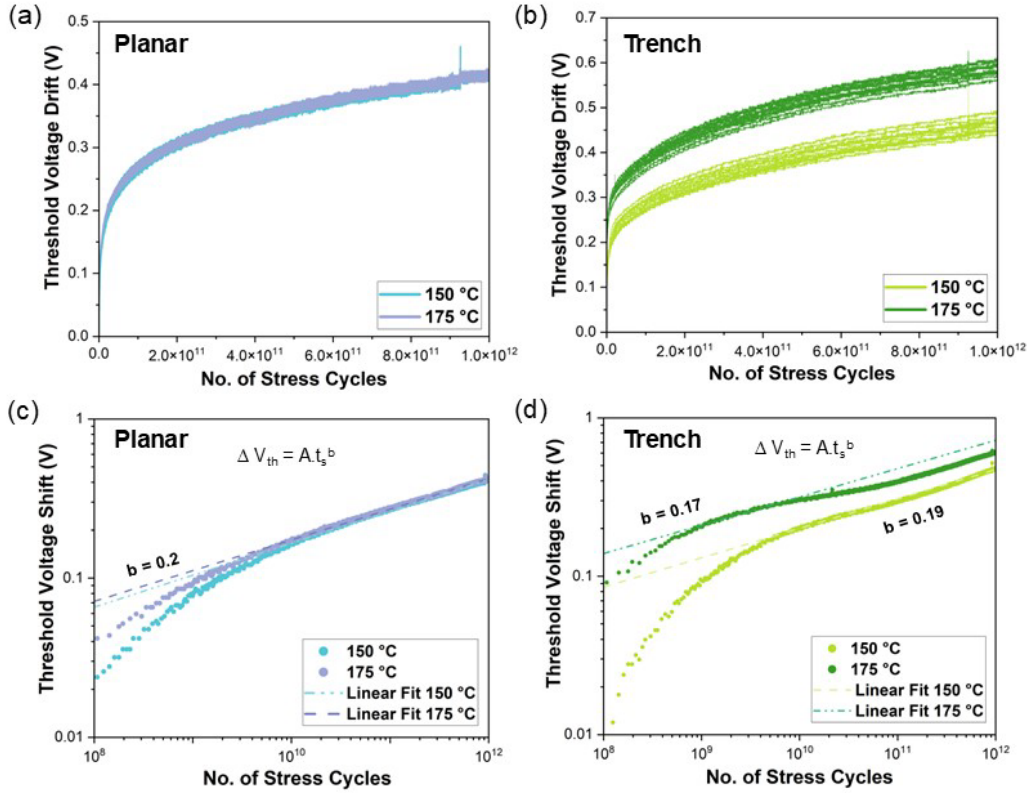

Fig. 5. Threshold voltage drift as a function of stress cycles measured at 150 °C and 175 °C for (a) planar devices, (b) trench devices, (c) planar devices depicted in double-logarithmic plot, and (d) trench devices depicted in double-logarithmic plot.

Two different temperature conditions were used for the DGS measurements, specifically 150 °C and 175 °C. For each temperature, 40 devices were tested per device type. The planar-type devices were stressed with $V_{GS,ON}$ = + 19 V and $V_{GS,OFF}$ = − 8 V. Fig. 5(a) depicts the V_{th} drift as a function of number of stress cycles for planar-type devices. The V_{th} drift progression for the planar-type devices is similar for both temperatures, accounting for a total drift of 0.4 V. Whereas the V_{th} drift for the trench-type devices demonstrates a clear distinction between the two temperatures, as shown in Fig. 5(b). Fig. 5(b) depicts the V_{th} drift as a function of number of stress cycles, here the devices were stress with $V_{GS,ON}$ = + 25V and $V_{GS,OFF}$ = − 11V. For the higher temperature the V_{th} drift was more severe resulting in a total V_{th} drift of 0.56 V. Additionally, no substantial drift in the $R_{DS,ON}$ value was observed after the total stress period for either device type. Indicating the V_{th} drift does not have a significant impact on the $R_{DS,ON}$ value. Fig. 5(c) and Fig. 5(d) illustrate the V_{th} drift as a function of stress cycles for different temperatures in a double-logarithmic plot for planar- and trench-type devices, respectively. The total V_{th} drift is expected to be composed of BTI and GSI parts, where the GSI component is dependent on the cumulative number of switching cycles [10], [21]. Whereas the BTI component is temperature dependent and frequency independent [10], [11]. For the given stress conditions, we observed the planar-type devices only display the BTI component, which can be fitted by power law exponent of 0.2. For the trench-type devices a deviation from the BTI component is observed at higher switching cycles, predominantly noticeable for the higher temperature. The BTI component has a power law slope of 0.17 and 0.19 for 175 °C and 150 °C, respectively. The deviation observed for the trench-type devices at higher switching cycles has a slope of lower than 1, this slope is lower than the expected power law slope of unity for the GSI component [10].

Summary

This study provides a detailed assessment of gate oxide stability and degradation mechanisms in next-generation SiC MOSFETs, comparing planar and trench topologies under static and dynamic stress conditions. The results demonstrate that trench-type devices generally exhibit superior threshold voltage stability under static stress conditions, this is most likely due to the thicker gate oxide used in trench-type devices in comparison to planar-type devices. Thus, calibrating the stress based on oxide thickness is crucial. Additionally, trench-type devices show higher predicted lifetime under operating conditions. However, this can be an overestimation from including high-bias stress in TDDB that leads to a shift in degradation mode. Trench-type devices are more susceptible to accelerated failure at extreme bias, likely due to localized field effects. Dynamic stress testing indicates the dominant contributor to the total V_{th} drift is the BTI component. Planar-type devices show minimal temperature dependence in V_{th} drift, whereas trench-type devices show a pronounced temperature dependence, resulting in higher V_{th} drift compared to static stress conditions. Furthermore, at higher switching cycles, the V_{th} drift in trench-type devices deviates from the expected BTI behavior, suggesting the on-set of additional degradation mechanisms. These findings underscore the importance of adapting reliability assessment methodologies to specific device topologies, rather than relying on generalized approaches, to ensure robust design and accurate lifetime prediction for SiC MOSFETs in advanced power electronics applications.

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