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Impact of Packaging on Discrepancy of Datasheet Static Measurements of SiC Power MOSFETs in Bare Dies and TO-247 Packaged Form-Factors

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Abstract. This paper presents a comparative analysis of 1200 V Silicon Carbide (SiC) MOSFETs characterized at bare die level and in TO-247 packaging. Static parameters including transconductance (g_m), drain leakage current ($I_{DS\text{-}OFF}$), output (I_{DS}-V_{DS}) and transfer characteristics (I_{DS}-V_{GS}), gate threshold voltage ($V_{GS(th)}$) and on-state resistance ($R_{DS(on)}$) are examined. Results show that the TO-247 package introduces parasitic resistance/inductance and higher thermal impedance, leading to disrupted g_m, though lower leakage $I_{DS\text{-}OFF}$, shifted $V_{GS(th)}$, and elevated $R_{DS(on)}$. The study quantifies the discrepancy between intrinsic die behavior and packaged device performance, underscoring the need to de-embed packaging effects for accurate device modelling and optimization.

Introduction

SiC MOSFETs are increasingly adopted in high-voltage, high-frequency power converters due to their high breakdown field, wide bandgap, and low specific on-resistance [1]. Device datasheets, however, are either derived from discrete packaged devices, where bond-wire inductance, lead-frame resistance, and limited thermal conduction influence measured performance, or on bare die which does not represent the actual final product. These parasitic and thermal effects in packaging could distort key device parameters such as g_m, $V_{GS(th)}$, and $R_{DS(on)}$, complicating the extraction of intrinsic device properties required for physics-based modelling [2].

To address this, this paper presents a direct comparison made between bare die and TO-247 packaged SiC MOSFETs. Bare die measurements, performed with Kelvin probing and controlled chuck temperature, isolate intrinsic semiconductor behavior, while TO-247 results reflect application-level operation under parasitic and thermal constraints. The discrepancies observed provide insights into the extent of packaging-induced artefacts and their relevance for both device benchmarking and converter design.

In short, we have characterized 1200 V Silicon Carbide (SiC) power MOSFETs from COOLCAD, to measure potential discrepancies that may arise between measurements performed on bare die versus those taken from devices in TO-247 packaging [3], due to the introduction of parasitic elements and thermal impedance in the package [4, 5].

Measurements Set-Up

The device characterizations were performed using a Keysight B1505A Power Device Analyzer/Curve Tracer, enabling high-voltage, high-current measurements with precision parameter extraction. For the TO-247 packaged devices, the N1265A high-current expander fixture was used as in Fig. 1, providing low-inductance Kelvin connections suitable for discrete characterization. For the bare die measurements, the devices were mounted on an MPI TS2000-HP semi-automatic on-wafer prober as in Fig. 2, which allows direct probing of source, drain, and gate pads with high accuracy and controlled chuck temperature.

The two setups introduce distinct measurement environments. The expander fixture for the TO-247 inevitably incorporates package-related parasitics, including bond-wire inductance, lead-frame resistance, and finite thermal conductivity through the case-to-ambient path. These effects manifest as increased $R_{DS(on)}$ and threshold voltage shifts due to higher influence of junction temperature. By contrast, on-wafer probing minimizes electrical parasitics via Kelvin contacts placed directly on the device pads and ensures efficient thermal management through the temperature-controlled chuck, thereby yielding values closer to the intrinsic device behavior.

Although any measurement system introduces small offsets, such as milliohm-level contributions to $R_{DS(on)}$ from cabling resistance or microamp-level offsets in leakage current from instrument resolution or equipment calibration precision, these errors are less significant compared to the impact of device packaging. For example, the TO-247 package can increase $R_{DS(on)}$ due to series resistance and self-heating. Therefore, the observed discrepancies between bare die and packaged devices are primarily dominated by the parasitic and thermal constraints imposed by the package itself.

Fig. 1. The Keysight B1505A Power Device Analyzer/Curve Tracer, enabling high-voltage, high-current measurements. For the TO-247 packaged devices, the N1265A expander fixture is used.

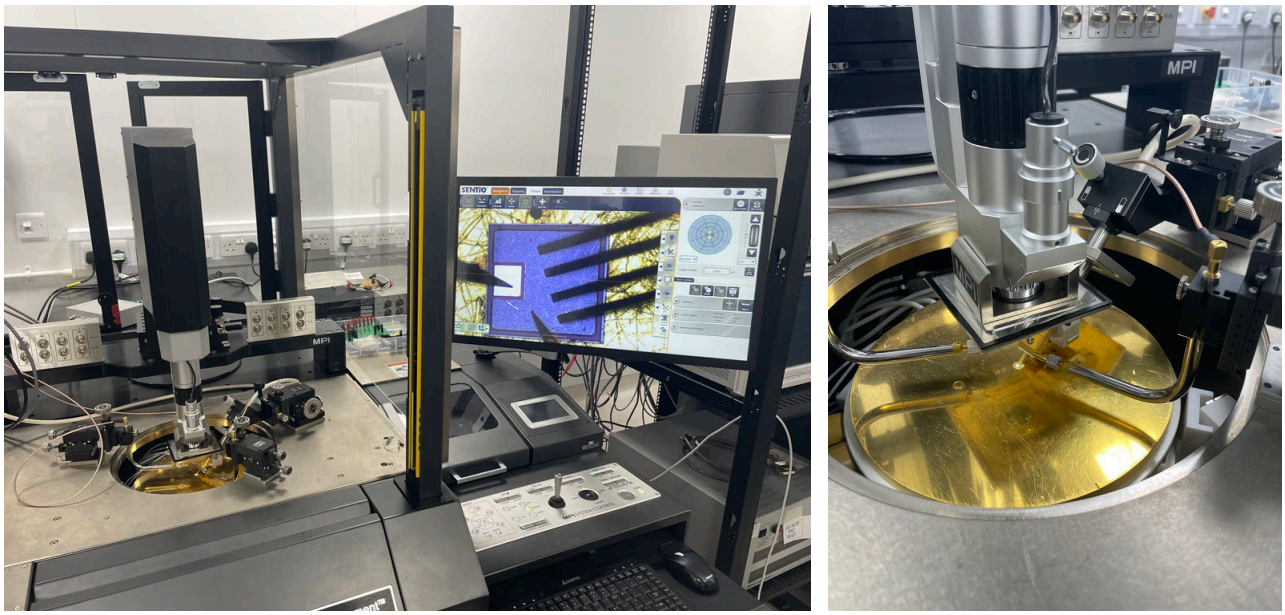

Fig. 2. The Keysight B1505A Power Device Analyzer for the bare die measurements too where the devices were mounted on an MPI TS2000-HP semi-automatic on-wafer prober.

Analysis of Measurements Results

Transconductance (g_m).

The experimental results presented in Fig. 3 offer critical insight into the influence of packaging on a foundational parameter: transconductance (g_m). The transconductance measurements of the TO-247 packaged device display a more sharply peaked g_m, reflective of instabilities observed when testing unpackaged devices and superior thermal management during probing. The properties, can however, display alternative trends if the measurement conditions are changed. For example, by reducing the pulse period from 200 ms to 10 ms, the impact of conduction power leading to internal heat generation and temperature rise is eliminated, enabling higher g_m. The differences in g_m peak shape and magnitude between bare die and packaged devices arise from the combined influence of thermal impedance, series resistance, amongst other parameters. The V_{DS} applied for the measurements shown in Fig. 3 has been 10 volts. The range selected for V_{GS} would is sufficient to support the conclusions regarding packaging-induced discrepancies.

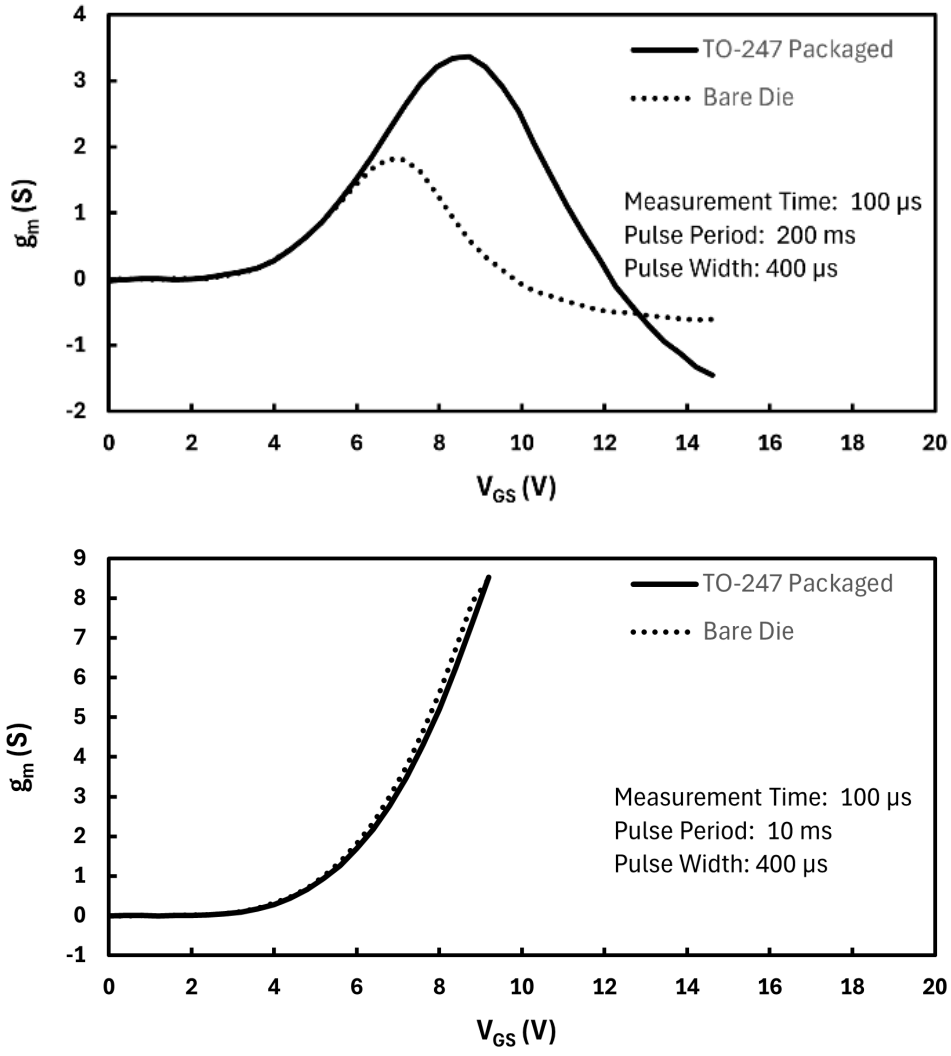

Fig. 3. Measurements of transconductance (g_m) on the bare die, compared with the same die packaged as a TO-247 discrete in different test conditions.

Drain-Source Leakage ($I_{DS\text{-}OFF}$).

Fig. 4 offers critical insight into the influence of packaging on another foundational parameter: the drain-source leakage current. The drain-source leakage current is consistently higher for the bare die, particularly at elevated drain voltages, due to the impact of environment on the bare die, leading to higher leakage, together with surface leakage induced by contamination, while the packaged device is fully protected from external influences. The differences also underline the importance of thermal

and parasitic considerations when interpreting the device datasheet values. Given the wide-bandgap of SiC, photo-generated effects under normal laboratory illumination are considered negligible compared with the leakage current levels measured. Furthermore, the leakage trends in Fig. 4 are consistent across the entire voltage range and do not show features typically associated with photo-induced leakage.

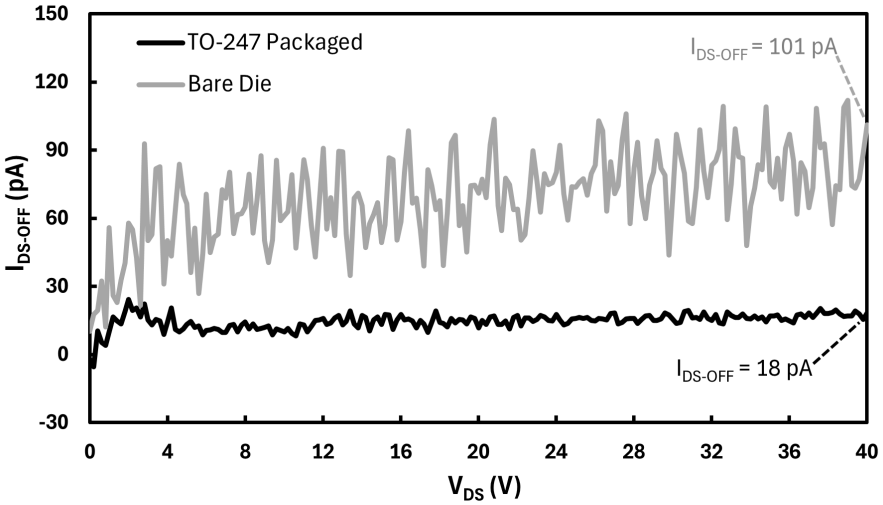

Fig. 4. Measurement of drain-source leakage current (I_{DS-OFF}) on the bare die, compared with the same die packaged as a TO-247 discrete.

Output Characteristics (I_{DS}-V_{DS}).

Fig. 5 focuses on the output characteristics (I_{DS}-V_{DS}) in different test conditions, revealing the extent to which packaging influences the device's output behavior under various operating conditions. The bare die displays the expected output behavior with different triode and saturation regions, reflecting the ideal field-effect behavior of a well-controlled SiC MOSFET channel. However, the TO-247 device exhibits some discrepancies, including a more gradual transition to the saturation region and reduced drain current at high V_{DS} at longer pulse widths. With reduction of pulse width and period, the impact of internal junction temperature build-up is reduced, relatively increasing the current of the packaged device. These shifts can be attributed to the increased $R_{DS(on)}$ and potential voltage drops across internal package resistance (R_{pkg}), as well as possible thermal degradation under extended bias conditions. Additionally, dynamic effects such as current crowding and self-heating within the package can distort the output curves, causing non-linearity and early onset of quasi-saturation. Longer pulse widths allow greater self-heating, which reduces I_{DS} through increased $R_{DS(on)}$ and mobility degradation. This effect is more pronounced in the TO-247 device due to higher thermal impedance and additional series resistance introduced by the package.

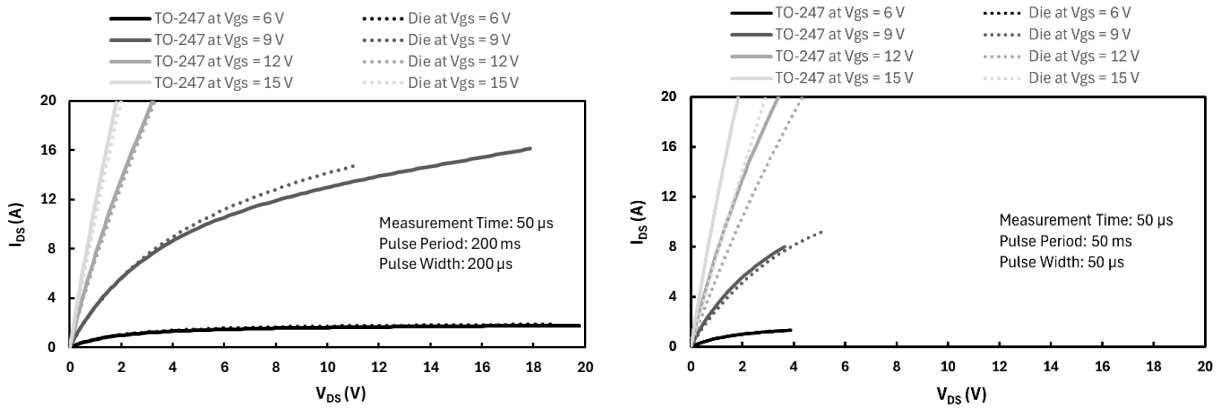

Fig. 5. The comparison and discrepancy of output characteristics (I_{DS}-V_{DS}) between the bare die and TO-247 packaged device in different test conditions.

Saturation (V_{DS}-V_{GS}).

In Fig. 6, the comparison of V_{DS} versus V_{GS} curves and extracted gate threshold voltages ($V_{GS(th)}$) between the two formats highlights further impacts of packaging. Initially, the device is in the cut-off region where the V_{GS} is lower than the $V_{GS(th)}$. Once V_{GS} increases beyond $V_{GS(th)}$ at low V_{DS} values, the current starts to flow, and the device is in the linear mode, effectively as a high resistor. Once the V_{DS} rises, the device effectively moves into the saturation mode of operation. The impact of additional resistance imposed by the packaging of the device means the onset of saturation is slightly delayed compared to the bare die. It must be noted that the pulse width affects saturation behavior through thermal effects. Longer pulses lead to delayed saturation due to increased effective $R_{DS(on)}$ from self-heating and package resistance.

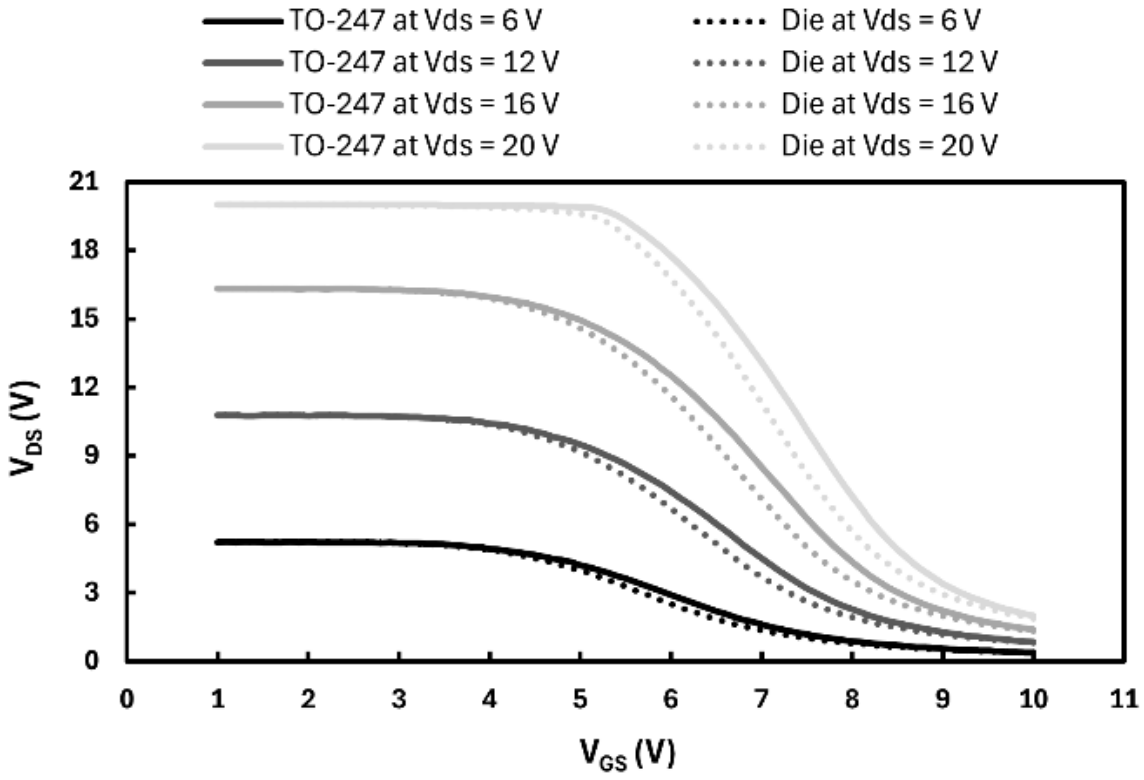

Fig. 6. Comparison of saturation by V_{DS}-V_{GS} on the bare die, compared with the same die packaged as a TO-247 discrete.

Gate Threshold Voltage (V_{TH}).

Fig. 7 highlights the comparison of the extracted gate threshold voltages ($V_{GS(th)}$). The limit for drain current to calculate the gate threshold voltage is 1 mA. During the measurements, the bare die showed a consistent threshold voltage with minimal hysteresis or drift due to its controlled thermal environment and the absence of mechanical or electrical stress. The TO-247 packaged device could demonstrate a slight shift in $V_{GS(th)}$, typically toward lower values, indicating temperature-induced threshold voltage drop and packaging-induced mechanical strain. Furthermore, voltage drops across the source connection in the TO-247 lead to inaccurate gate biasing, especially during fast transients, which can manifest as a threshold shift in measurement. The threshold voltage of the packaged device was measured to be slightly less than that of the bare die as the impact of internal temperature in packaged devices is higher, while the bare die is subject to surface leakage current. Nevertheless, it must be noted that the measured difference in $V_{GS(th)}$ between bare die and packaged devices is small and the difference is comparable to extraction uncertainty and likely influenced by a combination of temperature, surface effects, and measurement conditions.

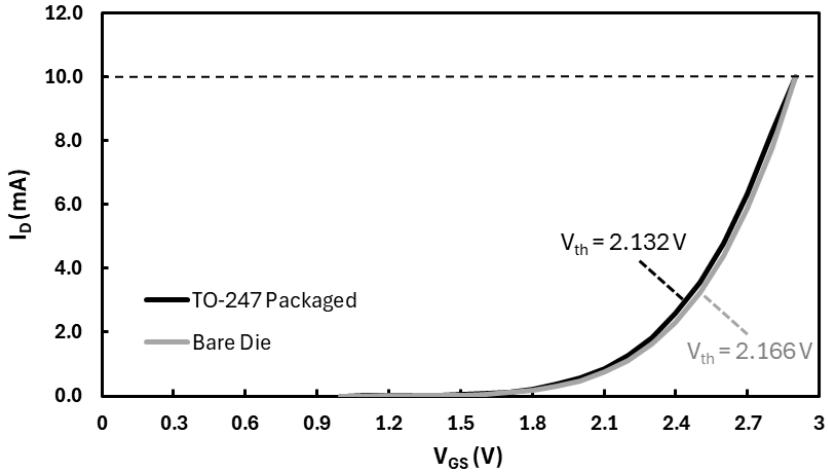

Fig. 7. Comparison of the gate threshold voltage on the bare die, compared with the same die packaged as a TO-247 discrete.

Transfer Characteristics (I_{DS}-V_{GS}).

Fig. 8 examines the transfer characteristics (I_{DS}-V_{GS}) of the device in bare die versus TO-247 format. The V_{DS} applied in these measurements is 10 volts. Extending the V_{GS} range is not necessary as the presented data demonstrates the key trends. The transfer characteristics of both devices show a steep increase in drain current with gate bias, suggesting high channel transconductance and uniform carrier mobility. This is especially true when testing with reduced pulse periods (pulse period reduced from 200 ms to 10 ms) which minimizes the impact of self-heating. The packaged device curve peaks higher, due to the more stable measurement mechanism on the device terminals and reduced surface leakage current, despite better thermal dissipation by the bare die on the Chuke.

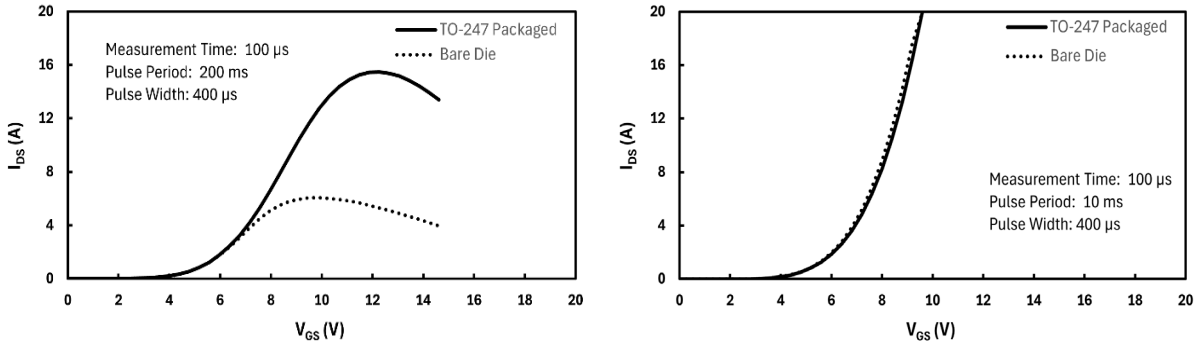

Fig. 8. Comparison of transfer characteristics (I_{DS}-V_{GS}) on the bare die, compared with the same die packaged as a TO-247 discrete in different test conditions.

On-state Resistance ($R_{DS\text{-}ON}$).

Fig.9 has depicted the $R_{DS\text{-}ON}$ values as another key parameter to evaluate. The $R_{DS(on)}$ values, derived from the linear region of these curves, are significantly higher in the TO-247 packaged device due to series resistances introduced by bond wires and lead frames, as well as junction heating under load. This increased $R_{DS(on)}$ not only affects conduction losses but also reflects how real-world packaging can obscure the true performance potential of the semiconductor die. This emphasizes the critical need for careful de-embedding of packaging effects in both datasheet interpretation and advanced power circuit design. However, the apparent reduction of extracted $R_{DS(on)}$ in these measurements for the packaged device at high current is not superior intrinsic performance. This is likely to have arisen from contact resistance, probe effects in bare-die measurements, and differing self-heating dynamics under pulsed conditions. For the bare-die measurements, true Kelvin sensing was implemented by placing separate force and sense probes directly on the source and drain pads, thereby minimizing series resistance and isolating the intrinsic die behavior. For the TO-247-3 package, a dedicated Kelvin source terminal does not exist, so the measured on-state resistance necessarily includes the

contribution of the source lead, bond wires, and internal package resistance. However, the Keysight N1265A fixture provides low-inductance connections and remote sensing up to the package terminals.

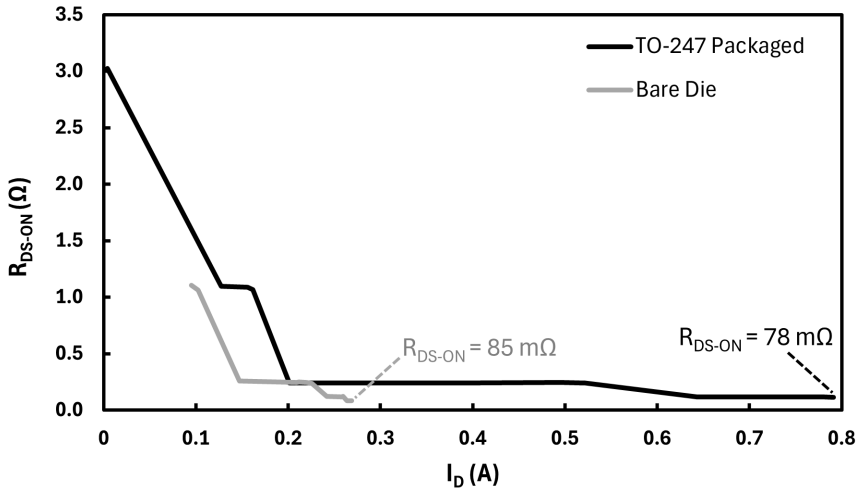

Fig. 9. Comparison of the on-state resistance (R_{DS-ON}) on the bare die, compared with the same die packaged as a TO-247 discrete.

Summary

The comparisons confirm that TO-247 packaging modifies the measured static behavior of 1200 V SiC MOSFETs. Direct junction temperature measurement was not performed. Packaging-induced parasitic elements impact the transconductance, increase $R_{DS(on)}$, and shift the $V_{GS(th)}$, while elevated thermal impedance raises leakage current and distorts output/transfer characteristics. Datasheet values derived from packaged devices therefore underestimate intrinsic die capability. Accurate compact models and loss predictions require careful de-embedding of packaging contributions. Bare die characterization remains essential to capture the true device physics, while packaged measurements are necessary to assess performance under practical operating conditions. Both perspectives are complementary to optimize SiC MOSFETs in high-performance power electronics.

Acknowledgement

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References

[1] Z. Zhu, R. Yao, H. Li, J. Li and Z. Chen, "Comparative Analysis on Switching Characteristics of Discrete SiC MOSFET in Press-pack Package and Wire-bonded Package", IEEE Int. Power Elec. Conf. & Expo. (PEAC), Guangzhou, China, 2022, p. 66-71, doi: 10.1109/PEAC56338.2022.9959610.

[2] J. O. Gonzalez, R. Wu, S. Jahdi and O. Alatise, "Performance and Reliability Review of 650 V and 900 V Silicon and SiC Devices: MOSFETs, Cascode JFETs and IGBTs," in IEEE Transactions on Industrial Electronics, vol. 67, no. 9, pp. 7375-7385, Sept. 2020, doi: 10.1109/TIE.2019.2945299.

[3] A. Lemmon, S. Banerjee, K. Matocha and L. Gant, "Analysis of Packaging Impedance on Performance of SiC MOSFETs," PCIM Europe 2016, Nuremberg, Germany, 2016, pp. 1-8.

[4] A. Anthon, J. C. Hernandez, Z. Zhang and M. A. E. Andersen, "Switching investigations on a SiC MOSFET in a TO-247 package," IECON 2014 - 40th Annual Conference of the IEEE Industrial Electronics Society, Dallas, TX, USA, 2014, pp. 1854-1860, doi: 10.1109/IECON.2014.7048754.

[5] N. Phankong, T. Yanagi and T. Hikihara, "Evaluation of inherent elements in a SiC power MOSFET by its equivalent circuit," 14th Euro. Conf. on Power Electronics, UK, 2011, pp. 1-8.