*Key Engineering Materials*
*ISSN: 1662-9795, Vol. 1054, pp 55-67*
*doi:10.4028/p-HwDA3m*

*Submitted: 2025-09-11*
*Revised: 2026-01-18*
*Accepted: 2026-02-28*
*Online: 2026-05-18*

# Impact of the Negative Gate Bias on Short-Circuit Robustness of SiC MOSFETs with Measurements and Simulations

Madhu Lakshman Mysore[1,a*], Rahul-Vijaybhai Chavda[1,b], Josef Lutz[1,c], Thomas Basler[1,d]

[1]Chemnitz University of Technology, Chair of Power Electronics, Chemnitz, Germany

[a*]madhu-lakshman.mysore@etit.tu-chemnitz.de, [b]rahul-vijaybhai.chavda@etit.tu-chemnitz.de, [c]josef.lutz@etit.tu-chemnitz.de, [d]thomas.basler@etit.tu-chemnitz.de

**Keywords:** short-circuit robustness, SC failures, thermal runaway, npn BJT activation, gate-leakage, TCAD.

**Abstract.** This work investigates the short-circuit (SC) robustness of 1200 V SiC MOSFETs from two different manufacturers (M1: trench-gate, M2: planar-gate) up to their destruction limits. Both devices, packaged in TO-247 4-pin housings with a nominal on-state resistance ($R_{ds,on}$) of 80 mΩ, were systematically tested under a gate-source voltage of $V_{GS,on}$ =15 V and at a fixed DC-link voltage of 800 V. In addition to determining the SC withstand capability, the study focuses on the influence of the negative gate bias ($V_{GS,off}$ ) on device robustness. Results show that SC capability and dominant failure mechanisms are strongly dependent on gate technology as well as on the applied $V_{GS,off}$ . Trench-gate M1 devices primarily fail due to gate oxide degradation under strong negative bias, while planar-gate M2 devices exhibit failures linked to parasitic BJT activation at SC turn-off or thermal runaway at $V_{GS,off}$ = 0 V. Additionally, TCAD simulations closely reproduce the measured trends and provide physical insight into the failure mechanisms. The experimental–simulation approach establishes a comprehensive understanding of SC robustness limits and failure types in state-of-the-art SiC MOSFET technologies.

## Introduction

Short-Circuit (SC) events in Silicon Carbide (SiC) power MOSFETs are critical failure modes in many high-power applications, such as motor drives, electric vehicle (EV) traction inverters, and uninterruptible power supply (UPS) units. During an SC event, devices experience severe electrical and thermal overstress and must possess sufficient short-circuit withstand capability until e.g. an external protection circuitry can safely interrupt the fault or the gate driver turn-off the device safely. A comprehensive understanding of SC robustness and the associated physical failure mechanisms is therefore essential for ensuring the reliability of SiC MOSFETs in demanding environments.

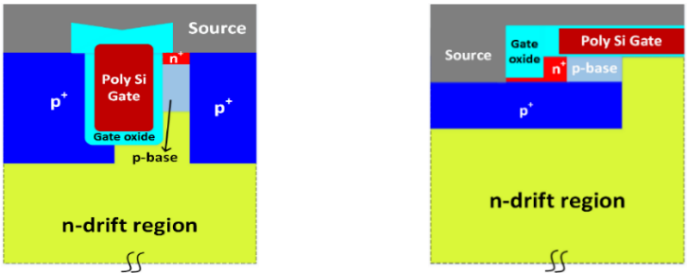
The short-circuit behaviour of SiC MOSFETs has been widely studied. Prior work has demonstrated that, despite lower on-resistance, the higher drain saturation current, and reduced chip area of SiC MOSFETs accelerate junction temperature rise, thereby degrading SC capability as compared to Si IGBT [1]. Repetitive SC stress has been reported to be more detrimental on planar devices compared to trench counterparts due to the differences in gate oxide thickness [2]. High-speed optical imaging in [3] further revealed aluminum metallization melting during the SC transient, highlighting the severity of the thermal stress. Detailed SC failure analysis of trench-gate and planar-gate SiC MOSFETs in [4] revealed that at a DC-link voltage of 400 V, fracture of the gate interlayer dielectric occurs, whereas at 800 V, failure is exacerbated by the activation of the parasitic bipolar junction transistor (BJT) due to extreme junction temperatures. Furthermore, in converter applications, negative turn-off gate voltages are often employed to suppress unintended turn-on from Miller capacitance-induced cross-talk – the parasitic turn-on effect [5]. However, all the aforementioned studies consider SC ruggedness at a fixed negative gate voltage ($V_{GS,off}$), leaving the dependence of SC withstand capability and failure modes on $V_{GS,off}$ largely unexplored. Notably, application of negative gate voltage prior to SC turn-on can the trapping of holes at the SiC/$SiO_2$ interface which leads to a shift (reduction) in threshold voltage known from the $V_{th}$-hysteresis effect**.**

In this work, the impact of negative gate bias on the SC robustness and failure mechanisms type on different gate technologies (trench and planar) for 1.2 kV SiC MOSFETs is systematically investigated at a DC-link voltage of 800 V. By combining experimental characterization with physics-based TCAD simulations, a comprehensive study is presented that elucidates the interplay between $V_{GS,off}$ values, device structure design, and SC withstand capability, thereby providing new insights into SC induced failure mechanisms for both gate technologies.

## Device Under Test and Simulation Model

The Device Under Test (DUTs) were commercially available 1.2 kV SiC MOSFET from two different manufacturers (denoted as M1, and M2) with similar current ratings but employs distinct cell technologies, as illustrated in Fig. 1. The device parameters for both SiC MOSFETs are summarized in Table. 1. Electro-thermal simulations were performed to understand the SC robustness dependency on $V_{GS,off}$ values and to analyze the associated SC failure mechanisms, using *Synopsys TCAD* [6]. As shown in Fig. 1, 1200 V half-cell trench-gate and planar-gate structures were designed and modelled to match the real structure and were subsequently calibrated [7]. Further, the doping concentrations for these models were derived from simulation-oriented literature and may not precisely replicate the parameters of commercial devices [4]. Nevertheless, these values are representative and adequate to capture the essential electrical and thermal behaviour of the studied structures [4]. The coupled electro-thermal behaviour was simulated using *Synopsys Sentaurus Device*, wherein the electrical and thermal domains were solved self-consistently to account for the strong temperature dependence of SiC material properties under high-stress conditions. The simulations incorporated periodic boundary conditions and employed advanced physical models, including the Okuto avalanche model, incomplete ionization model, Shockley-Read-Hall (SRH), Auger recombination, high-field carrier velocity saturation, temperature-dependent bandgap narrowing, temperature-dependent carrier mobility (Inverse Accumulation Layer model), and thermodynamic heat transport.

For thermal boundary conditions, surface thermal contacts were defined at the drain electrode with thermal resistance values of 1.1 K/W for the planar MOSFET and 0.69 K/W for the trench MOSFET, in accordance with device datasheets. To improve the accuracy of transient temperature predictions, the volume-specific heat capacities of SiC and Al were adjusted according to experimentally validated data reported from [8].



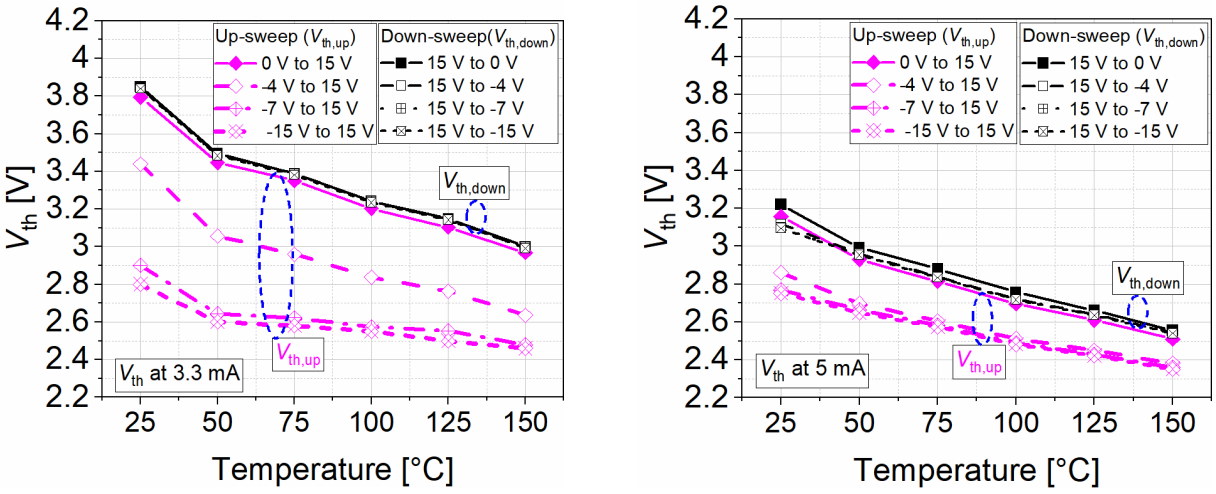

(a) M1 (b) M2

**Fig. 1.** Schematic cross-section of the cell head of SiC MOSFETs from different manufacturers.

**Table 1.** Device parameters of the SiC MOSFETs from different manufacturers.

| **Device parameters** | **M1** | **M2** |
|---|---|---|
| Gate technology | Trench | Planar |
| Rated current | 31 A | 32 A |
| $R_{ds,on}$ | 80 mΩ | 80 mΩ |
| Recommended $V_{GS,on}$ | 18 V | 15 V |
| Recommended $V_{GS,off}$ | 0 V | -4 V |
| Package type | TO-247-4 | |

## Threshold Voltage Characterization



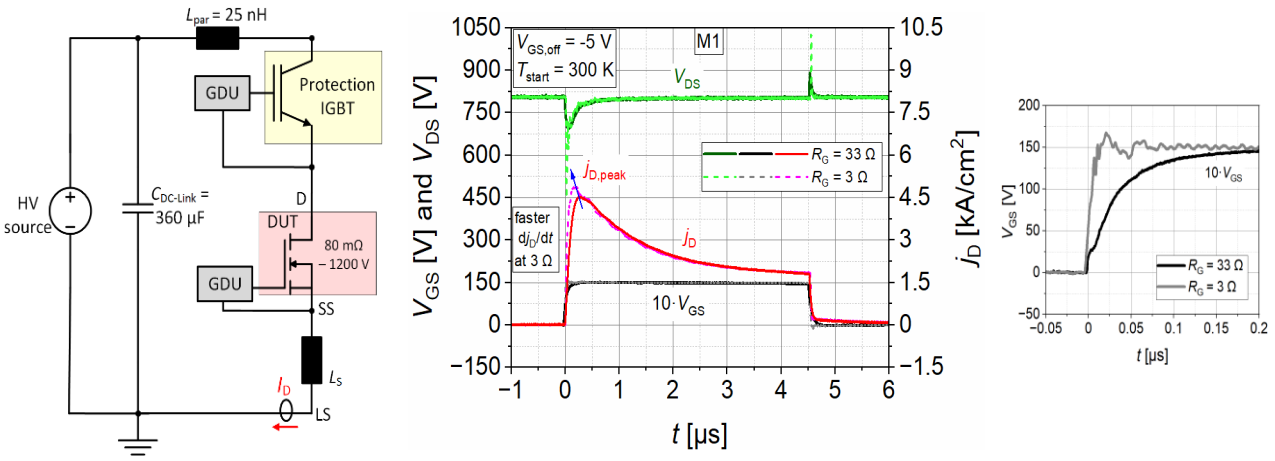

(a) M1 (b) M2

**Fig. 2.** Measured threshold voltage trend ($V_{th,up}$ and $V_{th,down}$) as function of temperature for two different manufacturers at a datasheet given current. Measured conditions of $V_{GS,on}$ = 15 V.

The SiC MOSFETs are susceptible to threshold voltage ($V_{th}$) drift and shift due to mechanisms such as bias temperature instability (BTI) and charge trapping at the SiC/SiO2 interface (hysteresis phenomenon). The measurement procedure for each DUT is applied according to the JEDEC standard JEP184 [9]. The pulse pattern and measurement principle is described in [10]. Accurate $V_{th}$ characterization of SiC MOSFETs, especially when combined with preconditioning, are crucial for assessing their reliability and performance. Preconditioning, like applying specific gate voltage pulse pattern as discussed in [10], can stabilize the $V_{th}$ and improve the measurement repeatability. In this study, both gate technologies were subjected to identical up-sweep and down-sweep voltage ramps for $V_{th}$ extraction as shown in Fig. 2. As the temperature increases, the $V_{th}$ decreases for both manufacturers. For the M1 device at fixed temperature, $V_{th}$ decreased progressively as $V_{GS,off}$ decreased from 0 V to -15 V. In contrast, the M2 device exhibited a smaller $V_{th}$ reduction, with values earlier saturating when $V_{GS,off}$ exceeded -7 V. Under down-sweep conditions, $V_{th}$ remained essentially unchanged for both gate-technologies, regardless of the applied negative gate bias during switching transients.

## Experimental Setup

The short-circuit (SC) measurement setup for the SiC MOSFET is schematically illustrated in Fig. 3(a). The protection IGBT (PIGBT) and the device under test (DUT) are connected in series close to the DC-link capacitors. The commutation loop parasitic inductance ($L_{par}$) was measured to be 25 nH. The gate-source voltage ($V_{GS}$) and drain-source voltage ($V_{DS}$) were measured at the sense-source (SS) terminal without the influence of load-source inductance ($L_S$). A Rogowski coil was used to measure the current. An exemplary SC waveform at a DC-link voltage of 800 V, with $V_{GS}$ switched between 15 V/-5 V for two different gate resistances ($R_G$), is shown in Fig. 3(b). For $R_G$ of 3 Ω, the SiC MOSFETs exhibited significantly faster SC switching transients, resulting in slightly higher gate voltage overshoot ($V_{GS,peak}$) and a correspondingly larger drain current density peak ($j_{D,peak}$). The increased current slope ($\mathrm{d}j_D/\mathrm{d}t$) causes a significant induced undershoot and overvoltage across the drain and source, thereby higher electrical stress.



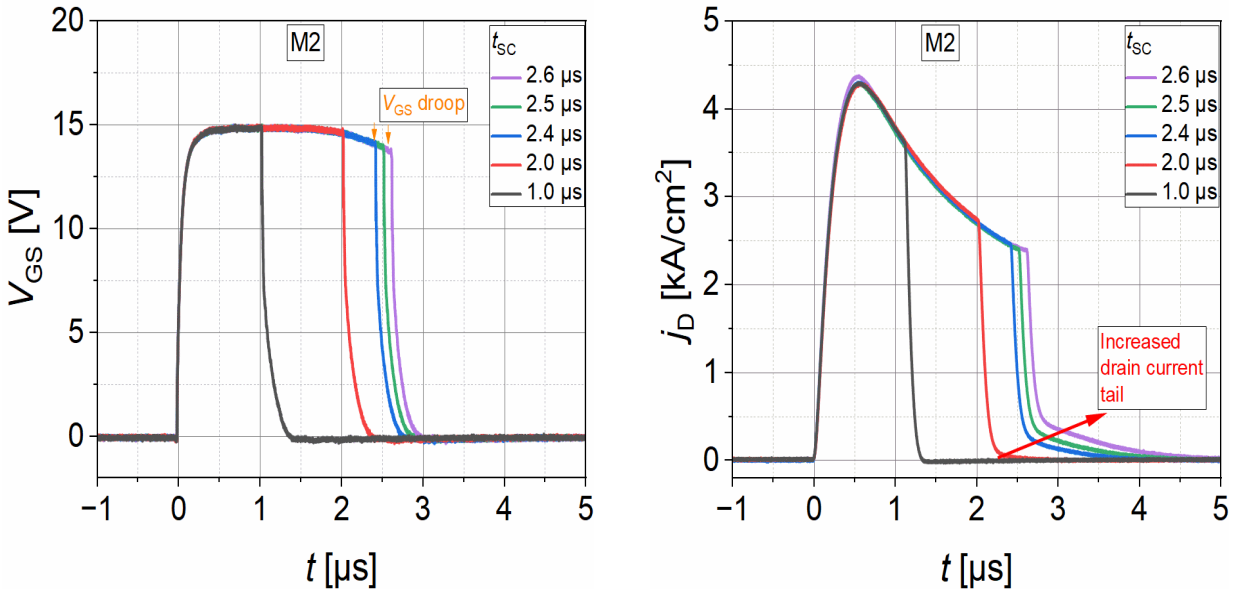

(a) (b) $V_{DC,link}$ = 800 V, $V_{GS}$ = 15 V/-5 V, $t_{SC}$ = 4.5 µs (c) zoomed $V_{GS}$

**Fig. 3.** (a) Schematic diagram of the short-circuit measurement setup (b) Measured SC behaviour of M1 devices at two different gate resistance for given conditions of $T_{start}$ = 300 K, $L_{par}$ = 25 nH. (c) Zoomed $V_{GS}$ turn-on.

## Short-Circuit Results and Analysis

The short-circuit characteristics of SiC MOSFETs are strongly influenced by multiple factors, including gate driving conditions and negative gate voltage prior to SC turn-on. In the following section, the effects of pulse width and negative gate voltages on SC behaviour are analyzed through a combination of experimental measurements and electro-thermal TCAD simulations.

### Influence of the $t_{SC}$




(a) $V_{GS}$ (b) $j_D$

**Fig. 4.** Measured SC behaviour of the planar-gate SiC MOSFETs for $V_{GS}$ = 15 V/0 V. Measurement conditions: $V_{DC,link}$ = 800 V, $R_G$ = 33 Ω, $T_{start}$ = 300 K, $L_{par}$ = 25 nH.

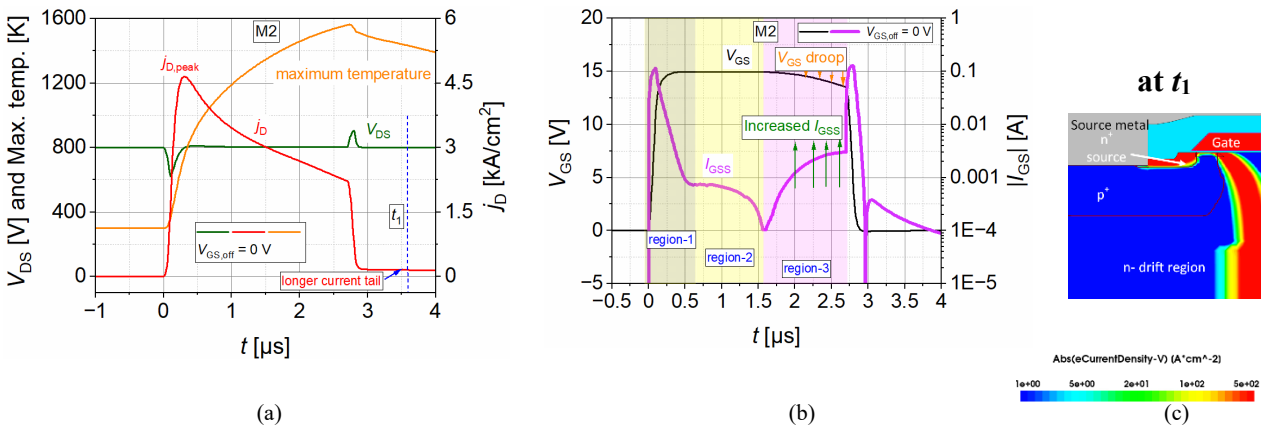
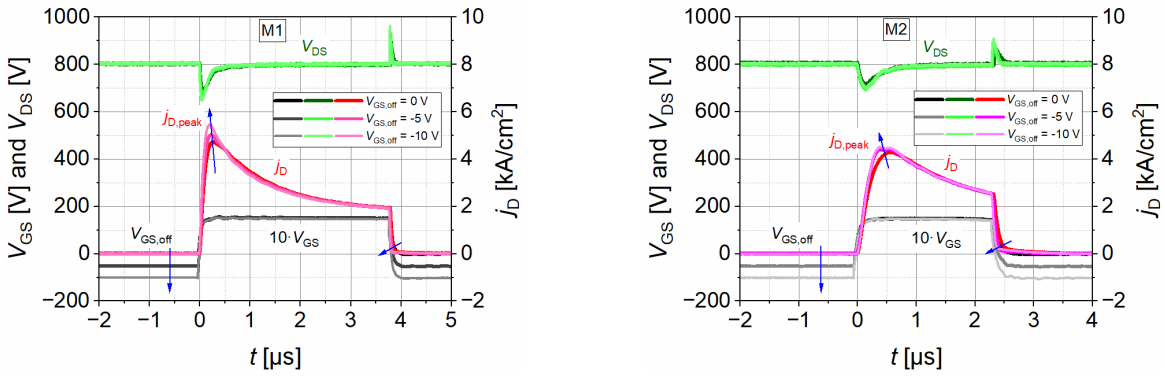



**Fig. 5.** Simulated SC behaviour of the planar-gate (M2) SiC MOSFETs for $V_{GS}$ = 15 V/0 V (a) $j_D$, $V_{DS}$ and maximum temperature transients. (b) $V_{GS}$ and $I_{GS}$ transients. (c) electron current density at $t_1$. Simulation conditions: $V_{DC,link}$ = 800 V, $R_G$ = 33 Ω, $T_{start}$ = 300 K, $L_{par}$ = 25 nH, and $t_{SC}$ = 2.6 µs.

At a DC-link voltage of 800 V, SC measurements were carried out on M1 devices under switched gate voltage of 15 V/ 0 V, as shown in Fig. 4. A gate voltage droop was pronounced for an SC pulse width beyond 2 µs, [Fig. 4(a)]. The drain current density ($j_D$) reaches a peak value shortly after the onset of SC event, but decreases with increasing $t_{SC}$ due to carrier mobility reduction in combination with JFET effect [11]. Additionally, a prolonged drain current tail was observed after SC turn-off, which becomes more prominent with longer SC durations. This is due to the strongly reduced gate threshold voltage at very high temperature from SC event and a possible parasitic npn turn-on [12]. Further, the simulations utilized the Direct Tunneling model (includes thermionic emission model) to capture the non-permanent increased gate leakage current during SC event, as previously reported in [13]. The simulated SC behaviour for planar-gate at DC-link voltage of 800 V is plotted in Fig. 5. A significant rise in the maximum temperature was observed during the SC pulse, [Fig. 5(a)], which directly contributes to the increased $I_{GSS}$ via thermionic emission mechanisms in time region-3, as depicted in Fig. 5(b). This rise in $I_{GS}$ results in a pronounced droop in the steady-state gate voltage. In contrast, the gate leakage current in region-1 and region-2 is primarily dominated by the classical gate charging pulse and displacement currents via $dV_{GD}/dt$ across the Miller capacitance. After SC turn-off, the electron current flowing through channel reflects the reduced $V_{th}$ induced by very high junction temperature.

### Influence of the $V_{GS,off}$

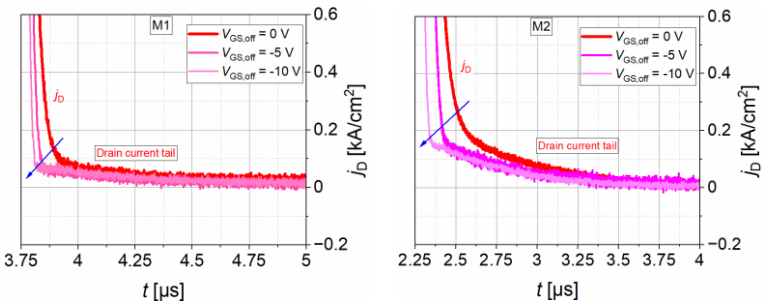



(a) M1 with $t_{SC}$ = 3.8 µs (b) M2 with $t_{SC}$ = 2.4 µs

**Fig. 6.** Measured SC behaviour at different $V_{GS,off}$ values for both manufacturers. Conditions: $V_{DC,link}$ = 800 V, $R_G$ = 33 Ω, $T_{start}$ = 300 K, $L_{par}$ = 25 nH, $V_{GS,on}$ = 15 V.

The applied negative gate voltages before the SC event influences $j_{D,peak}$. Due to hysteresis effect, the threshold voltage is reduced in a manner similar to the up-sweep behaviour shown in Fig. 2 [14]. This reduction in $V_{th}$ improves the device transconductance, thereby increasing $j_{D,peak}$ as illustrated in

Fig. 6. The corresponding zoomed-in drain current tail is plotted in Fig. 7. For the M1 devices, $j_{D,peak}$ increased monotonically with decreasing $V_{GS,off}$. However, the M2 devices exhibited an increase in $j_{D,peak}$ when $V_{GS,off}$ was reduced from 0 V to -5 V, after which $j_{D,peak}$ saturated despite further increases in negative bias. This behaviour correlates closely with the measured $V_{th}$ trends obtained from the up-sweep characterization for both devices. The plotted $j_{D,peak}$ for different $V_{GS,off}$ values for both manufacturers is displayed in Fig. 8. Following SC turn-off, achieved by switching the $V_{GS}$ from positive to negative value, the drain current tail was observed to be only slightly affected, see Fig. 7. For a fixed $V_{GS,on}$ and $R_G$, the switching transients becomes faster with increasing magnitude of $V_{GS,off}$. The substantial $V_{th}$ reduction caused by the elevated channel temperature during the SC event can prolong the longer channel-on condition [Fig. 5(c)]. However, by applying larger negative $V_{GS,off}$ enables the channel can be close more rapidly, thereby slightly reducing drain current tail duration.




(a) M1 with $t_{SC}$ = 3.8 µs (b) M2 with $t_{SC}$ = 2.4 µs

**Fig. 7.** Zoomed-in SC drain current tail at different $V_{GS,off}$ values for both manufacturers from Fig. 6. Conditions: $V_{DC,link}$ = 800 V, $R_G$ = 33 Ω, $T_{start}$ = 300 K, $L_{par}$ = 25 nH, $V_{GS,on}$ = 15 V.

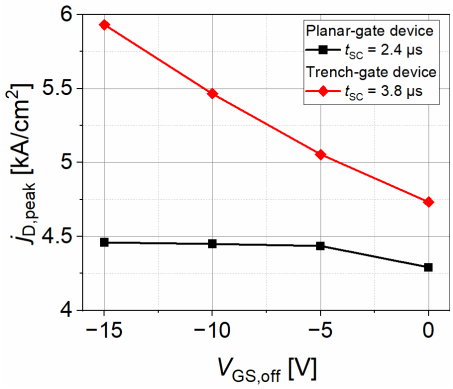
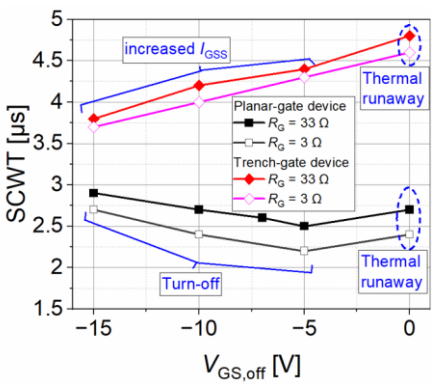
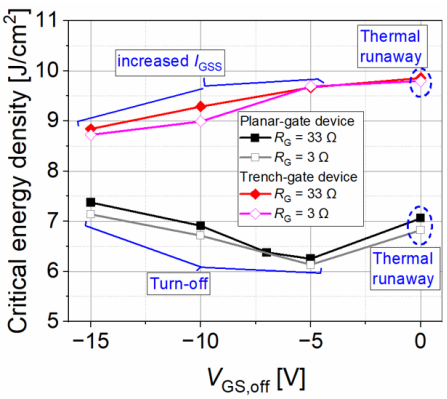



**Fig. 8.** Measured $j_{D,peak}$ as a function of $V_{GS,off}$ for trench and planar-gate SiC MOSFETs during SC turn-on. Conditions: $V_{DC,link}$ = 800 V, $R_G$ = 33 Ω, $T_{start}$ = 300 K, $L_{par}$ = 25 nH, $V_{GS,on}$ = 15 V.

## SC Robustness Limit

The SC capability was determined by gradually increasing the pulse width duration ($t_{SC}$) in steps of 100 ns for a fixed switched $V_{GS}$ and DC-link voltage. To determine their robustness limit, the measurements were carried out until the destruction of the DUTs or a strong drift in the electrical parameters such as gate leakage current ($I_{GSS}$), loss of blocking capability or increased drain-source leakage current ($I_{DSS}$) is detected, which indicate damage in the device.



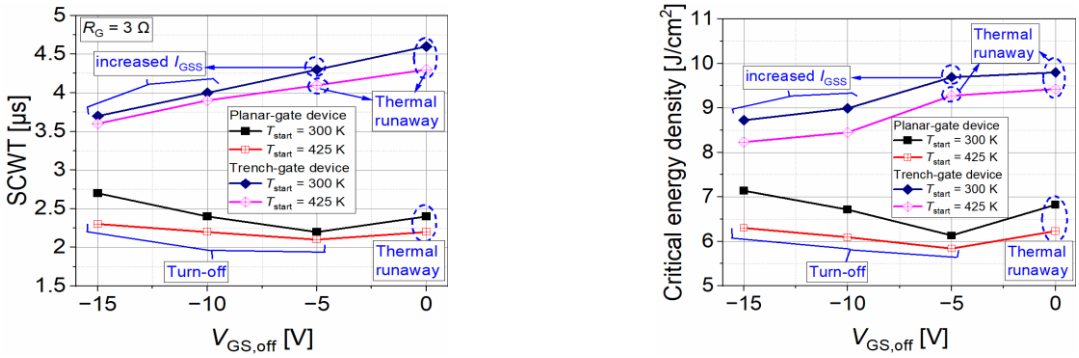




(a) SCWT vs different $V_{GS,off}$ (b) Critical energy density vs different $V_{GS,off}$

**Fig. 9.** Comparison of the trench and planar-gate SiC MOSFETs as a function of $V_{GS,off}$ for two different $R_G$. Measurement conditions: $V_{DC,link}$ = 800 V, $T_{start}$ = 300 K, $L_{par}$ = 25 nH, and $V_{GS,on}$ = 15 V.

**At $T_{start}$ = 300 K**

To determine the SC robustness at each $V_{GS,off}$ level, more than two devices were tested for each conditions. The measured short-circuit withstand time (SCWT) varied between 100 ns to 200 ns for a fixed test conditions. The SCWT for both technologies is compared as a function of $V_{GS,off}$ for two different $R_G$, as shown in Fig. 9(a). The trench-gate device exhibited a monotonic decrease in SCWT with more negative $V_{GS,off}$ values. Because the applied negative gate voltages before the SC event reduces the threshold voltage and correspondingly improves the transconductance, which leads to higher short-circuit current density peak ($j_{D,peak}$) as shown in Fig. 6(a). Hence, a higher energy dissipation for same $t_{SC}$. In contrast, the planar-gate device displayed decreased SCWT till $V_{GS,off}$ of -5 V and for further lower $V_{GS,off}$ values, the SCWT increases from 2.5 µs at -5 V to 2.9 µs at -15 V. The corresponding critical energy density of both devices is plotted in Fig. 9(b). The energy density shows a similar trend that of the SCWT. The planar-gate device exhibits a minimum critical energy density at $V_{GS,off}$ = -5 V. A smaller $R_G$ resulted in faster SC switching transients and increased energy dissipation due to $j_{D,peak}$, see Fig. 3(b). Nonetheless, the overall trends in SCWT and energy density remained consistent, with slightly reduced SCWT values within the range of 100 ns to 200 ns. At $V_{GS,off}$ = 0 V, both gate technologies exhibit the thermal runaway failure irrespective of the $R_G$. With increasingly negative $V_{GS,off}$, the M1 devices demonstrated failures dominated by elevated $I_{GSS}$ values far above the datasheet limit, as confirmed through post SC pulse verification via source measurement unit (SMU). In contrast, planar-gate devices primarily show a SC turn-off failure under the same conditions.




(a) SCWT vs different $V_{GS,off}$

(b) Critical energy density vs different $V_{GS,off}$

**Fig. 10.** Comparison of the trench and planar-gate SiC MOSFETs as a function of $V_{GS,off}$ for two different $T_{start}$. Measurement conditions: $V_{DC,link}$ = 800 V, $R_G$ = 3 Ω, $L_{par}$ = 25 nH, and $V_{GS,on}$ = 15 V.

**At *T*start = 425 K**

Overall, the failure modes remained consistent for both manufacturers when the starting junction temperature (*T*start) was increased, as shown in Fig. 10. At 425 K, the SCWT tendency remains the same for both manufacturers. However, the last-pass SC event occurred 100–300 ns earlier compared to room temperature. For the M2 device, the failures at the corresponding negative *V*GS,off remained similar to those at room temperature. In contrast, the M1 device exhibited a shift in failure mechanism at *V*GS,off = -5 V, transitioning from increased gate leakage current failure at 300 K to thermal runaway failure at elevated temperature.

Notably, M1 device exhibited its longest SCWT at *V*GS,off of 0 V for both temperatures. Whereas the M2 device demonstrated higher SC robustness at *V*GS,off of -15 V across both temperature conditions. The lower critical energy density of the M2 device, compared to M1 device, can be attributed to the higher energy dissipation per unit channel-width, which further amplified by the unfavorable thermal network of the planar-gate [2]. The different SC failure modes observed in devices from both manufacturers are discussed in detail in the next section.

## SC Failure Types

The SC failure mechanisms in both gate technologies are analyzed using post-failure microscopic images along with TCAD simulations. Furthermore, the SCWT trends observed for both manufacturers are investigated and interpreted through detailed electro-thermal TCAD simulations.

Fig. 11 depicts the thermal runaway failure of the M1 SiC MOSFET at $V_{GS,off}$ of 0 V under elevated starting temperature. Although the device was switched-off to the preset condition of 15 V/ 0 V, a prolonged drain current tail persisted leading to thermal runaway at 7.4 µs for an SC pulse width of 4.2 µs. At the onset of thermal runaway, the device losses its blocking capability, accompanied by rapid increase in both $V_{GS}$ and $j_D$. Inset in Fig. 11 shows the post-failure chip surface of the M1device after decapsulating the TO package. Microscopic image reveals a completely burned surface caused by aluminum metallization melting, while the bond wire remained intact.

All M1 devices exhibited failure due to post SC increased $I_{GSS}$ with increased negative $V_{GS,off}$ values, except at -5 V for 425 K. Fig. 12 shows a representative non-destructive SC event at $V_{GS,off}$ of -10 V, where the device survives the SC stress without displaying any distinct failure transient. Nevertheless, only the intermediate measured $I_{GSS}$ in between the SC event shows a sudden increase after an SC pulse width of 4.2 µs for $V_{GS}$ of 15 V/-10 V, as illustrated in Fig. 13. For M1 devices, post $I_{GSS}$ remains nearly unchanged with increased SC pulse width, until an abrupt rise occurred, a similar observation for M1 devices is reported under overcurrent turn-off failure in [7]. Such a sharp increase in $I_{GSS}$ is indicative of pre-damage to the gate oxide, with measured values exceeding the maximum limits specified in the datasheet. The inset in Fig. 12 presents the post-failure chip surface of an M1 device after decapsulating the TO packages, revealing no damage or failure region on the chip surface or even on the gate runner.

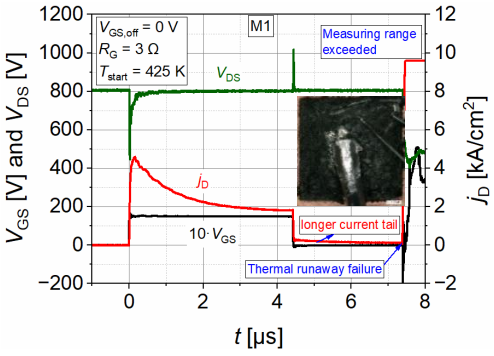



**Fig. 11.** Measured thermal runaway failure of the M1 device. Conditions: $V_{DC,link}$ = 800 V, $R_G$ = 3 Ω, $T_{start}$ = 425 K, $V_{GS}$ = 15 V/0 V, $L_{par}$ = 25 nH. Inset: microscopic image of the failed device.

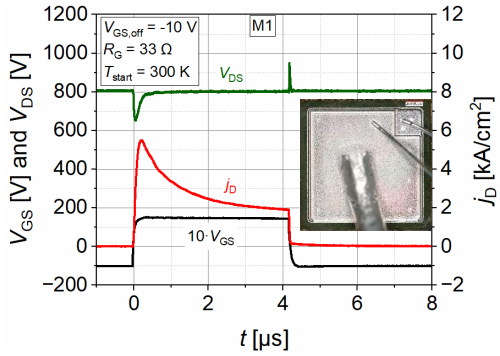



**Fig. 12.** Measured non-destructive pulse of the M1 device. Conditions: $V_{DC,link}$ = 800 V, $R_G$ = 33 Ω, $T_{start}$ = 300 K, $V_{GS}$ = 15 V/-10 V, $L_{par}$ = 25 nH. Inset: Microscopic image of the device.

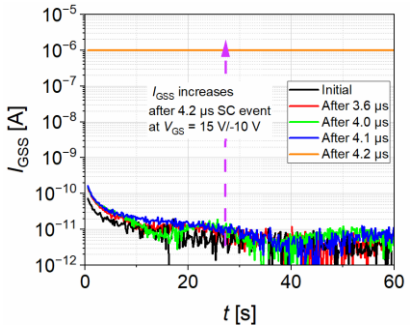



**Fig. 13.** Measured $I_{GSS}$ in between SC measurements for M1 manufacturer. Conditions as per the datasheet value: $V_{DS}$ = 0 V, $V_{GS}$ = 25 V.

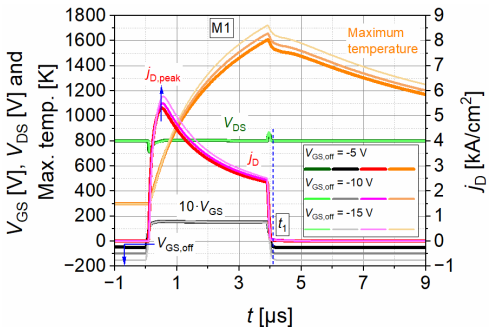
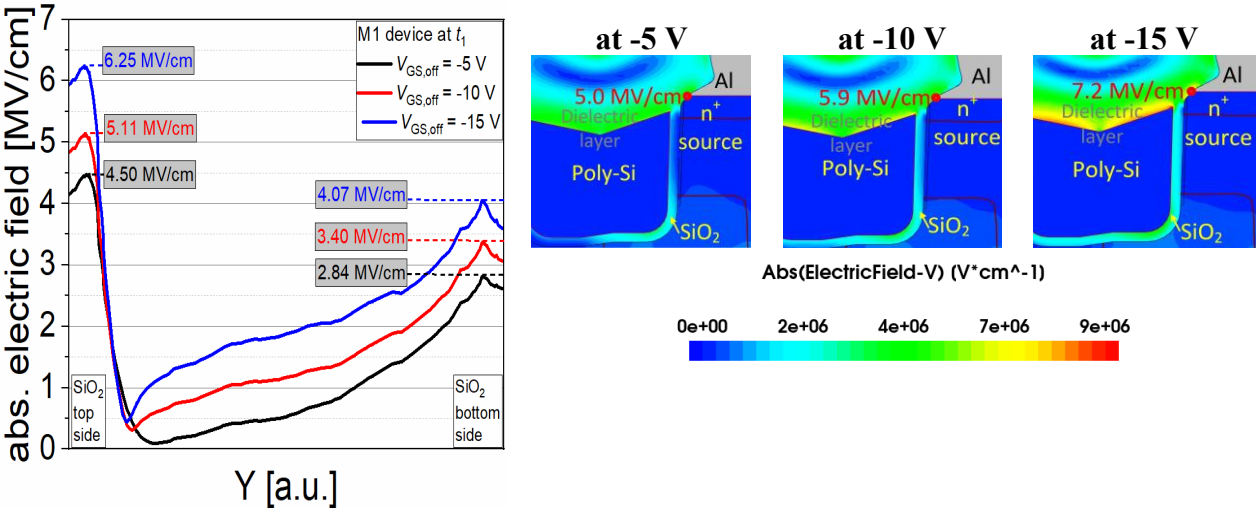



**Fig. 14.** Simulated SC behaviour of the trench-gate SiC MOSFETs for different $V_{GS,off}$ values. Conditions: $V_{DC,link}$ = 800 V, $R_G$ = 33 Ω, $T_{start}$ = 300 K, $L_{par}$ = 25 nH, $V_{GS,on}$ = 15 V, and $t_{SC}$ = 3.9 µs.

To investigate the mechanism behind the reduced SCWT with lower negative $V_{GS,off}$ values, SC simulations were performed for $t_{SC}$ of 3.9 µs at different $V_{GS,off}$ values, as plotted in Fig. 14. Applying a negative gate bias prior to the SC event reduces the threshold voltage because of hysteresis effect [14], thereby increasing the $j_{D,peak}$ through enhanced transconductance, see Fig. 6 and Fig. 14. The resulting higher $j_{D,peak}$ translates to greater energy dissipation and a corresponding rise in device maximum temperature during the SC event for the same $t_{SC}$. In measurements, the degraded M1 devices exhibit a permanent increase in $I_{GSS}$ post SC event after exceeding the critical SCWT, indicating gate-oxide degradation. To understand this effect, the time point $t_1$ was considered at simulated SC turn-off to study the influence of the negative voltage on the gate oxide field. Fig. 15(a) displays the plotted electric field distribution at the trench gate oxide adjacent to the channel for different $V_{GS,off}$ values at $t_1$. The electric field distribution in the simulated gate structure for various $V_{GS,off}$ values at $t_1$ is shown in Fig. 15(b).

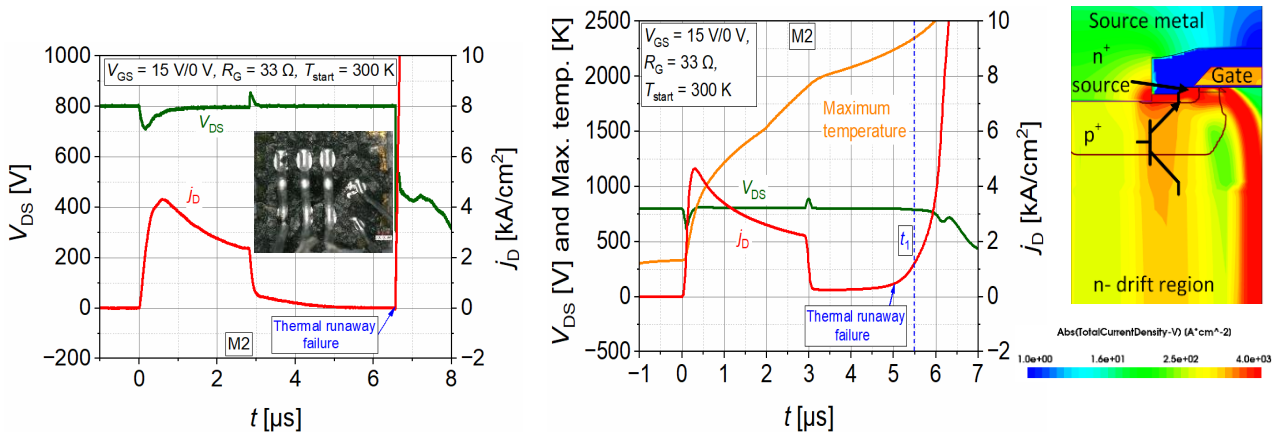
For a same SC duration, the electric field at the trench gate oxide adjacent to the channel increase with more negative $V_{GS,off}$. The high electric field contribution from the pn-junction under an 800 V DC-link voltage, combined with gate voltage driven field from $V_{GS}$, sum up to an effective high electric field in trench oxide. Furthermore, the simulation reveal that electric field at the dielectric/Al interface [highlighted by the red dot in Fig. 15(b)] also intensifies with more negative $V_{GS,off}$. The elevated device temperature under stronger negative $V_{GS,off}$ additionally induce higher thermo-mechanical expansion stress between layers, which may lead to inter-layer dielectric cracking, as discussed in the literature [4, 15]. For $V_{GS,off}$ of -15 V, a peak electric field of 7.2 MV/cm was obtained at the interface between the dielectric and Al, see Fig. 15(b). This higher field accelerates localized degradation, eventually triggering pre-damage to the gate oxide of the devices which fits to increased $I_{GSS}$ at longer SC events. While these simulations were carried out at 3.9 µs, it is expected that further increase in pulse width similar to measurement conditions would raise the localized oxide field even further in gate oxide for -5 V and -10 V, thereby accelerating the gate degradation.




(a) Electric field at $t_1$

(b) Electric field distribution in M1 device at different $V_{GS,off}$

**Fig. 15.** (a) Simulated electric field in the trench gate oxide adjacent to channel. (b) Electric field distribution of the M1 gate structure at time point of $t_1$ for different $V_{GS,off}$ values. Conditions: $V_{DC,link}$ = 800 V, $R_G$ = 33 Ω, $T_{start}$ = 300 K, $L_{par}$ = 25 nH, $V_{GS,on}$ = 15 V, and $t_{SC}$ = 3.9 µs. For cut, see Fig. 14.

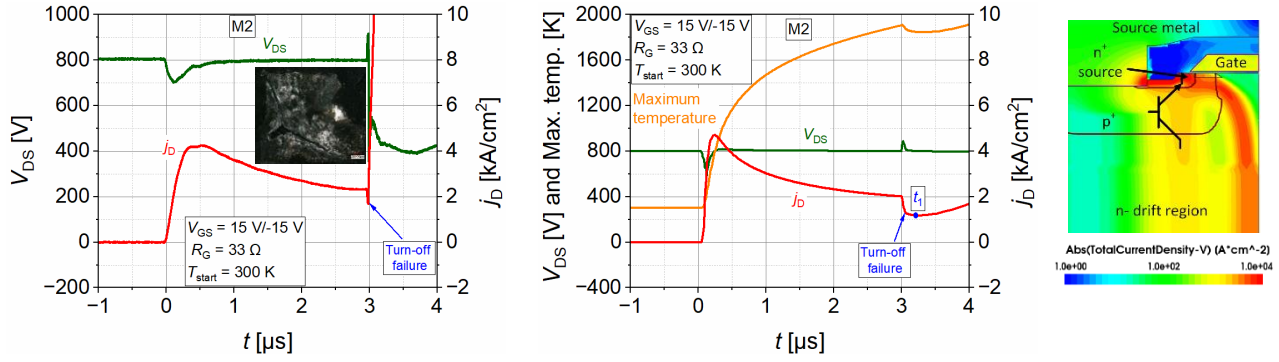



(a) Measured thermal runaway (b) Simulated thermal runaway (c)

**Fig. 16.** (a) Measured thermal runaway failure of the M2 device. Inset: microscopic image of the failed device. (b) Simulated thermal runaway failure of the M2 device. (c) Total current density at $t_1$. Conditions: $V_{DC,link}$ = 800 V, $T_{start}$ = 300 K, $R_G$ = 33 Ω, $V_{GS}$ = 15 V/0 V, $L_{par}$ = 25 nH, and $t_{SC}$ = 2.9 µs.

Fig. 16(a) shows the measured thermal runaway failure for the M2 device at $V_{GS,off}$ of 0 V. The inset microscopic image reveals a post-failure signature similar to that of M1 device, characterized by strong surface damage caused by Al metallization melting. Fig. 16(b) displays the simulated thermal runaway event for conditions similar to measurements. Although the simulated SC behaviour does not perfectly replicate the experimental results at extreme high temperatures due to the limitation in the high temperature physical models in simulator. The failure tendency of the simulated results matches with measured results and underlying mechanisms are consistent with measurements.

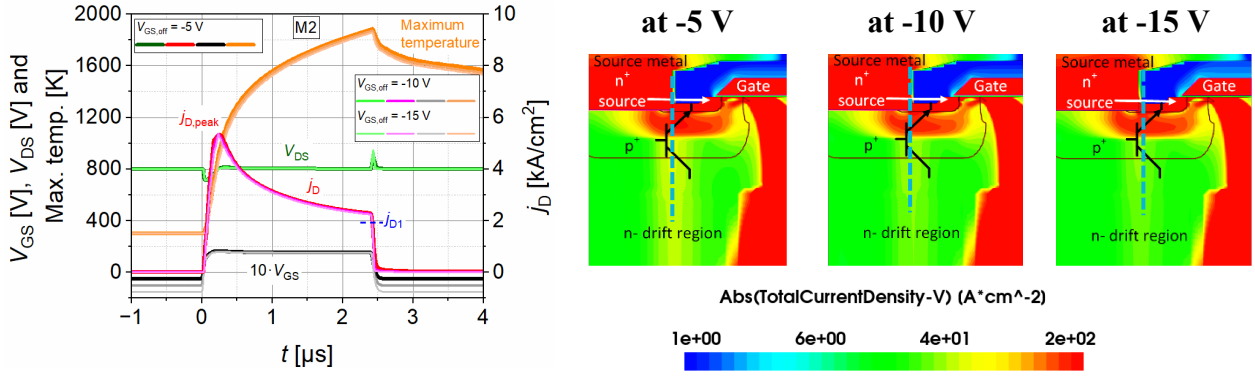
At $V_{GS,off}$ of 0 V, simulation result shows a pronounced drain current tail after SC is turned off, despite the gate being switched 0 V from preset conditions. This behaviour arises from strong reduction in $V_{th}$ at extreme junction temperature, which sustains partial channel conduction even after SC turn-off, see Fig. 16(c). The drain current tail, in combination with high DC-link voltage, imposes additional thermal stress on the device. This triggers a positive feedback loop in which higher temperatures enhance thermal generation. At such extreme temperatures, the parasitic npn bipolar junction transistor (BJT) could be activated and contributes one part of the remaining current tail as shown in Fig. 16(c). Once activated, this results in catastrophic device destruction and the current might focus to a single cell.




(a) Measured SC turn-off failure (b) Simulated SC turn-off failure (c)

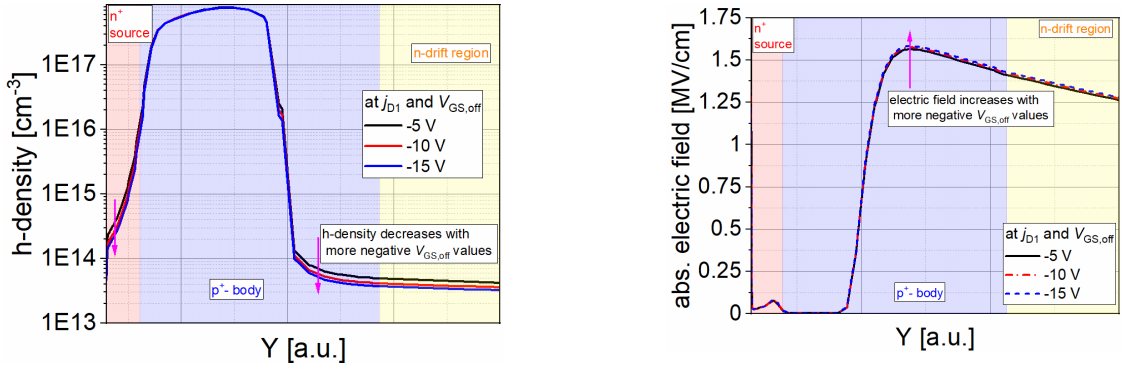
**Fig. 17.** (a) Measured SC turn-off failure. Inset: microscopic image of the failed device. (b) Simulated SC turn-off failure of the M2 device. (c) Total current density at $t_1$. Conditions: $V_{DC,link}$ = 800 V, $T_{start}$ = 300 K, $R_G$ = 33 Ω, $V_{GS}$ = 15 V/-15 V, $L_{par}$ = 25 nH, and $t_{SC}$ = 3.0 µs.

All M2 device with planar-gate consistently exhibited SC turn-off failure for $V_{GS,off}$ values ranging from -5 V to -15 V. A representative SC turn-off failure at $V_{GS,off}$ of -15 V and $t_{SC}$ of 3 µs, is shown in Fig. 17(a), together with corresponding TCAD simulation under comparable conditions in Fig. 17(b). In the simulation, SC turn-off failure occurs when the maximum SiC temperature reaches approximately 1900 K. At this extreme temperature, the voltage drop across the $n^+$-source and p-body junction forward-biases the base-emitter junction of the parasitic BJT, thereby initiating its activation and triggering an uncontrollable increase in the current [4]. Fig. 17(c) shows the simulated total current density distribution at $t_1$ [marked in Fig. 17(b)], clearly revealing conduction paths consistent with parasitic BJT activation. Moreover, once the parasitic BJT is activated, the current level becomes uncontrollable and the rising temperature further intensifies the failure process. Experimentally, SC turn-off failures in these conditions caused complete destruction of the TO packages. Post-failure microscopic analysis revealed extensive burning of the chip surface, with large regions of the Al metallization melted away.




(a) Simulated SC at different $V_{GS,off}$ (b) Total current density at different $V_{GS,off}$

**Fig. 18.** (a) Simulated SC behaviour of the planar-gate SiC MOSFETs for different $V_{GS,off}$ values. (b) total current density distribution for different $V_{GS,off}$ values at same current density $j_{D1}$. Conditions: $V_{DS}$ = 800 V, $R_G$ = 33 Ω, $T_{start}$ = 300 K, $L_{par}$ = 25 nH, $V_{GS,on}$ = 15 V, and $t_{SC}$ = 2.4 µs.




(a) Hole density at different $V_{GS,off}$ (b) Electric field at different $V_{GS,off}$

**Fig. 19.** (a) Hole density (b) electric field for different $V_{GS,off}$ values at same current density $j_{D1}$. For plots cut was across $n^+$ source, $p^+$-body and drift region, see Fig. 18(b).

Interestingly, the M2 SCWT increases with more negative $V_{GS,off}$ values, see Fig. 10. To gain insight into this trend, SC simulations were performed at different $V_{GS,off}$ values for 2.4 µs, as shown in Fig. 18(a). The corresponding total current density distribution at the same current density of $j_{D1}$ [marked in Fig. 18(a)] is displayed in Fig. 18(b). At $V_{GS,off}$ of -5 V, a clear latch-up of the parasitic npn BJT is observed. In contrast, at -10 V only a weak BJT activation occurs, while at -15 V the BJT remains effectively suppressed. This behaviour is governed by the gate-bias-dependent transient charging of the $p^+$-body during SC turn-off. At $V_{GS,off}$ of -5 V, the slower gate discharge and miller plateau enhance capacitive coupling between gate, drain and body regions. Consequently, a displacement current associated with rising $V_{DS}$ influences the p-body, leading to transient hole

accumulation and partial forward biasing of the parasitic BJT as shown in Fig. 19(a). With stronger negative gate bias, faster gate discharge results in stronger $p^+$-body depletion. The increased overvoltage at SC turn-off generates slightly higher electric field peak as shown in Fig. 19(b). This field enhances more carrier sweep-out, suppress the hole storage in the base, and prevents sufficient base current formation, thereby inhibiting parasitic BJT activation. Nevertheless, with further increase in SC pulse width, the maximum SiC device temperature rises due to higher energy dissipation and eventually leading to the SC turn-off failure at higher negative $V_{GS,off}$ values. All the failure types observed in this work for trench and planar-gate is summarized in Table 2.

**Table 2.** Failure types at different $V_{GS,off}$ between trench and planar-gate SiC MOSFETs.

| | **Failure types at 300 K** | | **Failure types at 425 K** | |
|---|---|---|---|---|
| **$V_{GS,off}$ values** | **Trench** | **Planar** | **Trench** | **Planar** |
| 0 V | Thermal runaway | Thermal runaway | Thermal runaway | Thermal runaway |
| -5 V | Post increased $I_{GSS}$ | SC turn-off | Thermal runaway | SC turn-off |
| -10 V | Post increased $I_{GSS}$ | SC turn-off | Post increased $I_{GSS}$ | SC turn-off |
| -15 V | Post increased $I_{GSS}$ | SC turn-off | Post increased $I_{GSS}$ | SC turn-off |

## Summary

The short-circuit (SC) robustness and failure mechanisms of SiC MOSFETs with distinct cell technologies from different manufacturers were systematically investigated through measurements supported by TCAD simulations. The observed $V_{GS}$ droop during the SC event is attributed to the increased gate leakage current from thermionic emission at very high junction temperatures.

Further, the trench-gate M1 device is strongly influenced by the applied negative gate bias prior to turn-on due to hysteresis effect. The M1 device exhibits the highest short-circuit withstand time (SCWT) at $V_{GS,off}$ of 0 V, with failure governed by thermal runaway. At more negative $V_{GS,off}$, SCWT decreases significantly due to increased $I_{GSS}$. TCAD simulations confirm that negative gate bias enhances the electric field at the interface between the dielectric and Al, thereby accelerating gate oxide degradation. In contrast, the planar-gate M2 device shows a distinct behavior: SCWT decreases when $V_{GS,off}$ is shifted from 0 V to –5 V, but subsequently increases for stronger negative bias, with the highest SCWT observed at –15 V. However, this bias exceeds datasheet limits, making $V_{GS,off}$ of 0 V the most reliable operating point within specification. Failure analysis reveals that at 0 V bias, M2 devices fail through thermal runaway, validated by TCAD simulations that show parasitic npn BJT activation after SC turn-off. At higher negative bias, SC turn-off failures dominate, also triggered by parasitic BJT latch-up as confirmed in simulations. Practically, these results indicate that for trench-gate devices, negative $V_{GS,off}$ should be minimized to reduce gate oxide field stress, whereas for planar-gate devices, moderate negative bias can improve the SCWT.

Overall, the results highlight a fundamental trade-off between gate oxide reliability in trench devices and parasitic BJT suppression in planar devices**.** These findings emphasize that SC robustness is not universal but highly dependent on device architecture, gate biasing strategy, and thermal limits. The combined measurement–simulation approach not only validates the physical failure mechanisms but also provides practical design guidelines for optimized gate drive strategies and reliability improvements in next-generation SiC MOSFET technologies.

## Acknowledgements

We would like to express our sincere gratitude to Detlef Conrad from Synopsys for his support to the understanding and implementation of the models investigated in this work.

**References**


[1] J. Sun, H. Xu, et. al., “Comparison and analysis of short circuit capability of 1200 V single-chip SiC MOSFET and Si IGBT,” in *Proc. 13th China Int. Forum Solid State Lighting*, Nov. 2016, pp. 42–45.

[2] A. Piccioni, “Repetitive Short-Circuit Ruggedness of Different of SiC MOSFETs channel Design” *in Proc. 2025 IEEE Int. Reliability Physics Symp.* (IRPS), Monterey, CA USA, Mar. 2025, pp. 2B.2 1-6.

[3] T. Ziemann, et. al., “Time resolved short circuit failure analysis of SiC MOSFETs,” in *Proc. 31st Int. Symp. Power Semiconductor Devices ICs (ISPSD)*, May 2019, pp. 219–222.

[4] K. Yao, et. al., “Investigation of SiC MOSFET Short-Circuit Failure Mechanisms Using Electrical, Thermal, and Mechanical Stress Analyses” in *IEEE transactions on Electron Devices*, Vol. 67, NO. 10, OCTOBER 2020, pp. 4328-4334.

[5] S. Jahdi, et. al., "Temperature and Switching Rate Dependence of Crosstalk in Si-IGBT and SiC Power Modules," *IEEE Transactions on Industrial Electronics,* vol. 63, no. 2, pp. 849-863, 2016.

[6] *TCAD Sentaurus Manual,* Synopsys Inc., Mountain View, CA, USA,2025.

[7] M. L. Mysore, et al., “Investigation of Overcurrent Turn-Off Robustness of 1200 V SiC MOSFETs”, will be published *in the conference 21st ICSCRM*, Raleigh, USA, Sep. 2024.

[8] A. Tsibizov, et. al., “Accurate temperature estimation of SiC power MOSFETs under extreme operating conditions,” *IEEE Trans. Power Electron.*, vol. 35, no. 2, pp. 1855–1865, Feb. 2020.

[9] JEDEC, "Guideline for evaluating Bias Temperature Instability of Silicon Carbide Metal-Oxide-Semiconductor Devices for Power Electronic Conversion," in *JEDEC JEP 184*, 2021.

[10] C. Schwabe, et. al., “SiC MOSFET threshold voltage stability during power cycling testing and the impact on the result interpretation,” *in Proc. 2023 IEEE Int. Reliability Physics Symp.* (IRPS), Monterey, CA USA, Mar. 2023, pp. p86.SiC1-6.

[11] T. Basler, et. al., “Practical Aspects and Body Diode Robustness of a 1200 V SiC Trench MOSFET” in PCIM Europe 2018, 5 – 7 June 2018, Nuremberg, Germany, pp. 536-542.

[12] B. Kakarla, “Short-Circuit Behaviour SiC MOSFETs” PhD thesis, ETH Zürich, 2021.

[13] J. Roig, et. al., “On the TCAD Modeling of Non-Permanent Gate Current Increase During Short-Circuit Test in SiC MOSFETs” *in Proc. 20th ICSCRM*, Sorrento, Italy, 2023, pp. 866-872.

[14] T. Aichinger, et. al., “Threshold voltage peculiarities and bias temperature instabilities of SiC MOSFETs” *Microelectronics Reliability*, vol 80, pp. 68-78, 2018.

[15] P. D. Reigosa, et. al., “Effects of short-circuit stress on the degradation of the $SiO_2$ dielectric in SiC power MOSFETs” *Microelectronics Reliability*, 88-90, pp. 577-583, 2018.