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Effects of Dynamic Reverse Bias Stress on the Blocking Capability of SiC MOSFETs

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Abstract. As a switching device, a SiC MOSFET operates under high-frequency and fast switching edges, facing severe reliability challenges in the dynamic mode. The degradation of electrical characteristics of SiC MOSFETs under high-voltage dynamic switching conditions is systematically investigated in this study. It is found that the threshold voltage and on-resistance exhibit initial transient degradation but they both stabilize, with changes remaining within ±5%. They show no dependence on the pulse amplitude, frequency, duty cycle, or temperature. This is attributed to the shielding effect of the P-well structure on the electric field in the channel region, which suppresses the continuous accumulation of interface charges. Additionally, the body diode voltage drop shows no significant shift, indicating that the dynamic reverse bias stress has no substantial impact on the n- drift region. However, the blocking capability can degrade and the degradation trajectory exhibits cross-coupling effects of multiple factors. Breakdown voltage degradation is positively correlated with the pulse voltage amplitude, frequency, duty cycle, and test temperature. As these stressors increase, carriers gain higher energy in the couple electro-thermal fields, leading to enhanced charge injection efficiency and trapping depth, increased interface charge accumulation, and localized electric field distortion, resulting in nonlinear degradation of the device's blocking capability. This study reveals the degradation mechanisms of SiC MOSFET under dynamic stress conditions, providing a theoretical basis for the optimization of interface engineering and dynamic operation adaptation design of high-reliability power devices.

Introduction

In practical applications, Silicon carbide (SiC) MOSFETs experience coupled electro-thermal stresses induced by the complex operating condition, imposing stringent reliability challenges on the devices. Currently, the evaluation of high-temperature voltage endurance in SiC MOSFETs primarily relies on constant-stress high temperature reverse bias (HTRB) testing. This involves applying a DC bias slightly below or equal to the rated voltage continuously at the maximum operating junction temperature to verify long-term stability of the blocking performance [1]. However, in the power conversion circuits where SiC MOSFETs operate as switching devices, their working mode requires high-frequency transitions among blocking, turn-on, conduction, and turn-off states. The drain-source voltage is not constant but instead a high-voltage, fast-switching, positively off-set, high-frequency repetitive pulse waveform [2]. Under such dynamic reverse bias (DRB) stresses, SiC MOSFETs face significantly more severe reliability challenges. The traditional constant-stress reliability evaluation methods, primarily developed for silicon (Si) devices, fail to adequately assess the insulation capability of the chip termination structures and gate oxides under high-frequency switching conditions specific to SiC devices [3].

The European power electronics center's testing standard AQG-324 emphasizes the necessity of conducting DRB test to evaluate the impact of high-frequency pulse stress on the performance stability of SiC devices. Building upon the traditional constant-bias HTRB tests, the standard establishes fundamental principles and testing conditions for dynamic bias evaluation [4]. Room-temperature DRB testing has also been recommended as an additional qualification requirement in standards such as AEC-Q101 [5]. To address reliability challenges on SiC devices under dynamic

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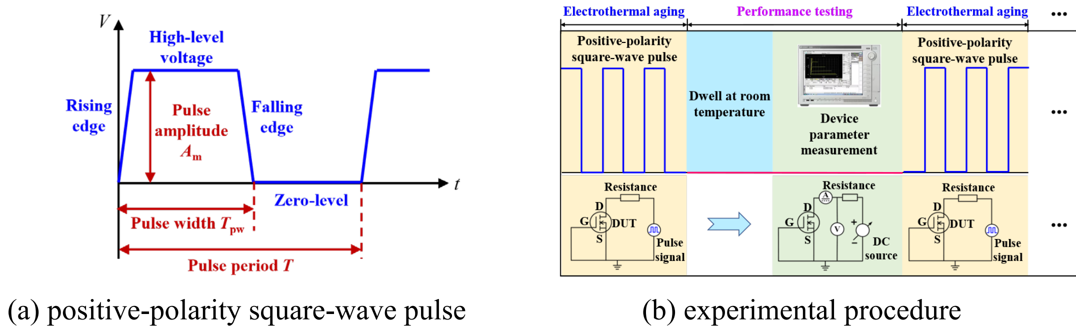
operating conditions, researchers worldwide have conducted some studies. A self-developed DRB test platform with adjustable drain-source voltage slew rate ($\mathrm{d}V_{DS}/\mathrm{d}t$) was reported in [6]. Using this platform, the impact of dynamic drain-source stress on the electrical property of SiC MOSFETs was investigated. The results demonstrated increases in both threshold voltage V_{th} drift and body diode forward voltage drop V_{SD}. Through simulation analysis, the degradation behavior was attributed to enhanced hole trapping in the gate oxide layer above the JFET region and body diode area. Simulation studies on the failure mechanisms of SiC MOSFETs under extreme $\mathrm{d}V_{DS}/\mathrm{d}t$ switching conditions were reported in [7]. The results revealed that the charging/discharging current in the P-well of the main junction region generates high transient electric fields in the gate oxide at the boundary between the transition zone and active area. These findings underscore that chip design must account for not only static voltage endurance but also transient blocking capability under DRB stresses like in applications.

This paper investigates the influences of main DRB variables, including pulse amplitude, pulse frequency, duty cycle, and temperature, on the blocking capability reliability of a 1200 V, 4H-SiC MOSFETs by monitoring the change of electrical parameters during the aging process. The post-stress recovery characteristics of device performance are also tracked, and the difference in reliability degradation mechanisms between the HTRB and DRB conditions is analyzed. The findings are expected to provide insights which can be used for the design, manufacturing, and application validation of SiC MOSFETs from a reliability testing perspective.

Experiment Setup

The DRB stress reliability tests on SiC MOSFETs are conducted using the commercial test platform. As illustrated in Fig. 1, the experimental procedure involves the electrothermal aging and performance testing phases. The parameter measurement circuit is exemplified by the blocking property test.



(a) positive-polarity square-wave pulse (b) experimental procedure

Fig. 1. Program for dynamic reverse bias test.

During the aging phase, a positive-polarity square-wave pulse voltage is applied as the drain-source stress to the device under test (DUT), with adjustable pulse amplitude, frequency, and duty cycle. The voltage slew rate ($\mathrm{d}V_{DS}/\mathrm{d}t$) at pulse rising and falling edges is 50 V/ns. And the case temperature is set according to test requirements. To eliminate interference from active gate stress introduction, the gate-source terminals of DUT are maintained in short-circuited state. After continuous aging for a specified duration, the applied electrothermal stress is removed, and the DUT is allowed to cool to room temperature (25±1 °C). Electrical parameters are then measured using the Agilent B1505A power device analyzer. The test program described here is repeated until the cumulative DRB stress duration reached 168 hours. Three DUTs are tested under each condition.

To differentiate the degradation sites in the chip under DRB stress from an electrical testing perspective, the cell structure is partitioned into the functional areas correlated with specific evaluation parameters in Fig. 2. The threshold voltage (V_{th}) is primarily associated with the state of channel region and its overlaying gate oxide layer. For 1200V SiC MOSFETs, the drift region resistance constitutes the dominant component (40%-50%) of the total on-resistance (R_{DSon}), followed by the channel resistance (30%-40%). The conduction performance of the DUT is primarily governed by the health condition of the two regions. Under blocking conditions, reverse

bias stress in the active area is sustained by the PN junction formed between the P-well region and the N- drift region. The body diode forward voltage drop (V_{SD}) can serve as a key indicator for assessing the structural integrity of the critical drift region. The blocking capability of the DUT stems from the widening and overlapping of the depletion layer in the termination field-ring PN junctions. The breakdown voltage (BV) is predominantly determined by the design and integrity of edge termination structure.

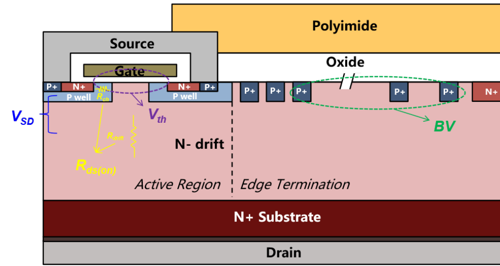


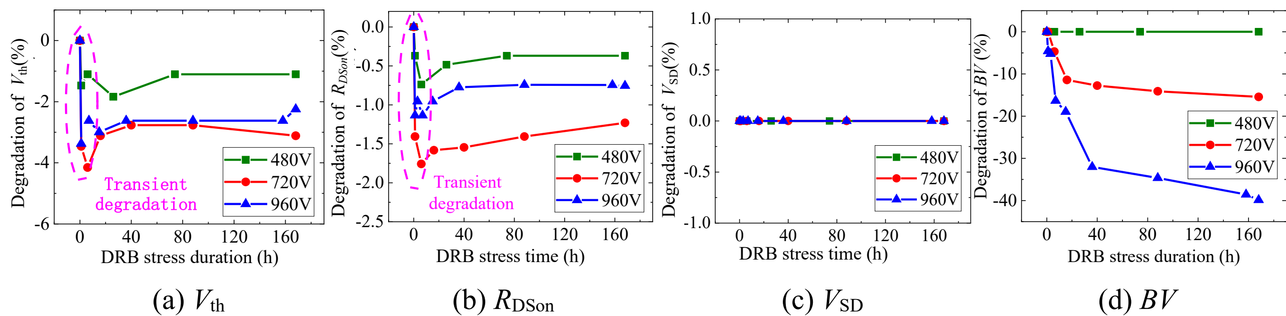
Fig. 2. Correlation between device cell structure and key electrical parameters.

This study is conducted on 1200 V SiC MOSFET devices, where ten samples from the same production batch undergo HTRB testing with stress conditions V_{DS}=960 V and T_J=175 °C. Throughout the 168 hour aging period, all DUTs maintained stable blocking performance without exhibiting significant BV degradation.

Result and Discussion

Impact of Pulse Voltage Amplitude.

The impact of pulse magnitude (A_m) is investigated through the application of square-wave pulse voltages at three discrete amplitude levels (80%, 60%, and 40%) relative to the rated operating voltage (1200 V). Meanwhile, the remaining DRB stress variables are maintained constant with a pulse frequency of 25 kHz, duty cycle of 50%, and ambient temperature of 30 °C during the testing period.The time-dependent degradation characteristics of device performance parameters under different A_m values are shown in Fig. 3.



(a) V_{th} (b) R_{DSon} (c) V_{SD} (d) BV

Fig. 3. Time-dependent degradation of device performance parameters under different A_m values.

The degradation ratio is quantitatively defined as the ratio of the difference between the measured values at each time point and their initial values with respect to the initial values, serving as a metric to characterize the performance attenuation of devices under specific stress conditions. A positive degradation indicates that the measured value exceeds the initial value, meaning the performance parameter increases over time, while a negative value signifies that the measured value falls below the initial value, reflecting a decreasing trend of change. Through normalization, this metric eliminates individual variations, enabling effective comparison of degradation behaviors under different stress conditions.

As shown in Fig. 3(a)-(c), with increasing stress time, V_{th} and R_{DSon} of the device exhibit consistent degradation trends. During the first hour of stressing, the degradation is relatively rapid before gradually stabilizing. V_{SD} shows no observable degradation throughout the period. Under DRB testing, the N- drift region serves as the primary voltage-bearing zone within the active area.

The absence of degradation in V_{SD} indicates this region remains unaffected, implying no variation occurred in the drift region resistance. The observed synchronous short-term degradation of both V_{th} and R_{DSon} could predominantly be associated with the channel region.

At gate oxide/SiC interface near the channel region, an electric-field-induced charge transfer phenomenon can occur [8]. Under high drain-side electric fields, positive charges (holes) generated by impact ionization are transported to the SiO_2/SiC interface, with some becoming trapped there. These trapped charges effectively act as an additional forward bias applied to gate, enhancing channel conductivity and leading to transient reductions in both V_{th} and R_{DSon}. Although DRB stress affects the channel region to some extent, the shielding effect of the P-well on nearby electric field prevents sustained degradation progression [9]. The observed degradation remains to be transient and limited in magnitude, with no discernible dependence on the pulse amplitude.

In contrast to V_{th} and R_{DSon}, the degradation of BV exhibits pronounced dependence on A_m, as illustrated in Fig. 3(d). With the same stress duration, the degradation of BV shows a nonlinear increasing trend with elevated pulse amplitudes. At 480 V, BV exhibits no measurable degradation. At 720 V, the degradation rapidly exceeded 10% before stabilizing towards 15-20%. At 960 V, the degradation of BV reached 40%.

This suggests that when A_m exceeds a critical value ranging from 480 V to 720 V for the device under study in this paper, the high electric field between the drain and source imparts sufficient kinetic energy to charge carriers, thereby triggering impact ionization process. As shown in Fig. 4, a high hole concentration is generated near the field oxide/SiC interface within the termination region. The electric field induces hole injection into the interface, where the holes are captured by deep-level traps. These trapped charges cause field distortion, thereby degrading the blocking capability of the terminal field-ring PN junction [10]. Further increasing the pulse voltage amplitude enhances the vertical electric field at field oxide/SiC interface, leading to improved charge injection efficiency as well as deeper trap penetration. This intensified interface charge accumulation effect significantly degrades the BV stability of SiC device.

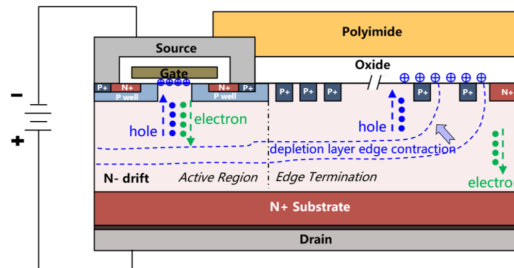


Fig. 4. Mechanism analysis of breakdown voltage degradation in devices.

Impact of Pulse Voltage frequency and duty cycle.

SiC MOSFETs are widely employed in high-frequency applications such as the photovoltaic inverters and industrial motor drives, where the devices are consistently subjected to voltage transients during switching operations. It is therefore essential to investigate degradation behavior for devices under DRB stress with varying frequencies and duty cycles.

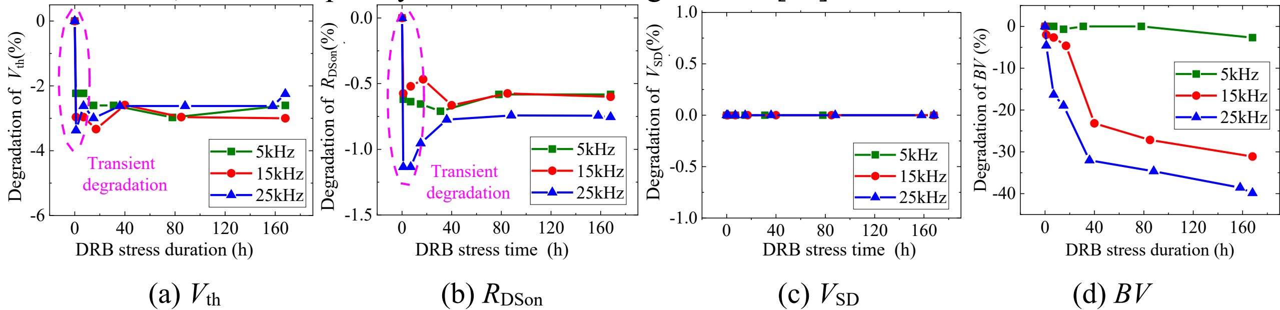
To investigate the influence of pulse frequency on device electrical parameter degradation, the experiment was conducted with pulse frequencies set at 5 kHz, 15 kHz, and 25 kHz, while maintaining constant amplitude, duty cycle, and temperature at 960 V, 50%, and 30 °C, respectively. The time-dependent degradation characteristics of device performance parameters under varying frequencies are shown in Fig. 5.

As shown in Fig. 5(a)-(c), similar to the case under different voltage amplitudes, V_{th} and R_{DSon} of the device exhibit a brief degradation followed by stabilization with increasing stress time under different pulse frequencies. The degradation is limited (within 5%) and shows no dependence on pulse frequency. Meanwhile, the voltage drop of V_{SD} shows no signs of degradation.

In contrast, the degradation of BV demonstrates significant dependence on the pulse frequency, as shown in Fig. 5(d). The degradation of BV is consistent across different pulse frequencies - it

increases with stress time and becomes more pronounced at higher pulse frequencies. Under dynamic reverse bias stress at 5 kHz, the degradation of BV after 168 h is 2.7%, indicating negligible degradation. After the same effective stress time, the drop of BV reaches 31% at 15 kHz and 40% at 25 kHz.

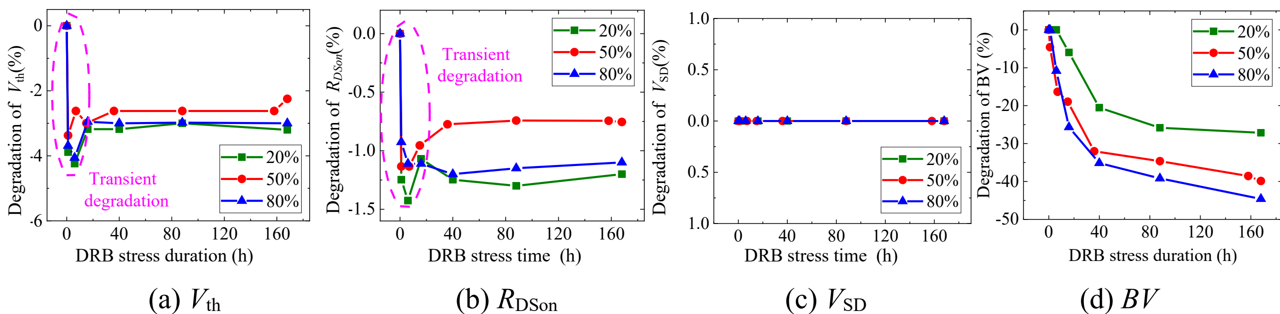
At low pulse frequencies (0-5 kHz), the device experiences fewer high-electric-field stress events per unit time. This allows more time for charges trapped in deep-level traps to relax, with some detrapping occurring during stress intervals, thereby mitigating charge accumulation and its modulation of the electric field. As the pulse frequency increases, although the total duration of high and low voltage levels remains unchanged, the number of voltage transitions per unit time rises significantly. This reduces the available charge relaxation time, enhances residual charge accumulation, and consequently accelerates BV degradation [11].



(a) V_{th} (b) R_{DSon} (c) V_{SD} (d) BV

Fig. 5. Time-dependent degradation of device performance parameters under different frequencies.

To investigate the influence of pulse duty cycle on the device electrical parameter degradation, square-wave pulses with duty cycles of 20%, 50%, and 80% were applied under fixed amplitude, frequency, and temperature conditions of 960 V, 25 kHz, and 30 °C. The time-dependent degradation characteristics of the device performance parameters under different duty cycles are shown in Fig. 6.



(a) V_{th} (b) R_{DSon} (c) V_{SD} (d) BV

Fig. 6. Time-dependent degradation of device performance parameters under different duty cycles.

As shown in Fig. 6(a)-(c), the degradation behaviors of V_{th}, R_{DSon} and V_{SD} under different pulse duty cycles are consistent with those observed under various pulse frequencies. V_{th} and R_{DSon} show a brief degradation at the initial stage of stressing before settling down, with the level of degradation remaining within 5%. No duty cycle dependence was observed. Meanwhile, no degradation in V_{SD} was detected under any of the tested duty cycle conditions.

A positive correlation is observed between BV degradation and the pulse duty cycle, as shown in Fig. 6(d). After the same stress duration, the degradation of BV increases with higher duty cycles. When the duty cycle rises from 20% to 50%, the degradation increases from 27% to 40%. Beyond 50% duty cycle, the degradation growth slows. The pulse duty cycle represents the proportion of high-level voltage duration within each stress cycle. A higher duty cycle extends the time during which the device is under high reverse bias electric field. This prolongs carrier acceleration in the electric field, increasing the probability of impact ionization. More charges are driven by the field to fill deep-level traps and form fixed charges. The resulting charge accumulation distorts the local electric field, macroscopically leading to an increased BV degradation.

Impact of Temperature.

Given that SiC MOSFET devices may operate in high-temperature harsh environments, their dynamic reliability under such conditions warrants thorough investigation. To examine the impact of dynamic reverse bias stress on the degradation of electrical parameters at different temperatures, tests were conducted at 30 °C, 100 °C, and 175 °C. Other stress conditions (amplitude, frequency, and duty cycle) were set to 960 V, 25 kHz, and 50%, respectively. Figure 7 shows the degradation of the SiC MOSFET performance parameters as a function of stress time under these temperature conditions.

As shown in Fig. 7(a)-(c), under different test temperatures, V_{th} and R_{DSon} of the device exhibit an initial brief degradation followed by stabilization with the increase of stress time. Owing to the protective effect of the P-well on the channel region in the active area, the overall degradation remains limited. Meanwhile, V_{SD} shows no signs of degradation.

In contrast, a positive correlation is observed between the degradation of BV and temperature, as shown in Fig. 7(d). After 168 hours of stress at 30 °C, the degradation reaches 40%. At 100°C under the same electrical stress conditions and duration, the drop of breakdown voltage increases to 50%, while at 175 °C, the degradation rises to 55%. Under the same electric field strength near the drain-source region induced by the pulsed voltage, elevated temperature enhances the thermal motion of carriers, increasing the probability of high-energy attainment and intensifying the hot carrier injection effect. This leads to deeper charge trapping and reduced detrapping likelihood. Furthermore, higher temperatures significantly lower the activation energy for trap generation in the oxide layer, accelerating the formation of defects at the SiO_2/SiC interface and within the oxide. These defects act as charge trapping centres, capturing carriers and forming fixed charges, which distort the local electric field and ultimately degrade the breakdown robustness of the device.

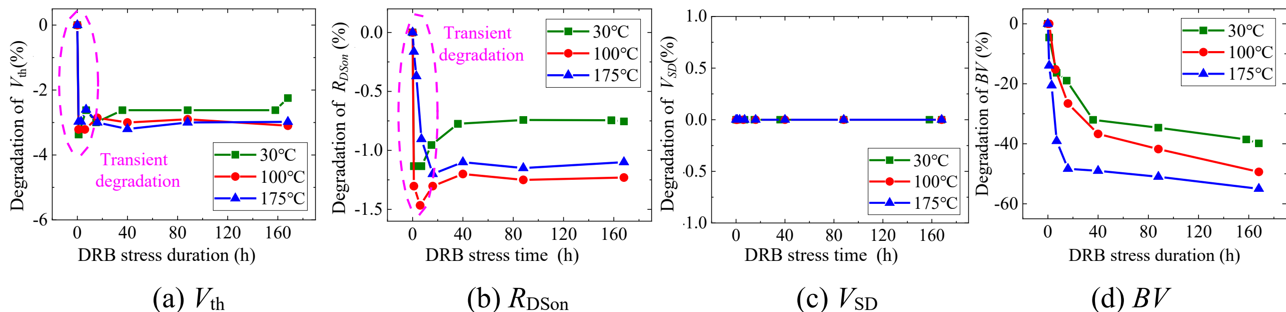
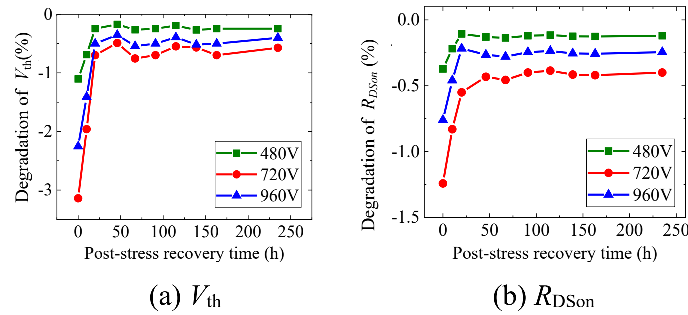


Fig. 7. Time-dependent degradation of device performance parameters under different temperatures.

Post-stress Recovery Behavior of Device.

After removing the dynamic reverse bias stress, the recovery of the SiC MOSFET's electrical performance was tracked for over 200 h to determine the nature of the parameter degradation. As mentioned in the previous results, V_{th} and R_{DSon} showed no significant dependence on pulse amplitude, frequency, duty cycle, or temperature. Therefore, the recovery behavior of V_{th} and R_{DSon} under different pulse amplitudes is presented here as an example, with the results shown in Fig. 8.

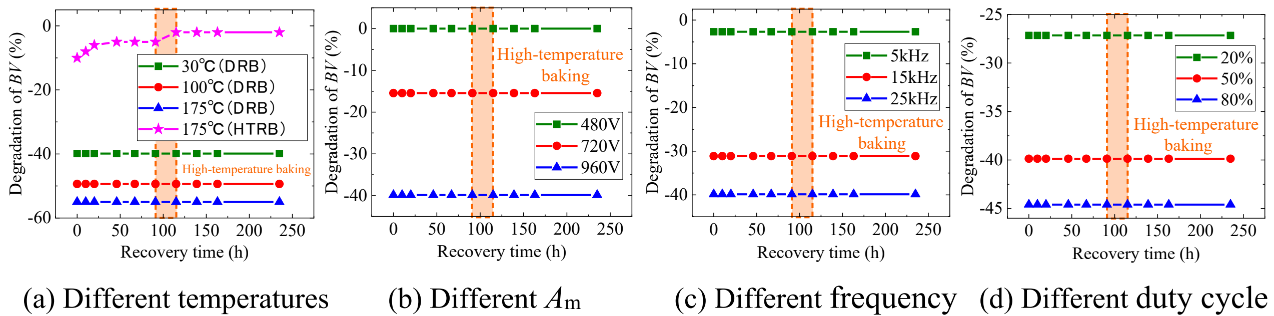
During the initial recovery phase (within 24 h), the degradation of both V_{th} and R_{DSon} decreased rapidly. After 50 h of recovery, the parameters entered a saturated state, with the residual degradation stabilizing around 0.5%. After stress removal, both V_{th} and R_{DSon} demonstrated a self-recovery capability, with a distinct time-dependent characteristic. This behavior is attributed to the release of trapped charges at the SiO_2/SiC interface in the channel region. The P-well structure in the SiC MOSFET shields the electric field in the channel, resulting in shallow charge injection and limited accumulation during dynamic reverse bias stress. Under room-temperature storage after stress removal, the shallow trapped charges are released through lattice vibrations or thermal motion, leading to a gradual recovery of carrier concentration and mobility in the channel region.



(a) V_{th} (b) R_{DSon}

Fig. 8. The degradation of threshold voltage and on resistance varies with recovery time.

The recovery of breakdown voltage under different dynamic stress conditions is shown in Fig. 9. For comparison, Fig. 9(a) also includes the breakdown voltage recovery behavior after constant reverse bias stress (HTRB, under V_{DS} = 960 V and T_J = 175 °C).



(a) Different temperatures (b) Different A_m (c) Different frequency (d) Different duty cycle

Fig. 9. Recovery of breakdown voltage under different dynamic stress variables.

After conventional constant-stress HTRB tests, degraded SiC MOSFETs can gradually recover under room-temperature storage, and the level of degradation further decreases after high-temperature baking. In contrast, devices degraded under dynamic reverse bias stress show no recovery in breakdown voltage - neither after room-temperature storage nor high-temperature baking.

The difference in breakdown voltage recovery behavior after constant and dynamic reverse bias stressing is primarily attributed to the charge injection depth and the types of traps involved. Under constant bias, the electric field is relatively stable, and charge injection is mainly confined to shallow-level traps near the SiO_2/SiC interface. These traps have low energy barriers, allowing captured charges to be gradually released via thermal relaxation at room or elevated temperatures, thereby restoring the breakdown voltage close to the initial value. Under dynamic stress, however, the high-frequency pulsed electric field induces higher-energy charge injection, resulting in greater injection efficiency and deeper trapping [11]. Deep-level traps have higher energy barriers and require larger de-trapping activation energies, making charge release difficult even after high-temperature baking. This leads to irreversible degradation of the breakdown voltage.

To improve the degradation of blocking capability under DRB stress, scholars have proposed recommendations from the perspective of optimizing the chip cell structure design. These include inserting isolation rings in the transition zone between the active and terminal regions to shunt transient currents [7], or introducing local buffer layers in the edge termination area to suppress hole injection [12], thereby enhancing the robustness of the device.

Conclusion

This study experimentally investigates the possible degradation of the electrical characteristics of SiC MOSFETs under high-voltage fast-switching dynamic stressing. The main conclusions are as follows:

1) With increasing stress time, the threshold voltage and on-resistance exhibit brief degradation before stabilizing. The extent of degradation is limited and shows no dependence on pulse amplitude, frequency, duty cycle, or temperature, which is primarily attributed to the electric field

shielding effect of the P-well near the channel region. The body diode voltage drop shows no degradation, indicating that the dynamic reverse bias stress does not affect the N- drift region. After stress removal, both the threshold voltage and on-resistance demonstrate self-recovery behavior with distinct time-dependent characteristics.

2) The degradation of the breakdown voltage shows a positive correlation with pulse amplitude, frequency, duty cycle, and temperature. As any of these factors increases, carriers gain more energy from the coupled electro-thermal fields, enhancing charge injection efficiency and trapping depth. This intensifies interface charge accumulation, leading to local electric field distortion and a significant reduction in the breakdown voltage. After stress removal, neither room-temperature storage nor high-temperature baking can reverse the negative shift of breakdown voltage.

3) The difference in breakdown voltage recovery behavior under constant and dynamic reverse bias conditions stems primarily from the charge injection depth and the trap types involved. Under constant stress, charge injection is confined to shallow-level traps near the interface, and the trapped charges can be released via thermal relaxation at room or elevated temperatures, making the degradation reversible. Under dynamic stress, the high-frequency pulsed electric field enhances the energy and depth of charge injection. Deep-level traps have higher energy barriers and require larger detrapping activation energies, preventing charge release even after high-temperature baking and resulting in irreversible breakdown voltage degradation.

Acknowledgement

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