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Enhanced Gate Oxide Reliability in Vertical SiC Power MOSFETs via Optimized Processing and Screening

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Abstract. Intrinsic gate oxide reliability of silicon carbide (SiC) power MOSFETs has improved significantly over the years. Nonetheless, to achieve a level of overall reliability comparable to silicon devices, it is essential to address extrinsic defects that could introduce early life failures in the gate oxide of SiC devices. Gate screening can be performed to eliminate these early life failures; however, proper optimization of screening methodology is required to maximize the useful life of the devices while maintaining a low failure rate and avoiding potential adverse effects, such as threshold voltage instability, due to the high gate stress during screening. In this paper, we demonstrate enhanced intrinsic and extrinsic reliability of gate oxide across two distinct wafer fabrication facilities, achieved through optimized processing and screening methodologies.

Introduction

Silicon carbide (SiC) vertical power MOSFETs offer efficient switching, thanks to their wide-band gap leading to lower on-resistance at a similar operating voltage as compared to their silicon counterparts [1]. Therefore, ensuring excellent reliability has become a primary focus for SiC-based devices. Although gate oxide intrinsic reliability has shown great improvements over the years, there has not been much discussion about extrinsic reliability until recently [2-3]. In Ref. [2], it has been argued that gate oxide screening should be performed on SiC MOSFETs that suffer several orders of magnitude higher failure rate due to larger extrinsic populations when compared with Si MOSFETs. This paper addresses gate oxide reliability across all three phases of the bathtub curve, addressing early life failure regime from extrinsic defects, constant failure regime due to random failures, and wear-out failure regimes due to intrinsic failures. It also demonstrates enhanced gate oxide reliability obtained through highly optimized processing and screening in both 150 mm and 200 mm wafer fabrication/process technologies.

Overview of Gate Screening through a Bathtub Curve

Figure 1 illustrates a schematic representation of the screening effect on the failure rate of the gate oxide over time in terms of a bathtub curve. Despite proper screening of the devices, random failures can still occur due to the stochastic thermal process represented by the Weibull shape parameter value of $\boldsymbol{\beta} \sim 1$ within the screened population (see Fig. 1a-b). Once the devices are screened down to the random failure regime at the bottom of the bathtub curve, additional screening will reduce the useful life of the devices (see Fig. 1c). Therefore, it is essential to develop an optimized screening methodology that effectively eliminates the early extrinsic population, while minimizing the reduction of useful lifetime. In addition to useful lifetime consideration, the screening method should not be so overly aggressive as to produce large gate threshold instabilities, or cause impact-ionization-driven negative threshold voltage drift (see Fig. 2) [4-6].

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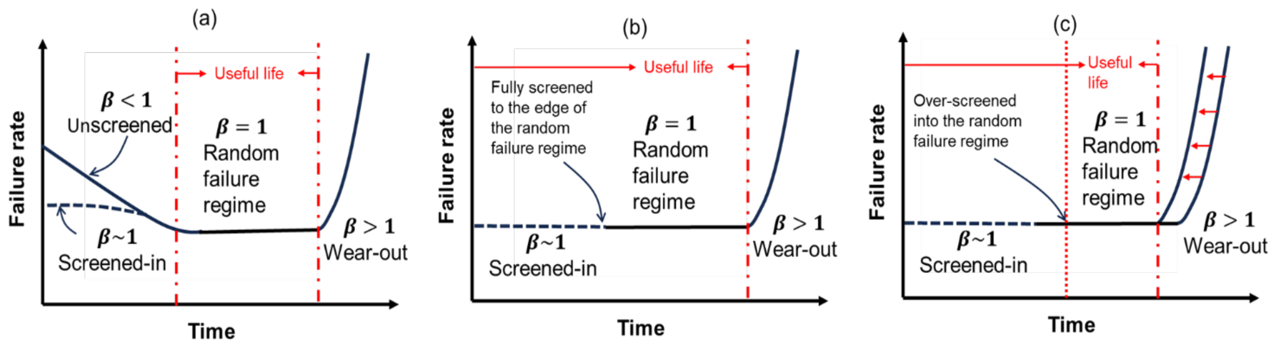

Fig. 1. Schematics of bathtub curves showing all three phases of device lifetimes in the context of gate oxide reliability under different scenarios of gate screening – (a) partially screened population (b) optimally screened population (c) overly screened population.

It has been shown in Ref. [4] that over screening with high gate bias stress above a critical electric field can lead to bandgap impact ionization in SiO_2 as shown in Fig. 2. Due to impact ionization, holes can be generated which then travel back towards SiC/SiO_2 interface and get trapped near or at the interface resulting in a semi-permanent negative drift in threshold voltages. Recent charge pumping experiment showed higher charge pumping current with high gate stress indicating generation of new interface traps [5]. Gate Hall measurements exhibited mobility degradation under high gate stress along with the increase in interface traps [6]. Therefore, a proper optimization of screening methodology is required to obtain benefits of screening without causing unwanted adverse effects.

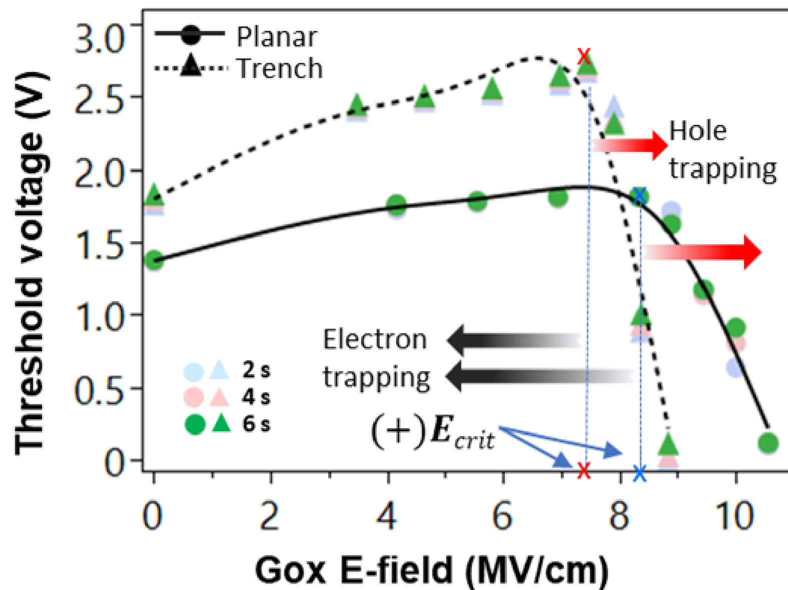

Fig. 2. Negative threshold drift under high positive bias due to hole generation via impact ionization and trapping (reproduced from reference [4]).

Results of Gate Screening Experiment in 150mm Wafer Fabrication Facility

A highly optimized screening methodology has been developed by Wolfspeed to effectively eliminate defective populations, considering the aforementioned factors. Figure 3 illustrates the decrease in failure rate down to < 0.5 parts per billion device hours (ppb/device-hour), as derived from a large volume of devices subjected to gate screening stress on the 150 mm wafer fabrication process. In order to study the lifetime and failure rate at the operating conditions, approximately 1600 screened devices were stressed under constant bias time-dependent dielectric breakdown (TDDB) test below the critical field (defined in Fig. 2) over a wide range of fields and temperatures, allowing for the extraction of electric field acceleration and activation energy for the thermochemical model [6].

TDDB tests are performed at electron trapping regime as indicated in Fig. 2 to avoid impact ionization (hole trapping) at higher electric fields that overestimate the lifetime projections at the operating conditions under low electric field.

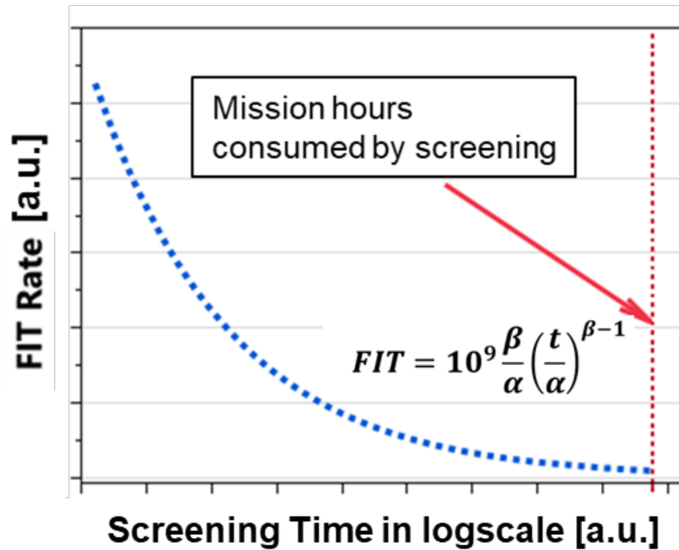

Fig. 3. Measured FIT observed during screening of gate oxide from a large number of devices.

Figure 4 shows the lifetime projection under typical operating conditions for two different populations – a wear-out region with $\boldsymbol{\beta} > 1$ and a random failure region with $\boldsymbol{\beta} \sim 1$. This demonstrates that all defective populations with $\boldsymbol{\beta} < 1$ are screened out and the devices are well within the random failure regime. When the lifetime was estimated for a typical mission condition, the projection from the $\boldsymbol{\beta} = 1$ branch indicates a low failure probability value of ~ 1 ppb for automotive mission maximum. In case of an industrial application (e.g. solar), that failure probability at mission maximum (~100 years) can be ~100 ppb.

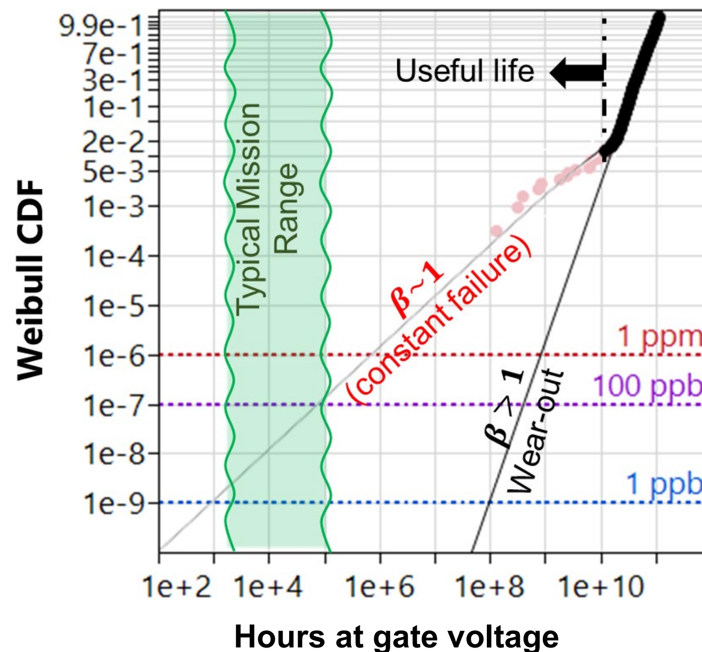

Fig. 4. Lifetime projection from TDDB data collected (1.6k devices from 150 mm process technology) over a wide range of voltages and temperatures using the thermochemical model with a defective subpopulation.

After calculating failure-in-time (FIT) rate of the screened-in devices at the typical mission condition from TDDB study in Fig. 4 and FIT rate of the screened-out devices from the gate screening

study in Fig. 3, a bathtub curve is constructed which features a decreasing failure rate initially, a constant failure rate in the middle and a wear-out failure rate at the end, analogous to an ideal reliability bathtub curve (see Fig. 5). To the best of our knowledge, a gate oxide reliability bathtub is presented for the first time for SiC devices utilizing data acquired from gate screening and TDDB tests. It is crucial to emphasize that early life failures ($\boldsymbol{\beta} < 1$) have been completely screened-out prior to shipping. As a result, shipped devices exhibit only a low constant failure rate from the onset and maintain this rate during the entire operational life. However, it is important to note that the minimum failure in time (FIT) achieved after optimized screening is determined by the random failure rate, which could potentially be improved by optimizing process technology.

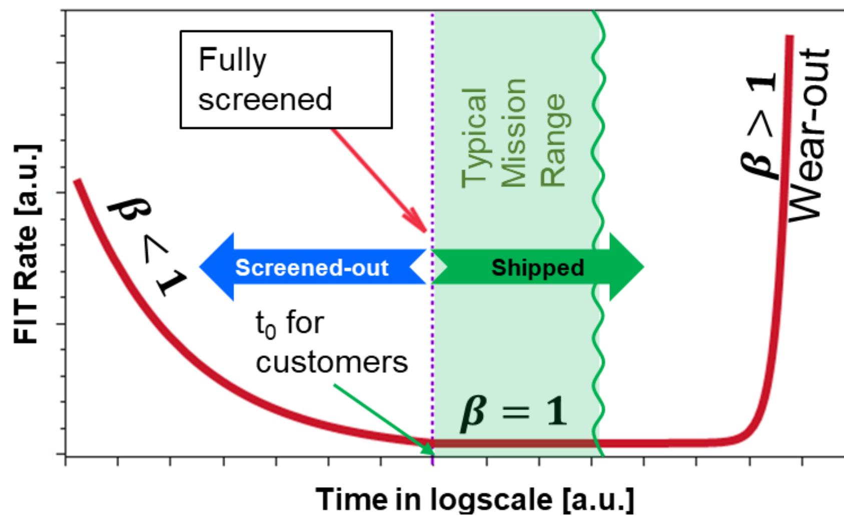

Fig. 5. Gox reliability bathtub curve constructed by combining gate screening failure data and TDDB data from Fig. 3 and 4.

Enhanced Reliability of Gate Oxide in 200mm Wafer Fabrication Facility

Analogous to the study in 150 wafer fabrication facility, a targeted TDDB study has been performed to evaluate the effectiveness of screening methodology in 200 mm where further enhancement of gate oxide reliability has been achieved by optimizing processing and screening. Figure 6 presents TDDB data for approximately 900 screened-in packaged devices over a wide range of temperatures (125°C to 200°C) and at multiple constant gate voltages. It is noteworthy to mention again that TDDB tests were performed in the electron trapping regime, ensuring that the failure mechanism under TDDB conditions remains consistent with the operating conditions at low electric fields. Hence, thermochemical (Linear E) model is utilized to project lifetime at the operating condition. The extracted thermochemical model parameters for SiC/SiO_2, namely Si-O bond strength at zero field (ΔH_0) and effective dipole moment (P_{eff}) are found to be 1.74eV and 13.8eÅ, respectively. These values are comparable to those reported for Si/SiO_2 [7] devices, indicating the gate oxide quality and reliability in SiC/SiO_2 devices are similar.

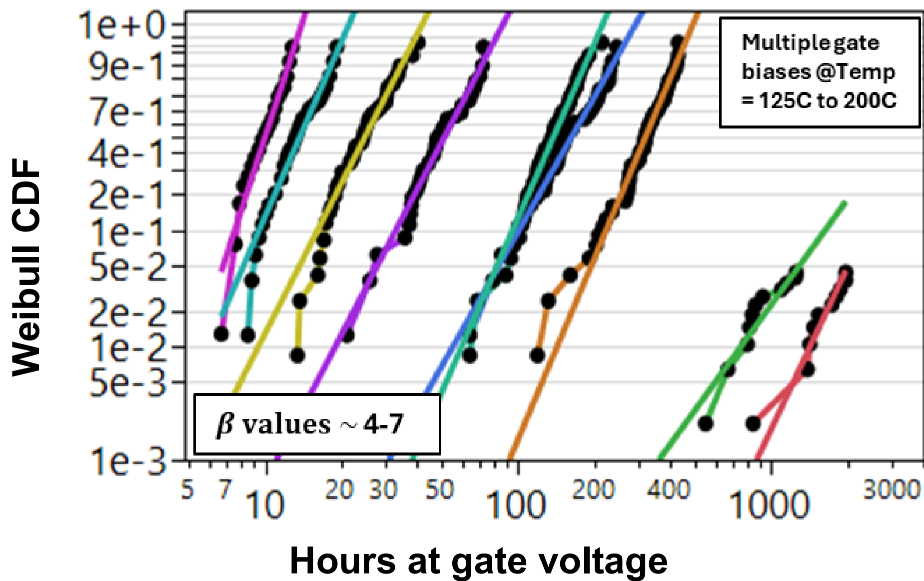

Fig. 6. Cumulative failure distribution over time from a TDDB test of ~900 devices from 200 mm process technology.

Additionally, approximately 3400 screened devices were stressed under TDDB to extract information about the extrinsic population. Figure 7 shows the lifetime projection for the 4300 tested devices under typical operating conditions, showing <<1 ppb at even 100 years. It is noteworthy that the percentage of random failure population is reduced by at least ~100x as compared to the 150 mm technology. In addition, all of the defective population is now being screened, to the detection level of this study.

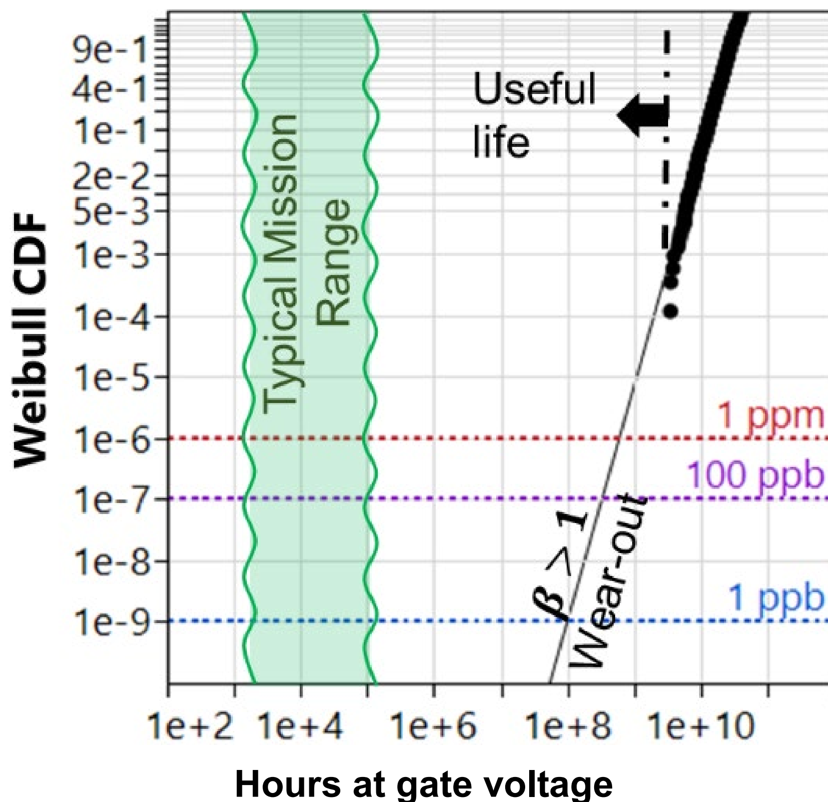

Fig. 7. Lifetime projection from TDDB data collected (4.3k devices from 200 mm process technology) over a wide range of voltages and temperatures showing ~100x decrease in random failures.

Summary

We provide an overview of gate oxide screening utilizing a bathtub curve for gate oxide reliability and show how excessive screening can impact intrinsic device lifetimes and threshold voltage stability. Through accelerated lifetime testing, we demonstrate that optimized gate screening, along with improved processing and quality measures for MOSFETs fabricated on 150mm and 200mm wafers, result in highly reliable gate oxide and extremely low failure rates across two distinct manufacturing facilities.

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