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Cumulative Threshold Voltage Shift Induced by Surge Current in Planar SiC MOSFETs after Bipolar Gate Switching Stress

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Abstract. In this work, we report the impact of combined surge current stress and bipolar gate switching stress (GSS) on the threshold voltage (V_{th}) shift of planar SiC MOSFETs. The V_{th} shift exhibits a strong dependence on the sequence of these two applied stresses. It is found that both the surge current stress and GSS can separately result in a positive shift in V_{th}, and the V_{th} shift is cumulatively aggravated in the combined stresses only if the bipolar GSS is applied first. This is attributed to the generation of new defects during the bipolar gate switching, which act as trap centers for subsequent surge stress. This finding reveals the cumulative damage characteristics of SiC MOSFETs under complex operating conditions.

Introduction

SiC MOSFETs have demonstrated excellent performance for high-voltage power conversion applications owing to their superior characteristics, leading to their wide adoption in electric vehicle traction inverters, aerospace power systems, and solar power converters [1-3]. However, threshold voltage instability in SiC MOSFETs remains a concern affecting device reliability and performance, primarily due to charge trapping at the SiC/SiO_2 interface [4].

In industrial applications, the switching transients associated with capacitors and inductors give rise to surge currents that can reach magnitudes several times the rated current of SiC MOSFETs. Surge current represents a common electrical stress condition that can lead to a shift in the V_{th} of SiC MOSFETs [5]. On the other hand, in practical high-power converter applications, to ensure the stability and efficiency of power systems, applying a negative turn-off voltage is an effective way to prevent false turn-on in SiC MOSFETs. Therefore, bipolar gate switching stress is consistently applied to the gate electrode. Under bipolar gate switching operation, the switching cycle emerges as an additional influencing factor, contributing to a more severe degradation of the V_{th} compared to static gate stress conditions [6]. In previous studies, the V_{th} instability of SiC MOSFETs under either bipolar GSS or surge current stress has been extensively investigated separately [5,6]. However, in real-world applications, SiC MOSFETs are often subjected to combined stress conditions, yet their impact on V_{th} remains unclear. In this work, the influence of combined stress on V_{th} degradation is systematically investigated.

Experimental Details and Results

For comparison, two Measurement-Stress-Measurement (MSM) procedures were designed to evaluate the impact of the combined stress on V_{th} instability, as depicted in Fig. 1(a). In Case One, the surge-first stress sequence was designed to replicate the application scenario in which a device is required to perform switching operations after experiencing surge current stress. Conversely, to evaluate the impact of long-term bipolar gate switching operations on surge reliability, Case Two employed the reverse stress order. In both cases, V_{th} recovery was monitored after the combined stress.

In the bipolar GSS test, a +18 V/-8 V bipolar square wave at 1 MHz (duty cycle of 50 %, see Fig. 1(b)) was applied to the gate terminal, while the source and drain terminals were shorted to ground.

To more accurately characterize the transient changes in V_{th} during the reliability test, stress-to-measurement delays and V_{th} measurement times should be minimized [7]. Therefore, an ultrafast (≤10 μs) V_{th} measurement technique was employed in our test to accurately monitor variations in V_{th} and stress-to-measurement delays were reduced to 5 μs to minimize the impact of V_{th} recovery.

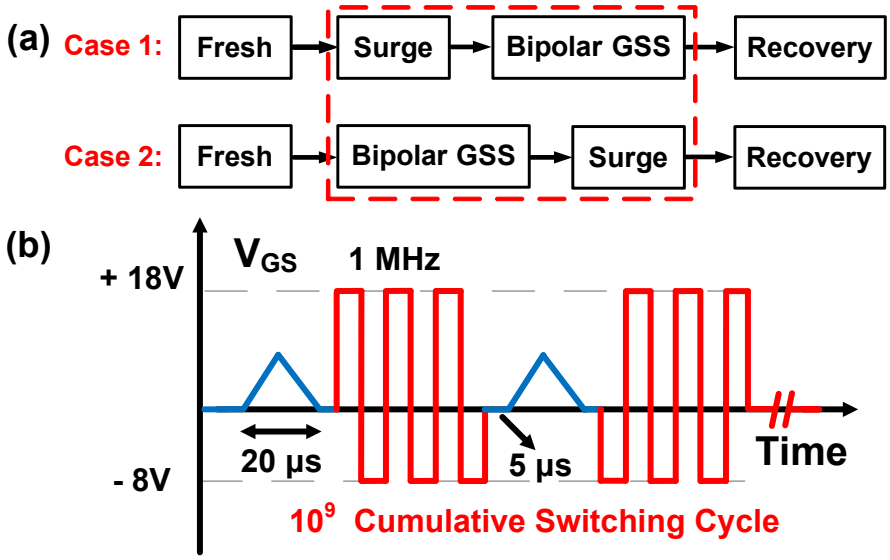

Fig. 1. (a) Two procedures with combined bipolar GSS and surge current stress. (b) Bipolar gate switching and triangular V_{th} measurement waveform for the bipolar GSS test.

A group of 650-V commercially available planar-gate SiC MOSFETs ($R_{DS(on)}$ = 60 mΩ, I_D@25°C = 29 A) was selected as the device under test (DUT). First, a single pulse surge test was performed. A half-sinusoidal surge current, with a duration of 10 ms, was generated by a resonating capacitor and inductor. Figure 2(a) shows the half-sinusoidal waveforms of surge current (I_{SD}) from 30 A to 70 A for the DUT biased at V_{GS} of 0 V. The V_{th} was monitored after each surge current stress, as shown in Fig. 2(b). The V_{th} of the SiC MOSFET is defined as the gate-source voltage when the drain current reaches 10 mA at V_{DS} = 2 V. The V_{th} increased slightly after the initial 30-A surge stress and then remained nearly unchanged for further surge stress before the device failed. At the 70-A surge current stress, the V_{th} shift of the SiC MOSFET was around 0.26 V.

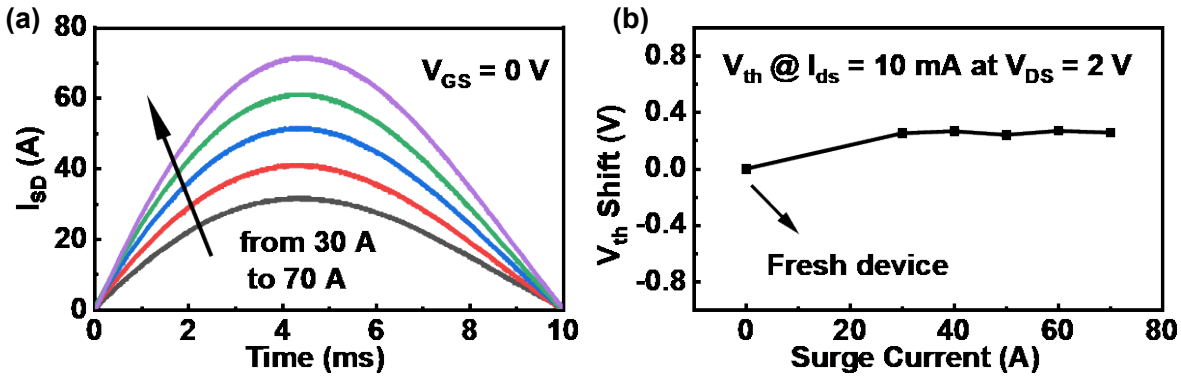

Fig. 2. (a) Surge current waveforms of a 650 V/29 A planar SiC MOSFET under varied surge stress. (b) V_{th} shift after each surge current stress.

Figure 3(a) compares the V_{th} shift as a function of switching cycles during the bipolar GSS test for a fresh device and a device that had undergone a 40-A surge current. Both devices exhibited a positive V_{th} shift of approximately 0.2 V after 10^9-cycle bipolar gate switching. Similar to the V_{th} shift observed in the stress phase, the V_{th} recovery behavior also exhibited little difference between the two devices, as shown in Fig. 3(b). After a 10-minute recovery period, approximately 0.1 V of the

V_{th} shift induced by bipolar gate switching was recovered. These results suggest that the initial surge stress has minimal impact on how V_{th} degrades during the subsequent bipolar GSS phase and recovers afterwards.

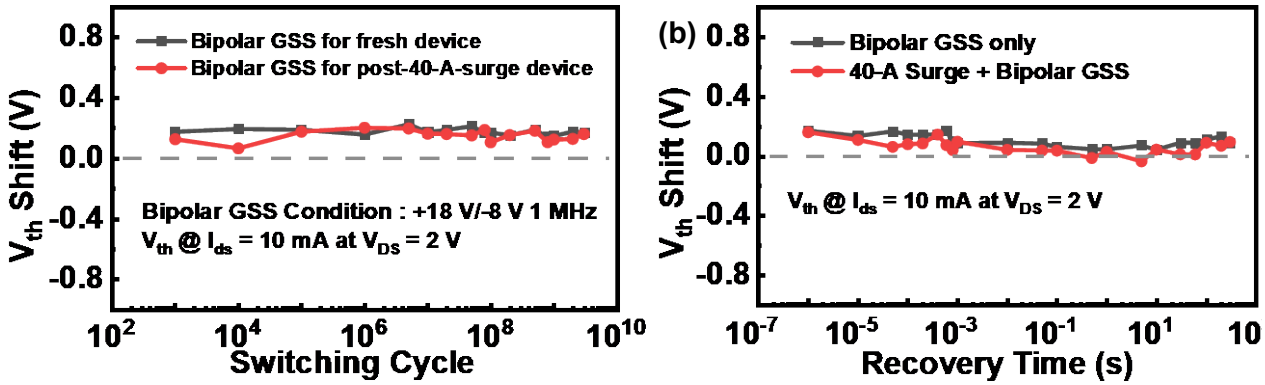

Fig. 3. (a) V_{th} shift during bipolar gate switching stress for fresh and post-40-A-surge-current devices. (b) The V_{th} recovery process for device with bipolar stress only and surge-first device with bipolar GSS.

In contrast, when the device was first stressed with bipolar gate switching for 10^9 cycles and then subjected to a 40-A current surge, the V_{th} shift was ~0.2 V larger than that in the device with surge only or the device with bipolar gate switching only, as compared in Fig. 4. The V_{th} shift induced by surge stress following the bipolar GSS showed minimal recovery in a 10-minute period. These results indicate that the V_{th} shifts induced by combined bipolar GSS and surge stress exhibit a cumulative effect, particularly when the bipolar GSS was applied first.

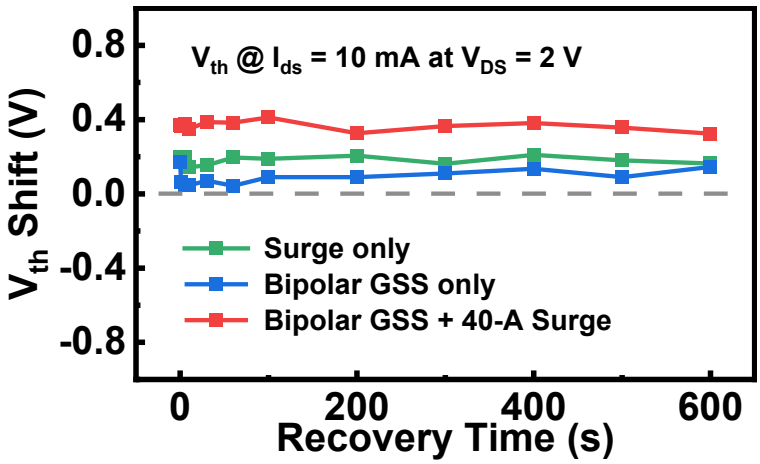

Fig. 4. The V_{th} recovery process for bipolar-stress-first device after surge and other stress conditions.

Discussion

The V_{th} degradation in SiC MOSFETs is mainly due to the presence and charging of trap states at the SiO_2-SiC interface or inside the gate oxide. The distinctive V_{th} shift under the two stress sequences can be explained as follows. In reverse conduction, partial surge current flows through the MOSFET channel at V_{GS} of 0 V during the single surge test, resulting in electron trapping at the SiO_2-SiC interface without generating defects [8], as shown in Fig. 5(a). An increase in net negative charges beneath the gate leads to a positive V_{th} shift. Figure 5(b) illustrates the gate oxide degradation and V_{th} shift mechanisms under bipolar gate switching. Due to the rapidly changing electric field stress in the gate, the bipolar gate switching can generate additional acceptor-like interface defects at the SiO_2-SiC interface [9]. For the case with the bipolar GSS test applied first, the bipolar switching stress acts

as a defect-generation phase, creating additional acceptor-like interface states. Crucially, the subsequent surge stress involves high-density channel carrier injection. This high electron flux efficiently fills these newly generated interface traps. This generation-then-filling process leads to a significantly larger positive V_{th} shift. In contrast, for the surge-first case, trap generation is negligible; hence, the V_{th} degradation induced by the subsequent bipolar stress remains comparable to that of the bipolar-stress-only condition. Therefore, the cumulative degradation mechanism is fundamentally attributed to the coupling between defect generation and charge trapping under combined stress conditions.

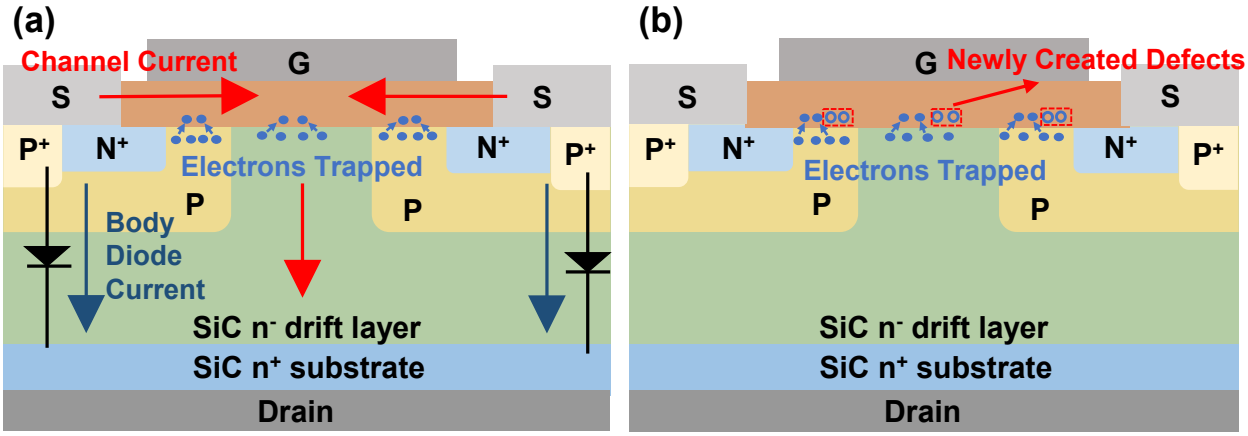

Fig. 5. Schematic of V_{th} shift mechanism of planar SiC MOSFETs under (a) surge current stress and under (b) bipolar gate switching stress.

Summary

The V_{th} shift in planar SiC power MOSFETs under combined stress conditions involving surge current stress and bipolar GSS was experimentally investigated. Applying surge current stress prior to the bipolar GSS test has minimal impact on the GSS-induced degradation and the subsequent recovery behavior. In contrast, the combined stress can induce a cumulative V_{th} shift when the bipolar GSS test is applied before the surge stress. This cumulative effect is attributed to the generation of additional traps at the SiO_2-SiC interface during bipolar gate switching stress. These newly generated traps can capture more electrons under subsequent surge current stress, leading to an additional V_{th} shift. Our work reveals the aggravated cumulative degradation of SiC MOSFETs under complex stress scenarios. It suggests that conventional single-stress assessment methodologies are inadequate to fully capture device reliability issues, necessitating the consideration of combined-stress interactions in practical evaluations. It can also offer circuit designers some valuable guidelines regarding the necessity of monitoring the long-term V_{th} stability of SiC MOSFETs during high-frequency bipolar gate switching (> 10^9 cycles) in practical applications.

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