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Degradation Mechanisms of 1200 V 4H-SiC Planar Power MOSFET under Negative HTGB Stress

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Keywords: SiC MOSFET, high-temperature gate bias (HTGB), reliability, threshold voltage (V_{th}), reverse transfer capacitance (C_{rss}), Fowler–Nordheim tunneling, hole injection.

Abstract. This study investigates the degradation behavior of 1200 V 4H-SiC planar MOSFETs under negative high-temperature gate bias (HTGB) stress. The devices were stressed at −20 V and 150 °C for 1008 hours. Key electrical parameters, including threshold voltage (V_{th}) and reverse transfer capacitance (C_{rss}), were monitored to evaluate time-dependent changes. The results reveal a clear two-phase degradation behavior characterized by a transition between electron-dominated and hole-dominated charge injection mechanisms. In the early stage, electron injection via Fowler–Nordheim (FN) tunneling causes a positive shift in V_{th} and a reduction in C_{rss}. With prolonged stress, partial charge compensation leads to a reversal of the electrical trends. These results demonstrate a time-dependent transition between electron injection and hole injection mechanisms. The findings provide insight into the long-term reliability of planar SiC MOSFETs under negative HTGB stress.

Introduction

SiC MOSFETs enable high-efficiency and high-voltage applications due to their superior breakdown voltage and switching speed [1]. However, interface traps at the SiC/SiO_2 boundary under high-temperature operation remain a key reliability concern [2,3,4].

To evaluate the stability of the gate oxide and interface, high-temperature gate bias (HTGB) testing is widely used [5,6]. Under positive bias conditions, electrons can tunnel from the poly gate into the oxide or interface traps. This causes an increase in V_{th} and a shift in the $C_g - V_{gs}$ curve, similar to the positive bias temperature instability (PBTI) effect observed in silicon MOSFETs [7]. However, SiC devices have lower barrier heights and more complex interface reactions. As a result, electron injection and trap generation are more sensitive and often irreversible, and this condition causes permanent degradation. In actual applications, negative gate bias is more common. When the device operates in switching circuits, applying 0 V during the off-state may lead to false turn-on due to dv/dt or common-mode noise. Applying a negative gate bias (−5 to −20 V) can effectively suppress such noise and improve system stability. Previous studies have shown that negative HTGB may trigger two competing carrier injection mechanisms. One is electron injection from the poly gate, and the other is hole injection from the P-well into the interface or oxide. These two processes may alternate during stress and interact with each other. This interaction causes non-monotonic changes in electrical parameters, such as V_{th} increases in the initial stage and then decreases, while C_{rss} decreases first and then increases. These effects indicate that negative HTGB involves complex dual-carrier behavior.

In addition, oxide traps located above the JFET region have a strong impact on the C–V characteristics [8]. Although the degradation under positive HTGB has been well studied, there is limited data on long-term effects under negative HTGB. Studies often lack full tracking of gate capacitance and dynamic capacitance.

This work focuses on a 1200 V planar SiC MOSFET stressed under $V_{gs} = -20$ V and 150 °C for 1008 hours. The time-dependent behavior of V_{th}, C_{rss}, and C_g–V_{gs} is carefully analyzed. By comparing experimental results with physical models, this study aims to clarify the degradation mechanisms under negative HTGB and provide insights for the long-term reliability of SiC MOSFETs under extreme bias conditions.

Experiment

This study uses a vertically structured 1200 V / 13 A planar SiC MOSFET developed in our laboratory using a conventional SiC MOSFET process [9]. A total of three devices with identical planar MOSFET structures were tested in this study. A cross-sectional view of the device is shown in Fig. 1. The P-well plays a key role in the device operation. It defines the channel behavior and may serve as the source of hole injection under negative HTGB stress. The JFET region controls the current path and the electric field distribution, which are closely related to interface field strength and long-term reliability. The device is packaged in a TO-247 format, making it suitable for high-voltage industrial and automotive power systems. It also offers stable high-temperature operation and good thermal conductivity.

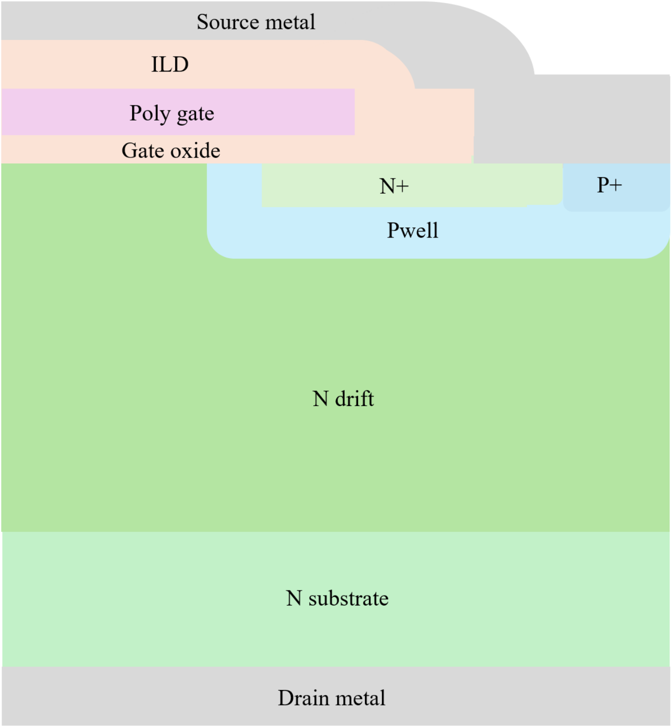


Fig. 1. The cross-sectional diagram of the planar MOSFET.

To simulate the off-state bias condition in real applications, this study conducted a continuous HTGB aging test. The gate bias was set to $V_{gs} = -20$ V, and the devices were placed in a high-temperature chamber at 150 °C under a constant gate voltage. Electrical measurements were performed at room temperature by interrupting the stress at predefined time intervals. Fresh devices were first characterized before stress, and subsequent measurements were carried out after stress durations of 168, 504, and 1008 hours using a Keysight B1505 analyzer. According to AEC-Q101 standards [10], the test was terminated if any key parameter shifted by more than ±20% from its initial value. Three key electrical parameters were monitored, and the full test procedure is illustrated in Fig. 2.

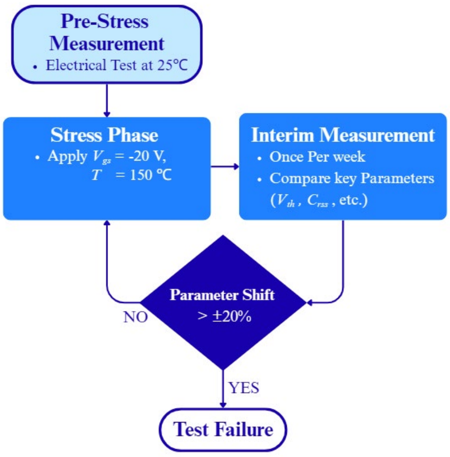


Fig. 2. Flow chart of the HTGB test procedure.

First, the V_{th} was extracted using the constant-current method. The V_{ds} was set to 10 V, and the V_{gs} was swept from 0 V to 20 V. The V_{gs} corresponding to I_{ds} = 10 mA was defined as V_{th}. Second, the C_{rss} was measured to study the depletion behavior between the JFET and drift regions. Third, the C_g was measured by applying a small-signal AC voltage of 25 mV at 1 MHz, sweeping V_{gs} from −15 V to +15 V.

Results and Discussion

A. Influence of HTGB on Threshold Voltage. Under HTGB stress, charge trapping at the SiC/SiO$_2$ interface or inside the gate oxide may cause a shift in threshold voltage (V_{th}) over time. This shift can affect the device's turn-on characteristics and pose a long-term reliability concern if the degradation accumulates. Therefore, this study focuses on analyzing the V_{th} shift behavior under negative HTGB conditions. The I_{ds}–V_{gs} transfer curves of the MOSFET are shown in Fig. 3. After 1008 hours of HTGB stress, the device still maintains good turn-on capability. However, near the steepest region of the curve (around V_{gs} = 11.5 V), a gradual shift is observed at each measurement point, indicating a time-dependent change in threshold behavior. To further evaluate device-to-device variation, Fig. 4 summarizes the distribution of V_{th} extracted from three structurally identical planar MOSFETs at different HTGB stress durations. The results show a clear time-dependent evolution of V_{th}, confirming that the observed shift is a consistent degradation trend rather than measurement fluctuation.

Fig. 5 shows the time-dependent trend of V_{th} variation extracted from the same device at different HTGB stress durations. The threshold voltage can be theoretically expressed by Eq. (1) [11]:

$$V_{th} = V_{th0} - \frac{Q_{ot}}{C_{ox}} - \frac{Q_{it}}{C_{ox}}. \tag{1}$$

Here, Q_{ot} represents the oxide trap charge, Q_{it} denotes the interface trap charge, and C_{ox} is the gate oxide capacitance. The theoretical threshold voltage V_{th0} can be further expressed by Eq. (2):

$$V_{th0} = \sqrt{\frac{4\varepsilon_S kTN_A \ln(\frac{N_A}{n_i})}{C_{ox}}} + \frac{2kT}{q}\ln(\frac{N_A}{n_i}). \tag{2}$$

In Eq. (2), ε_S is the dielectric constant of SiC, k is the Boltzmann constant, T is the absolute temperature, N_A is the doping concentration in the P-well region, and n_i is the intrinsic carrier concentration of SiC.

This study divides the V_{th} behavior into two phases. In Phase 1 (0–504 hours), V_{th} increased by approximately 2.17%. This is attributed to electrons tunneling from the poly gate into the oxide through the FN mechanism and being trapped at the interface, forming negative charges [6]. According to Eq. (1), these trapped negative charges in the oxide raise V_{th}. In Phase 2 (504–1008 hours), V_{th} decreased by about 1.16%. This is likely due to holes injected from the P-well being trapped at the interface, resulting in positive charge accumulation. Based on Eq. (1), the presence of positive oxide trap charges leads to a reduction in V_{th}. This behavior is consistent with the dual-charge-trapping model proposed by Shen et al. [7].

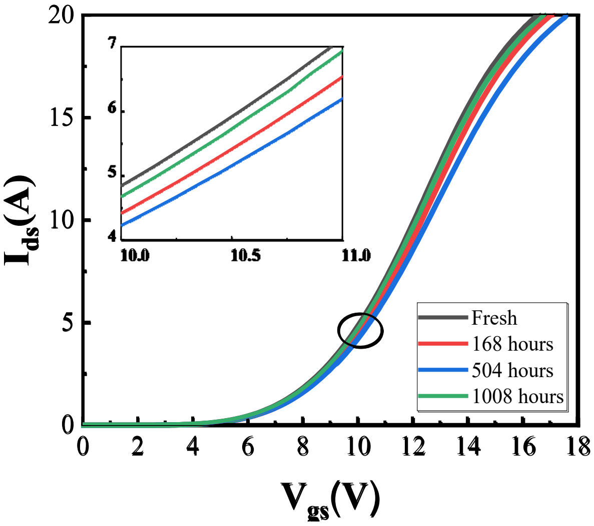


Fig. 3. Measured $I_{ds}-V_{gs}$ curves of MOSFET.

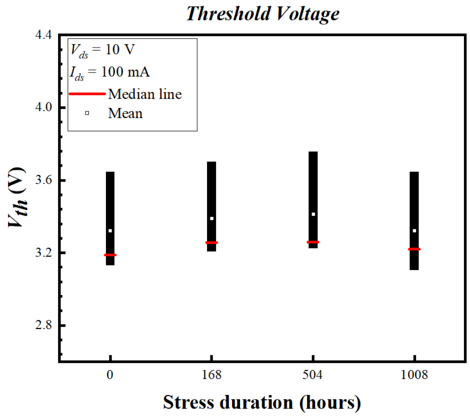


Fig. 4. Distribution of V_{th} measured from multiple devices under negative HTGB stress.

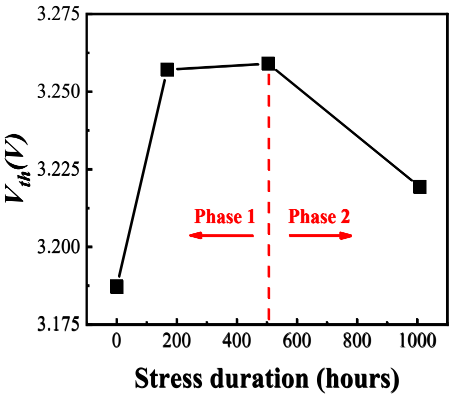


Fig. 5. Variations of V_{th} of the MOSFET under HTGB stress.

B. Influence of HTGB on $C_{rss}-V_{ds}$. C_{rss} is the capacitance between the gate and drain. It reflects the depletion behavior in the JFET and drift regions, both of which are crucial for determining the device's dynamic switching characteristics. C_{rss} affects the dV/dt rate during switching events. It is a key parameter for evaluating switching losses and device reliability. In the planar structure used in this study, C_{rss} is particularly affected by trap distribution in the oxide above the JFET region. Fig. 6 shows the $C_{rss}-V_{ds}$ curves at different stress durations. To further evaluate device-to-device variation, Fig. 7 summarizes the distribution of C_{rss} measured from multiple devices under negative HTGB stress, confirming that the observed trend is not dominated by sample-to-sample fluctuation. Fig. 8 presents the extracted C_{rss} values at V_{ds} = 1000 V for each time point. The results show a clear two-phase degradation change during the 1008-hour negative HTGB stress. In Phase 1 (0–504 hours), C_{rss} dropped by approximately 13.69%. This drop is likely caused by electrons tunneling from the poly gate and being trapped in the oxide, which expands the depletion region and suppresses the capacitive coupling. In Phase 2 (504–1008 hours), C_{rss} shows a gradual increase of about 6.71%, compared to the value at 504 hours. This rise is attributed to hole injection from the P-well into the oxide or interface. These holes partially neutralize the previously accumulated negative charge, resulting in a narrowed depletion region and hence an increase in capacitance.

This observed two-phase behavior of C_{rss} strongly supports the dual carrier injection mechanism proposed in Shen's model, where the dominant charge species changes over time. It also highlights the time-dependent and spatially dynamic nature of oxide trap evolution under long-term stress conditions.

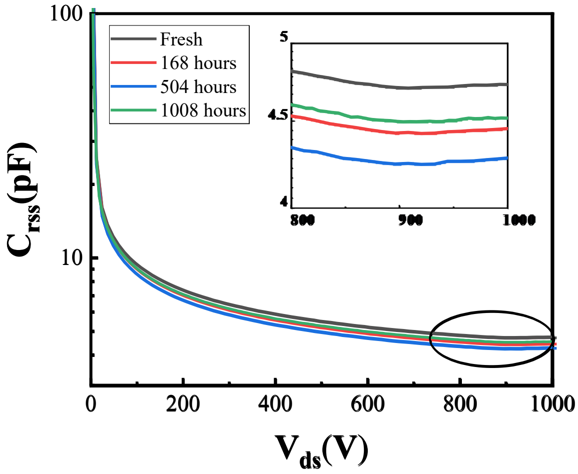
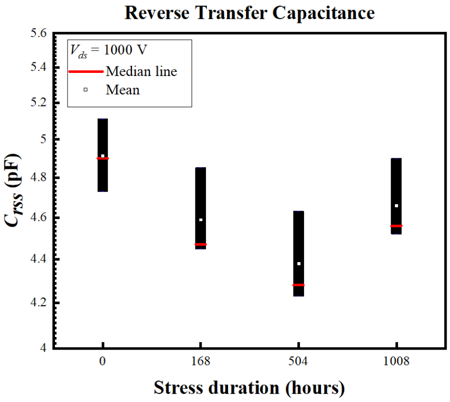


Fig. 6. Measured $C_{rss}-V_{ds}$ curves of MOSFET.



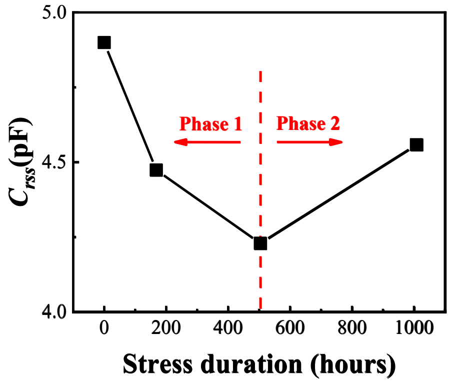


Fig. 7. Distribution of C_{rss} measured from multiple devices under negative HTGB stress.

Fig. 8. Variations of C_{rss} of the MOSFET under HTGB stress.

C. Influence of HTGB on C_g–V_{gs}. To further investigate the degradation mechanism of SiC MOSFETs under negative HTGB stress, this study compares the C_g–V_{gs} curves at 0 and 1008 hours, as shown in Fig. 7. In the range of $V_{gs} = -9$ to -6 V, defined as Region 1, the device is not fully turned on but the channel begins to modulate. After 1008 hours of stress, the C_g–V_{gs} curve in Region 1 shows a clear positive shift, and the slope increases significantly. This behavior suggests that a significant number of electrons are trapped in the oxide above the JFET region, increasing the local trap charge density.

Such localized trapping behavior reveals that the degradation is not uniformly distributed across the oxide but is highly dependent on the device's internal electric field profile and structure. The observation supports the spatial selectivity of trap formation, especially near high-field regions like the JFET. This finding is consistent with the time-dependent variations of V_{th} and C_{rss}, confirming the physical linkage between capacitance shifts and trap evolution. Overall, the positive shift in C_g–V_{gs} provides further evidence of position-dependent reliability degradation in SiC power devices under long-term negative bias stress.

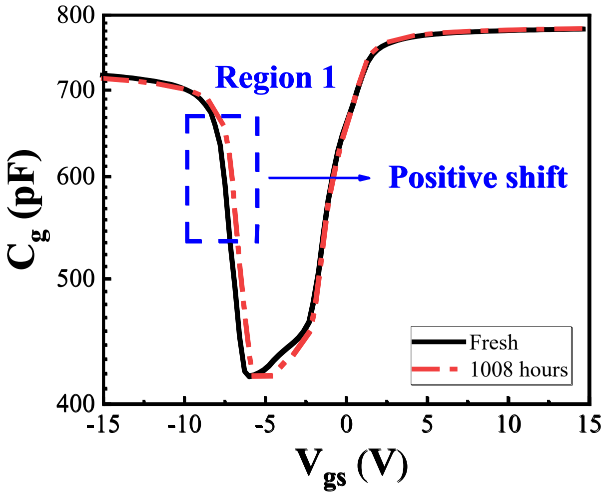


Fig. 9. Measured C_g–V_{gs} of MOSFET.

Conclusion

This study investigates the long-term degradation of 1200 V planar SiC MOSFETs under negative HTGB stress conditions. Electrical parameters including V_{th}, C_{rss}, and C_g–V_{gs} were monitored and analyzed over time. In Phase 1, V_{th} increased by 2.17% due to electron injection from the poly gate via FN tunneling. In Phase 2, V_{th} decreased by 1.16%, attributed to hole injection from the P-well and partial charge compensation. C_{rss} also showed a two-phase behavior. It dropped by 13.69% in Phase 1, suggesting expansion of the depletion region due to electron trapping above the JFET region. In Phase 2, C_{rss} increased by 6.71%, which implies that holes neutralized the trapped charges and caused the depletion region to shrink. Additionally, the C_g–V_{gs} curve showed a clear positive shift in Region 1, suggesting local trap formation above the JFET region and increased effective capacitance.

These findings confirm that negative HTGB triggers competing carrier injection behaviors and non-uniform trap distribution. The results offer insight into degradation physics and provide guidance for improved reliability modeling and bias design in SiC power devices. Furthermore, the spatial selectivity of trap generation highlights the importance of electric field engineering in device layout. Future work can focus on optimizing oxide quality and structural design to suppress localized stress effects. These insights contribute to extending the lifetime and ensuring robust operation of SiC MOSFETs in high-temperature, high-reliability applications.

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