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Understanding the Influence of Different Parameters on the Dynamic V_{SD} Behaviour of SiC MOSFETs during Power Cycling Test

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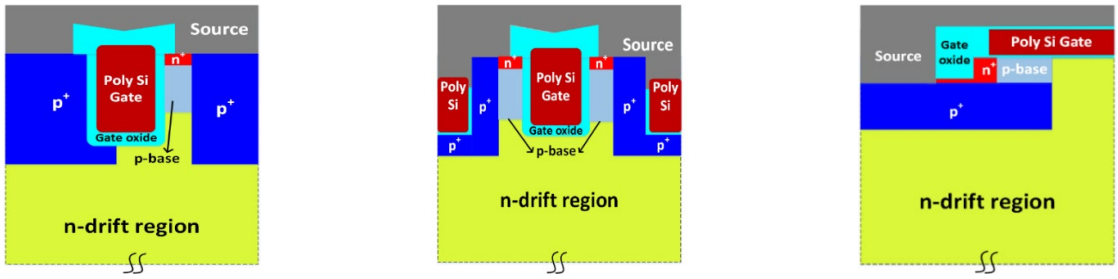
Abstract. An accurate junction temperature estimation is crucial for all reliability tests (e.g., power cycling tests) of power semiconductor devices, as it directly impacts the lifetime estimation. Studies on advanced silicon carbide (SiC) MOSFETs from various manufacturers indicate that conventional static temperature calibration methods can introduce significant error in virtual junction temperature determination due to the dynamic behaviour of the body diode's voltage drop (V_{SD}). In this study, a similar dynamic V_{SD} behaviour was observed by switching the gate voltage without applying a load current, using only a sense current across the body diode. However, this time-dependent dynamic V_{SD} behaviour can be completely eliminated by applying sufficiently negative voltage. Furthermore, dynamic V_{SD} behaviour is strongly influenced by different parameters such as gate loop inductance, gate resistance, turn-on gate voltage, junction temperature and sense current. Moreover, complementary 2D TCAD simulations under experimental conditions reveal that charge trapping and de-trapping at the SiC/SiO_2 interface, together with current sharing between the channel and body diode, fundamentally govern the observed transient V_{SD} dynamics. These findings provide critical insights for an accurate temperature determination and characterization of SiC MOSFETs under dynamic gate conditions.

Introduction

The ECPE Guideline AQG 324 standardized procedures and methodologies for the lifetime characterization of power electronic converters for automotive applications [1]. These procedures include thermal impedance measurement (Z_{th}) and active power cycling tests (PCT). During PCT, the virtual junction temperature (T_{vj}) of the device under test (DUT) is estimated using temperature-sensitive electrical parameters (TSEP). For SiC MOSFETs, the temperature-dependent built-in voltage drop across the intrinsic body diode (V_{SD}) is employed to determine T_{vj} by applying a sense current (I_{sense}) [1, 2]. However, this method faces several challenges - specifically, when the MOSFET channel is still partially-on at certain negative gate-source voltage. In general, a more pronounced body effect for SiC MOSFETs intensifies this effect. However, it can be mitigated by applying a sufficiently negative gate voltage [3]. Although in some cases, this mitigation value exceeds the lower limit of the gate voltage specified in the datasheet. Additionally, interface traps at the SiC/SiO2 interface can influence the transient V_{SD} behaviour [4]. Experimental measurements have shown that the V_{SD} transient often exhibits a slow decay lasting up to seconds before reaching steady-state voltage values, especially in the absence of load current [5]. However, this anomalous V_{SD} behaviour remains unexplained in the existing literature. In this work, a pulse pattern similar to the PCT cool-down measurement routine was applied by switching the gate source voltage (V_{GS}) without applying a load current (I_{load}). The time-dependent dynamic behaviour of the body diode's forward voltage drop (V_{SD}), was investigated by using only a small I_{sense} (like the sense current in a PCT) in the range of milliampere.

In this study, the influence of various parameters such as negative gate-source voltage ($V_{GS,off}$), gate inductance (L_g) and gate resistance ($R_{G,off}$) on dynamic V_{SD} behaviour is systematically analyzed. Additionally, 2D electro-thermal TCAD simulations were performed under measured conditions to gain deeper understanding of the device's internal behaviour, with specific focus on the impact of SiC/SiO_2 interface traps.

Device Under Test and Experimental Setup



(a) M1 (b) M2 (c) M3

Fig. 1. Schematic cross-section of the cell head of SiC MOSFETs from different manufacturers.

The Devices Under Test (DUTs) were commercially available 1.2 kV SiC MOSFET from three different manufacturers (denoted as M1, M2, and M3) with similar current ratings. Despite their similar current ratings, the three SiC MOSFETs have different cell technologies, as illustrated in Fig. 1. The corresponding device parameters are summarized in Table. 1. The measured input capacitance (C_{iss}) and reverse capacitance (C_{rss}) are plotted as a function of voltage for different manufacturers in Fig. 2. M1 device show the lowest C_{iss} along with smallest internal gate resistance as compared to other manufacturers. The planar-gate technology M3 have the lowest C_{rss} compared to the other trench-gate technologies, see Table 1. These capacitance characteristics are important for interpreting the dynamic V_{SD} behaviour for different gate technologies.

Table 1. Device parameters of the SiC MOSFETs from different manufacturers.

Device parameters	**M1**	**M2**	**M3**
Gate technology	Trench	Double trench	Planar
Rated current	31 A	31 A	32 A
$R_{ds,on}$	80 mΩ		
Recommended $V_{GS,on}$	18 V	18 V	15 V
Maximum allowed $V_{GS,off}$	-10 V	-4 V	-8 V
Internal gate resistance ($R_{G,int}$)	**2 Ω**	**12 Ω**	**9 Ω**
C_{iss} at 15 V	840 pF	912 pF	1545 pF
C_{rss} at 15 V	15 pF	140 pF	7 pF
Package type	TO-247-4		

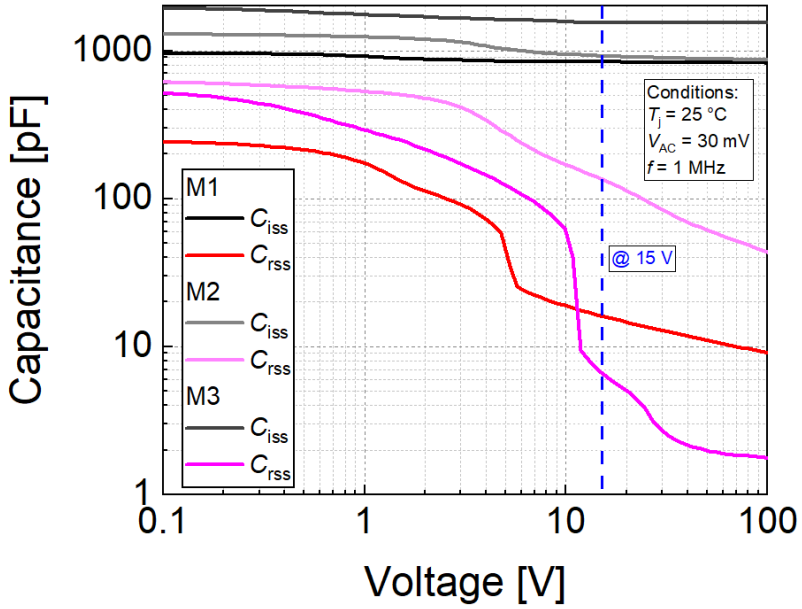
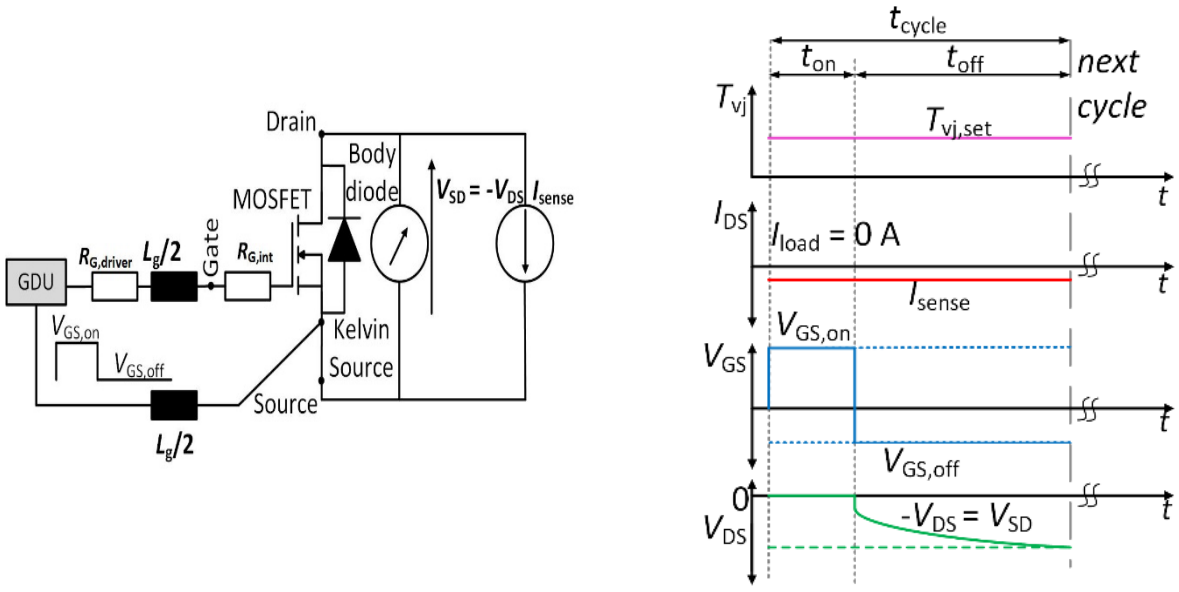


Fig. 2. Comparison of the input and reverse capacitance as a function of voltage for three different manufacturers.

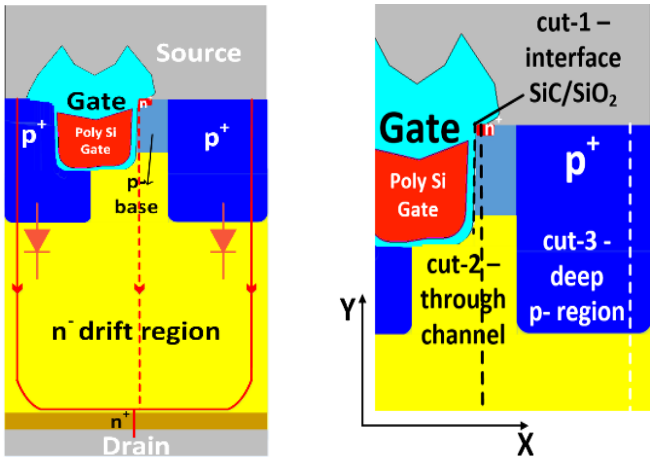


(a) (b)

Fig. 3. (a) Schematic diagram of the measurement circuit used for dynamic V_{SD} behaviour. (b) Pulse pattern.

The experimental setup used to measure the dynamic V_{SD} behaviour of a SiC MOSFET is schematically illustrated in Fig. 3(a). A similar circuit can be employed for T_{vj} (V_{SD}) calibration as well as Z_{th} and PCT measurements. Generally, the maximum and minimum junction temperatures are extrapolated during off-time of each cycle. In the absence of a load current, V_{SD}, which corresponds to T_{vj}, is expected to remain constant throughout the off-time (t_{off}) and during the transition from on-time (t_{on}), as no temperature and current variation occurs when I_{load} = 0 A and only the sense current of 100 mA is flowing constantly. However, by merely switching the gate voltage from positive to negative values, a dynamic V_{SD} behaviour is observed, as shown in Fig. 3(b). A similar observation has been reported in [5]. All V_{GS} and V_{DS} values were measured using a Kelvin source connection without the influence of load-source inductance for SiC MOSFETs.

TCAD Simulation Model



(a) (b)

Fig. 4. (a) Simplified structure of the M1 trench-gate SiC MOSFET. (b) Different cut through the zoomed-in structure.

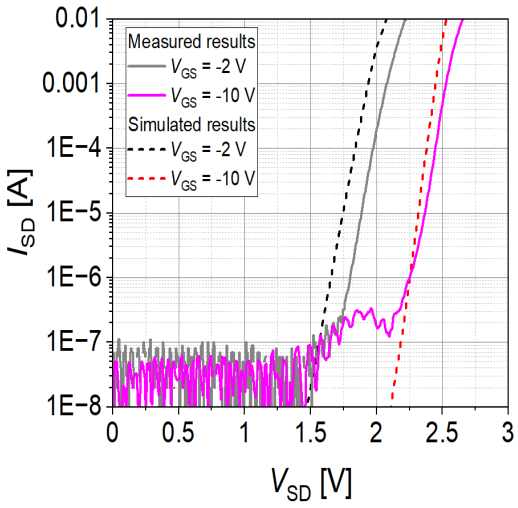


Fig. 5. Comparison of the simulated and measured I-V characteristic of the body diode.

Table 2. SiC/SiO_2 interface trap values used in the simulation model.

Trap types	**Energy [eV]**	**Density (D_{it}) [cm^{-2} eV^{-1}]**	**Reference**
Shallow acceptors	E_C - 0.14	$1x10^{12}$	[6, 7]
Shallow donors	E_V + 0.20	$1x10^{12}$	[8, 9]
Mid-gap donors	E_C - 0.70	$4x10^{11}$	[8, 10]

In this framework, the pn-junction voltage serves as the TSEP, while a parallel current in the channel may influence the dynamic V_{SD} behaviour and correspondingly the estimated junction temperature. To analyze the influence of the traps and channel dynamics on transient V_{SD} behaviour, a trench-gate half-cell 1.2 kV SiC MOSFET structure from M1 was designed and modeled using Synopsys TCAD tool [11], as shown in Fig. 4. Electro-thermal simulations were performed to investigate the dynamic V_{SD} characteristic of the body diode.

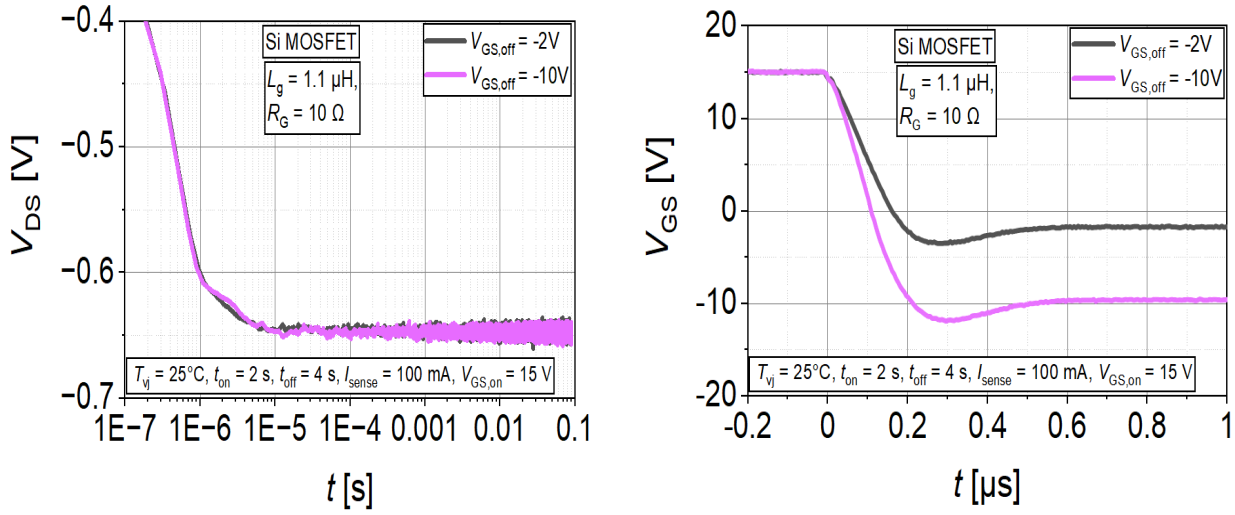
The SiC/SiO_2 interface hosts a variety of potential traps [8]. In the simulations, traps were localized at the SiC/SiO_2 interface. Shallow and deep trap levels were implemented in this work according to the literature (see, Table 2). Further, the simulated I-V characteristic of the body diode are compared with measurements for channel-on (-2 V) and channel-off (-10 V) conditions, as shown in Fig. 5. The simulated results show a slightly lower voltage drop but are in good agreement with measured results.

Additionally, a sense current of 1 µA was used for the half-cell simulation model instead of 100 mA. The sense current applied for the simulation model was scaled down according to the area factor of the real device.

Dynamic V_{SD} Measurement Results and Analysis

In the following, the focus is on the V_{SD} dynamic effects caused by the undershoot and overshoot in the gate voltage transients. These V_{GS} oscillation occurs at the turn-off of the gate voltage and typically persist for less than some hundreds of nanoseconds. The conventional real-time recording systems of the PCT are generally unable to resolve the V_{GS} oscillations due to their limited sampling rate. Therefore, an oscilloscope based measurement setup was employed to capture transient events and reveal their effect.

Si MOSFET Results



(a) V_{DS} (b) V_{GS}

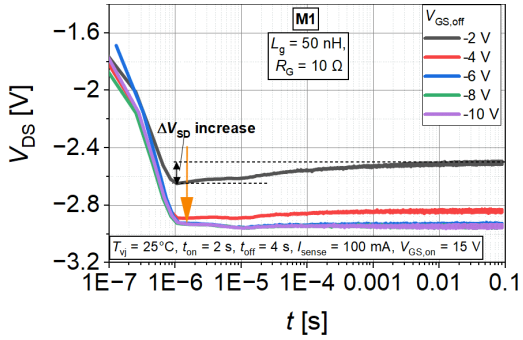
Fig. 6. Measured V_{SD} behaviour and corresponding V_{GS} of the Si MOSFET with gate loop inductance of 1.1 µH for different $V_{GS,off}$ values at a given conditions. Note: the time scaling for the V_{DS} is logarithmic, and for the V_{GS} is linear.

As an initial calibration step, the measurement setup was validated using a silicon MOSFET (IPP65R099C6) with an I_{sense} = 100 mA. The gate voltage was switched from +15 V to -2 V and -10 V. The measured V_{DS} remained unchanged after 10 µs irrespective of the applied negative gate voltage, with a steady voltage drop of 0.65 V, see Fig. 6(a). The corresponding gate voltage transients show small undershoot even with a L_g of 1.1 µH due to high C_{iss} of the device. The used L_g of 1.1 µH is an exemplary value at a PCT bench with a wired gate connection. The measured V_{SD} characteristics align well with the expected behaviour of this Si MOSFET, thereby validating that the measurement setup is reliable and introduces no significant artifacts into the experimental data.

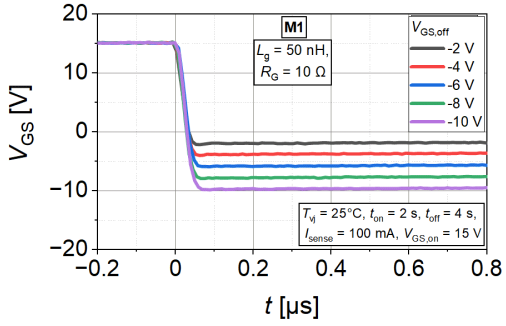
SiC MOSFET Results

During temperature determination using $V_{SD}(T_{vj})$ method, several factors may influence the measured V_{SD}. The impact of these parameters is analyzed in the following sections through a combination of measurements and TCAD simulations.

Influence of $V_{GS,off}$ at different L_g and $R_{G,off}$

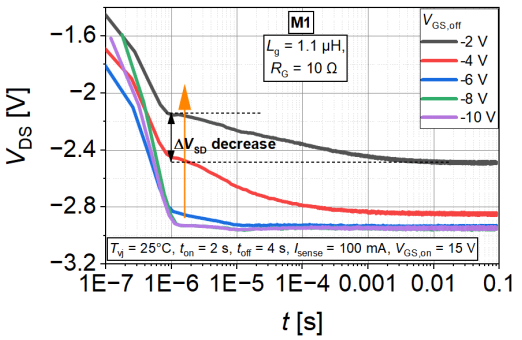


(a) V_{DS}

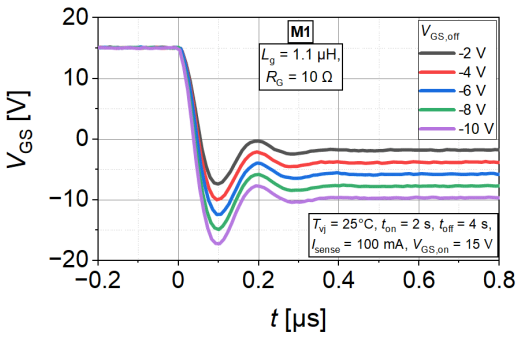


(b) V_{GS}

Fig. 7. Measured dynamic V_{SD} behaviour of the trench-gate M1 device with gate loop inductance of 50 nH for different $V_{GS,off}$ values. Note: the time scaling for the V_{DS} is logarithmic, and for the V_{GS} is linear.



(a) V_{DS}



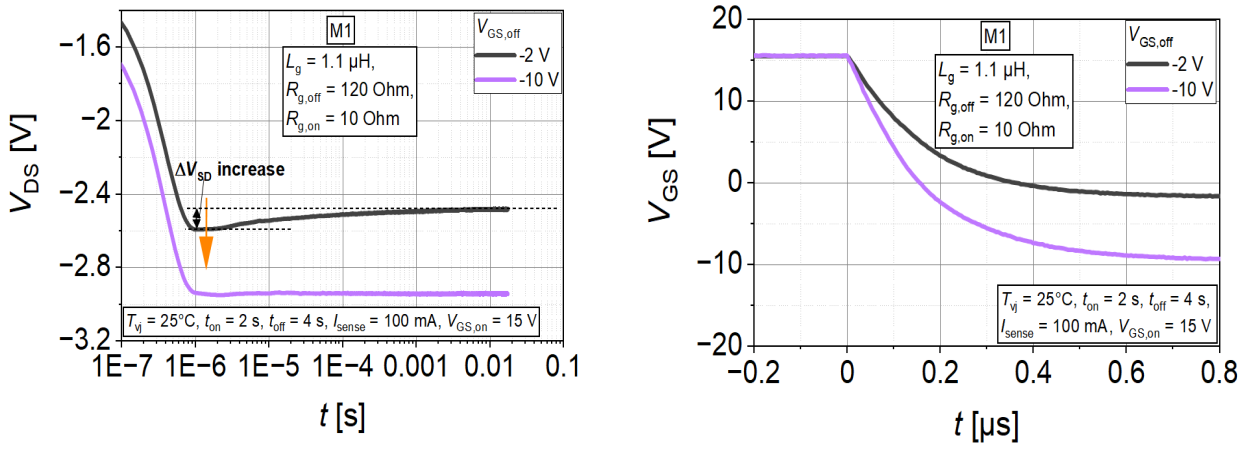
(b) V_{GS}

Fig. 8. Measured dynamic V_{SD} behaviour of the trench-gate M1 device with gate loop inductance of 1.1 µH for different $V_{GS,off}$ values. Note: the time scaling for the V_{DS} is logarithmic, and for the V_{GS} is linear.

For a low gate inductance of 50 nH, the dynamic V_{SD} behaviour for different $V_{GS,off}$ is displayed in Fig. 7, along with corresponding gate signal measured using an oscilloscope to detect the faster signal transients. At $V_{GS,off}$ values of -2 V and -4 V, the dynamic V_{SD} effect is clearly visible after gate turn-off. This initial transient ΔV_{SD} is attributed to electron trapping during the on-state of the gate voltage ($V_{GS,on}$) at SiC/SiO_2 interface states, and this results in elevated third quadrant voltage drop (V_{SD}) due to still increased threshold voltage (V_{th}) [4]. Especially, at -2 V condition (MOS depletion) holes for quick neutralization are missing. During the subsequent off-time t_{off} (similar to the relaxation phase), electrons are emitted over time and the V_{SD} gradually stabilizes, with the final steady-state value being dependent on both the applied $V_{GS,off}$ and the impact of the body effect. Notably, for L_g of 50 nH, no transient gate voltage over- or undershoot was observed during V_{GS} turn-off, [see Fig. 7(b)]. For e.g. the -10 V condition, enough holes (MOS accumulation) are quickly neutralizing the before trapped electrons from on-state and lead to a very quick stabilization of the V_{SD}. Also, the body effect does not play a role at this low $V_{GS,off}$ [12].

It is important to note that in larger PCT systems, the gate inductance loop can be much higher due to the use of longer gate-source connections as there is no need of high frequency switching in these test systems. To replicate such conditions, measurements were carried out with a gate loop inductance of 1.1 µH as shown in Fig. 8. The small gate resistance (10 Ω) in combination with the higher L_g leads to some oscillations in the V_{GS} transients at turn-off which are very important for the subsequent V_{SD} behaviour. The over- and undershoots persist for less than 200 ns, see Fig. 8(b). The V_{GS} oscillations closely define the dynamic V_{th} and consequently influence the V_{SD} response, as depicted in Fig. 8(a). A more negative V_{GS} undershoot occurring shortly after turn-off dynamically lowers the effective V_{th} due to enhanced hole trapping at the SiC/SiO_2 interface which is neutralizing

captured electrons from the V_{GS} on-state quickly. This results in a slightly more and longer opened channel (similar to the V_{th} hysteresis effect). As a result, the current sharing between the channel and body diode is altered [see Fig. 8(a)]. For $V_{GS,off}$ values of -2 V, -4 V and -6 V, the dynamic V_{SD} initially decreases at 1 µs, followed by an exponential decay towards its steady-state value. This observed dynamic V_{SD} behaviour is in contrast when compared to the low gate inductance loop but it seems to be more realistic focusing on real PCT-benches. In the next section, TCAD simulation results will be used to explain this observed phenomenon.

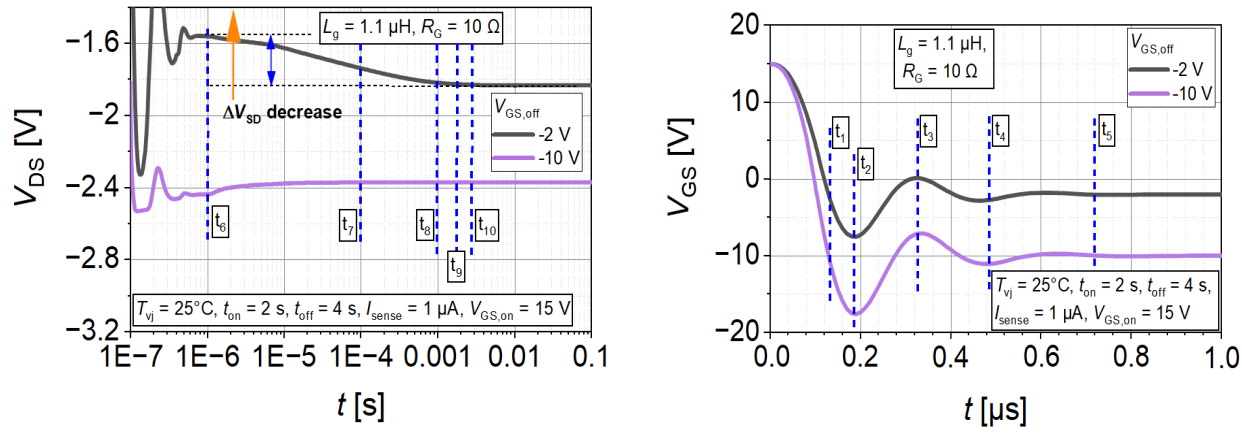


(a) V_{DS} (b) V_{GS}

Fig. 9. Measured Dynamic V_{SD} behaviour of the trench-gate SiC MOSFET at of $R_{G,off}$ = 120 Ω and for different $V_{GS,off}$ values. Note: the time scaling for the V_{DS} is logarithmic, and for the V_{GS} is linear.

The oscillations in the gate voltage due to high L_g can be mitigated by increasing the turn-off gate resistance ($R_{G.off}$) as demonstrated in Fig. 9. The measured dynamic V_{SD} behaviour is similar to conditions shown in Fig. 7. However, it could be summarized that at sufficiently negative V_{GS}, the V_{SD} becomes stable very shortly after V_{GS} turn-off and should lead to a stable T_{vj} readout – at least for the measured trench technology.

TCAD simulation results at L_g = 1.1 µH



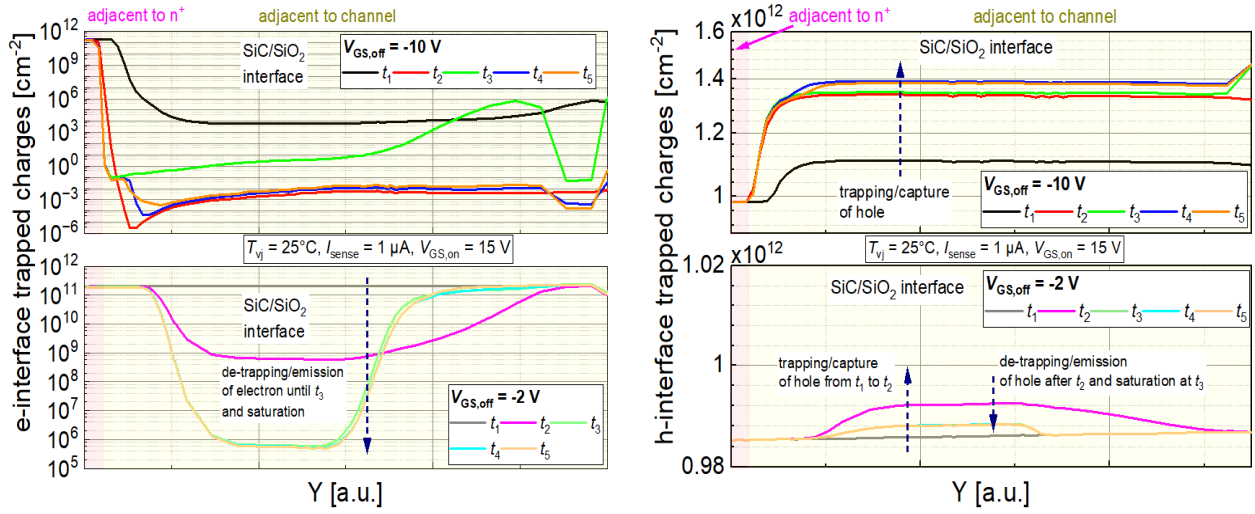
(a) V_{DS} (b) V_{GS}

Fig. 10. Simulated dynamic V_{SD} behaviour of the trench-gate M1 device with gate loop inductance of 1.1 µH for different $V_{GS,off}$ values at a given conditions. Note: the time scaling for the V_{DS} is logarithmic, and for the V_{GS} is linear.

Fig. 10 presents the simulated dynamic V_{SD} behaviour at L_g of 1.1 µH. The simulated results exhibit a good agreement with corresponding measurements shown in Fig. 8. For V_{GS} of -2 V, the V_{SD}

waveform demonstrates an exponential decay in the interval from 1 µs to 10 ms, followed by a steady-state value. A slight transient in V_{SD} is observed up to 10 µs for V_{GS} of -10 V. This transient behaviour can be mainly attributed to oscillations in the gate voltage. To clarify the underlying mechanisms and role of SiC/SiO_2 interface traps, the simulation results are analyzed in two stages.

In the first stage, the effect of the gate voltage transients is examined using five different time points from t_1 to t_5, corresponding to undershoot and overshoot occurring within the interval of 100 ns to 1 µs [see, Fig. 10(b)].

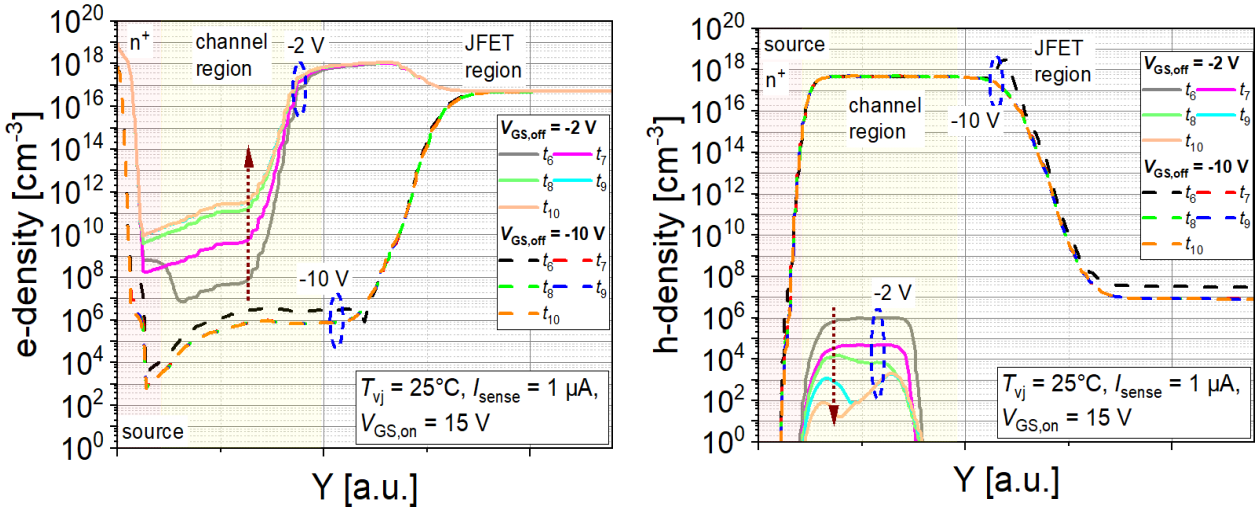


(a) (b)

Fig. 11. Simulated (a) e-interface (b) h-interface trapped charges at the SiC/SiO_2 interface at different time points (t_1 to t_5) in V_{GS} oscillation with L_g = 1.1 µH. For time points, see Fig. 10(b). cut-1 at interface. For -2 V case, electrons are quickly neutralized between t_2 and t_3.

The electron and hole interface trapped charges at SiC/SiO_2 are plotted in Fig. 11 for two values of $V_{GS,off}$. At t_2, corresponding to gate maximum undershoot, the strong negative bias enhances hole accumulation at the interface, promoting electron de-trapping and neutralization. The subsequent overshoot at t_3, which lasts only a few nanoseconds, has negligible influence on electron and hole de-trapping process at $V_{GS,off}$ of -2 V. For $V_{GS,off}$ of -10 V condition and at t_2, a very low amount of electrons is present at the interface since they are very quickly neutralized by the accumulated holes. As gate voltage stabilizes at t_4 and t_5, fast electron de-trapping and hole emission approaches saturation, which determines the initial V_{SD} value at 1 µs, but especially in the case of -2 V condition the amount of trapped electron at the interface is still much higher compared to -10 V condition. In the second stage, the dynamic V_{SD} behaviour beyond 1 µs is analyzed at time points t_6 to t_{10}, as illustrated in Fig. 10(a).

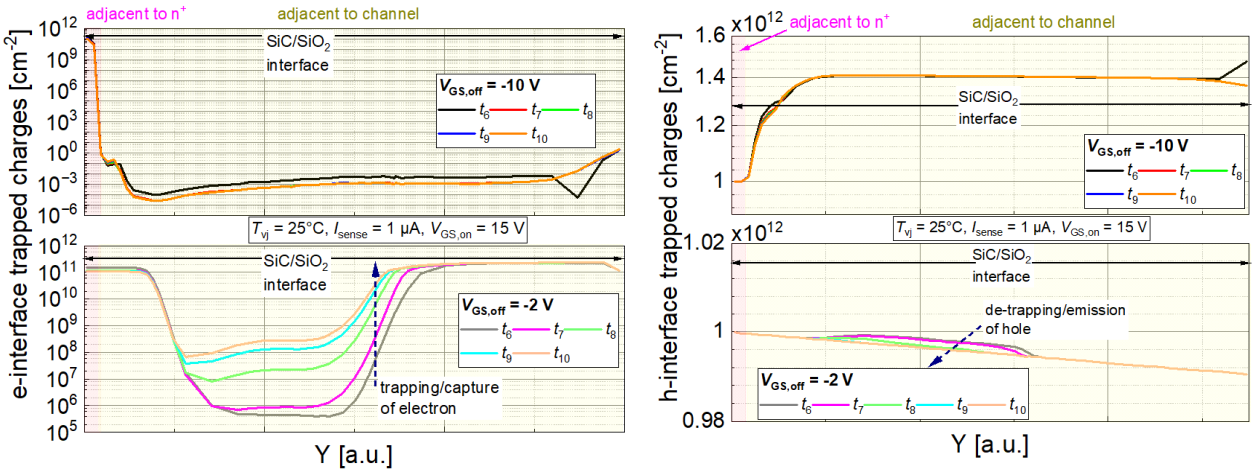
The simulated electron and hole density profile across the channel (cut-2) at different time points (t_6 to t_{10}) extracted from dynamic V_{SD} behaviour are shown in Fig. 12. For wide bandgap semiconductors devices like SiC MOSFETs, the electric field induced by the moderate negative gate bias (e.g. -2 V) is insufficient to fully deplete the channel due to the pronounced body effect. As a result, the electron density in the channel region remains significantly higher as compared to that at $V_{GS,off}$ of -10 V [Fig. 12(a)]. The weakened inversion channel at -2 V leads to parallel current flow between the channel and the intrinsic body diode of the SiC MOSFETs. The electron density continues to increases up to t_8, after which it saturates during V_{SD} steady state. However, under a strong negative voltage (-10 V), the channel is completely pinched-off and the conduction occurs exclusively through body diode. In this condition, the measured voltage drop remains constant after 10 µs, and the carrier density distribution shows negligible variation across different time points. Furthermore, the strong negative bias of the gate electrode attracts a high density of holes, see Fig. 12(b).



(a) e-density (b) h-density

Fig. 12. Simulated charge carrier densities through channel (cut-2) for different time points (t_6 to t_{10}) for the given simulation conditions with L_g = 1.1 µH. For time points see Fig. 9(a).

In SiC MOSFETs, the oxide layer can exhibit a higher density of interface traps (defects or localized charge sites) compared to Si based power devices [12]. The trapping and de-trapping mechanism, along with the partially-on channel conditions due to body effect for certain negative gate voltages, can modulate the V_{SD} transients. To investigate this dynamic behaviour, five different time points (t_6 to t_{10}) were analyzed for $V_{GS,off}$ values of -2 V and -10 V [see, Fig. 10(a)].

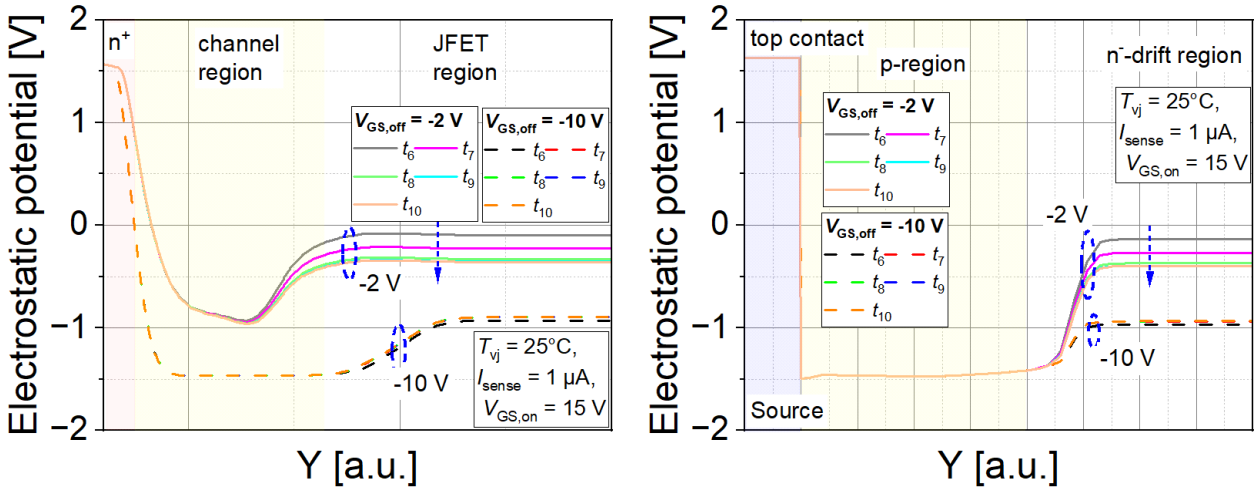


(a) (b)

Fig. 13. Simulated (a) e-interface (b) h-interface trapped charges at the SiC/SiO$_2$ interface for two different $V_{GS,off}$ values at different time points (t_6 to t_{10}) with L_g = 1.1 µH. For time points, see Fig. 10(a). cut-1 at interface.

Fig. 13 displays the electron and hole trapped charges at SiC/SiO$_2$ interface during dynamic V_{SD} transients. For $V_{GS,off}$ of -10 V, the strong negative bias fully depletes the channel, results in negligible change in either electron or hole trapping dynamics. These values remain constant over time after t_7. In contrast, for $V_{GS,off}$ value of -2 V, the electron occupancy of deeper levels increases progressively before saturating after a few milliseconds, which means the V_{th} is increasing again and the absolute value of V_{SD} is increasing. This phenomenon is attributed to the weak channel inversion taking the body effect into account (close to depletion) under moderate $V_{GS,off}$ value, which enhances local electron-density near the interface. The electrons are available from reverse current (I_{sense}) flow through the partially open channel. Meanwhile, the slow emission of holes locally affects the electrostatic potential, thereby dynamically modulating the current sharing between the channel and

pn-junction of the body diode via V_{th} change. Fig. 14 illustrates the simulated electrostatic potential distribution across channel and deep p-region. The slower trapping mechanism of deeper trap levels relative to the conduction band influences the electrostatic potential distribution profile, particularly under partially-on channel conditions, thereby contributing to the observed transient V_{SD} behaviour. For -2 V case, it can be clearly seen that with longer times after V_{GS} turn-off, the voltage drop across the body diode gradually rises.

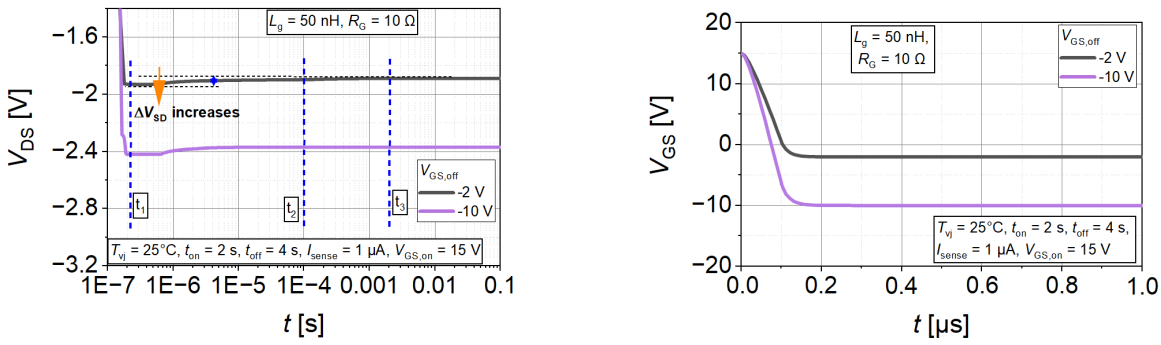


(a) across channel (cut-2) (b) across deep p-region (cut-3)

Fig. 14. Electrostatic potential for two different $V_{GS,off}$ values at different time points (t_6 to t_{10}) with L_g = 1.1 µH. For time points, see Fig. 10(a).

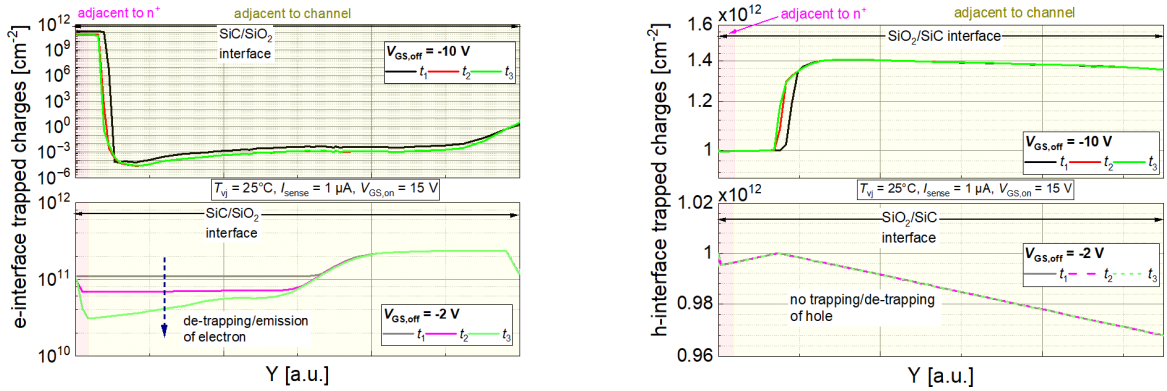
TCAD simulation results at L_g = 50 nH

Fig. 15 presents the simulated dynamic V_{SD} behaviour for L_g of 50 nH. The simulated results show good agreement with corresponding measurements in Fig. 7. Due to the relatively small gate loop inductance, no oscillations (no undershoot) in V_{GS} are observed. For V_{GS} of -2 V, the V_{SD} behaviour exhibit a slow exponential increase between 200 ns to 5 ms, after which it reaches a steady-state value. To analyze this behaviour, the electron and hole trapping dynamics at the SiC/SiO_2 interface were examined at three representative time points during the transient, as shown in Fig. 16. At V_{GS} of -2 V, all available electron traps are initially filled from the preceding on-state condition, see Fig. 16(a). The combination of fully occupied traps and a still weakly inverted channel explains the initial increase in ΔV_{SD} observed at 200 ns, in contrasting to the high-inductance case discussed in Fig. 10(a). Due to the missing undershoot in V_{GS} at L_g of 50 nH condition, the accumulated holes for quick neutralization are missing. Over time, gradual and slow electron de-trapping occurs, approaching saturation after several milliseconds. The release of trapped charge locally modifies the electrostatic potential leading to a slightly decreasing effective V_{th} and reduced V_{SD}, thereby modulating the current distribution between the inversion channel and the body-diode pn-junction. In contrast, for V_{GS} of -10 V, the channel is fully depleted. The strong negative bias attracts holes to the interface, leading to efficient neutralization of trapped electrons. Under these conditions, the V_{SD} stabilizes after approximately 1 µs with no significant change in trapped charge. The corresponding electrostatic potential distribution are shown in Fig. 17. For V_{GS} of -10 V, the potential decreases slightly within the first 200 ns and subsequently saturates without further variation. In contrast, under V_{GS} of -2 V, the potential exhibits a gradual reduction over time, consistent with the progressive de-trapping process as shown in Fig. 17(b). This behaviour is opposite to that observed under high L_g conditions, highlighting the critical role of gate-loop inductance and V_{GS} undershoot behaviour in shaping the dynamic V_{SD} response.



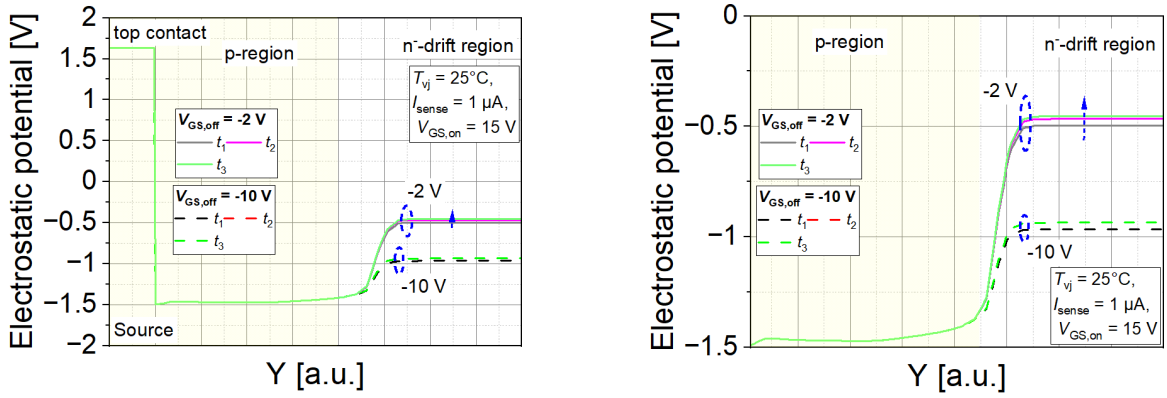
(a) V_{DS} (b) V_{GS}

Fig. 15. Simulated dynamic V_{SD} behaviour of the trench-gate M1 device with gate loop inductance of 50 nH for different $V_{GS,off}$ values at a given conditions. Note: the time scaling for the V_{DS} is logarithmic, and for the V_{GS} is linear.



(a) (b)

Fig. 16. Simulated (a) e-interface (b) h-interface trapped charges at the SiC/SiO_2 interface for two different $V_{GS,off}$ values at different time points with L_g = 50 nH. For time points, see Fig. 15(a). cut-1 at interface. Electrons de-trap very slowly.



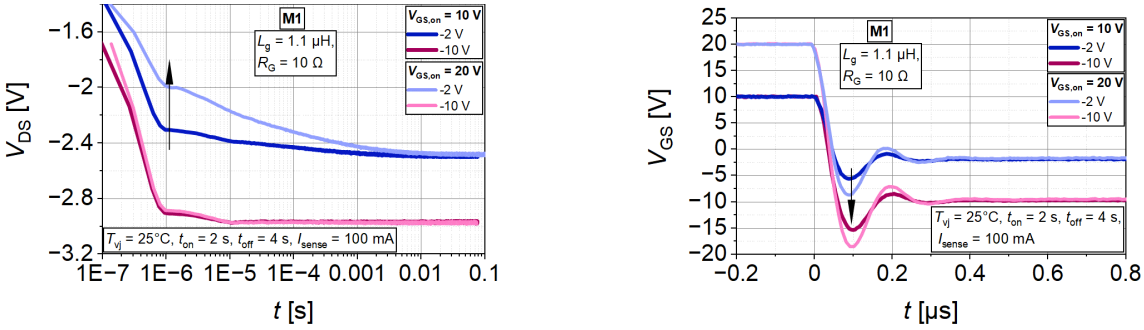
(a) (b) Zoomed plot of Fig. 17(a)

Fig. 17. Electrostatic potential across deep p-region (cut-3) for two different $V_{GS,off}$ values at different time points with L_g = 50 nH. For time points, see Fig. 15(a).

Influence of the $V_{GS,on}$

Fig. 18 illustrates the influence of different $V_{GS,on}$ values under fixed measurement conditions with L_g of 1.1 µH. As the gate voltage is switched from higher levels, the undershoot peak during gate turn-off increases [Fig. 18(b)]. This effect directly correlates with a reduction in the measured V_{SD} at

1 µs [Fig. 18(a)]. The observed behaviour can be explained by the stronger negative V_{GS} undershoot occurring immediately after turn-off, which dynamically reduces the effective V_{th} through enhanced hole trapping at the SiC/SiO_2 interface leading to more electrons neutralization quickly. As a result, the channel remains slightly more conductive for a longer duration, thereby reduced voltage drop across the device [3, 12].



(a) V_{DS} (b) V_{GS}

Fig. 18. Measured dynamic V_{SD} behaviour of the trench-gate M1 device with L_g of 1.1 µH for different $V_{GS,on}$ values at a given conditions. Note: the time scaling for the V_{DS} is logarithmic, and for the V_{GS} is linear.

Other parameters influence

In the following section the influences of the sense current and the junction temperature will be discussed. However, there was no influence of the t_{on} found in this work which means the on-time is long enough to fully charge the interface traps with electrons.

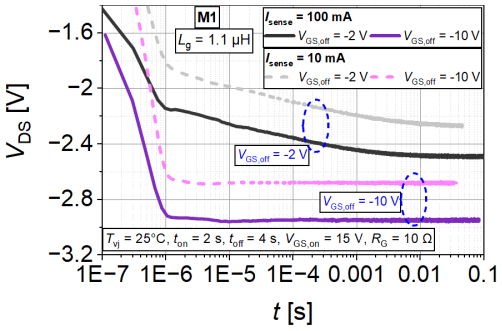


Fig. 19. Comparison of the dynamic V_{SD} behaviour of the M1 device with L_g of 1.1 µH for different sense current values at a given conditions.

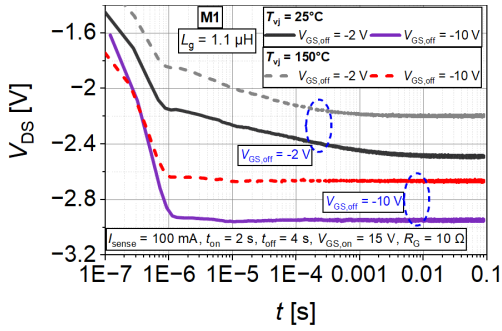


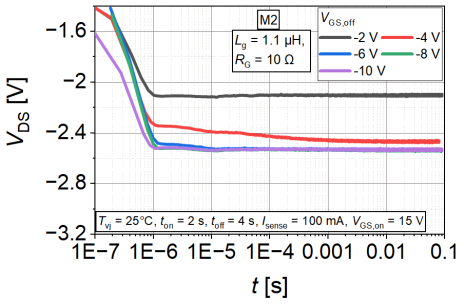
Fig. 20. Comparison of the dynamic V_{SD} behaviour of the M1 device with L_g of 1.1 µH for different junction temperature values at a given conditions.

Fig. 19 compares the influence of two different sense currents I_{sense} for $V_{GS,off}$ of -2 V and -10 V. In general, a lower sense current results in a reduced voltage drop. For $V_{GS,off}$ of -2 V, where the channel is not fully pinched off, reducing I_{sense} by a factor of ten, leads to a slower decay in the dynamic V_{SD} compared to the 100 mA case. This behaviour is attributed to the reduced current conduction through both the channel and the body diode. The lower carrier density at the SiC/SiO_2 interface with less hole available for neutralization consequently slows down the trapping process. In contrast, for $V_{GS,off}$ of -10 V, the lower I_{sense} results in an lower voltage drop and remains approximately constant during t_{off} as the channel is fully closed.

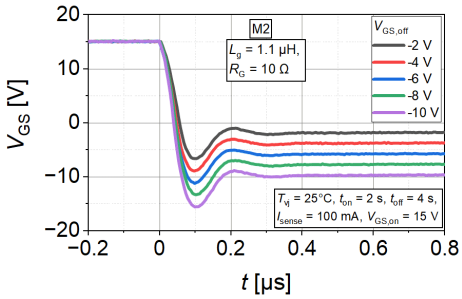
As the junction temperature increases, the built-in potential of the body diode decreases due to the rise in intrinsic carrier concentration (n_i), as illustrated in Fig. 20. For $V_{GS,off}$ of -2 V, where the channel remains partially on, the duration of the transient dynamic V_{SD} response shortens by a few milliseconds at elevated temperatures compared to room temperature. This behaviour can be attributed to the temperature dependence of trap kinetics. Specifically, the capture and emission time constant reduces with increase in temperature, thereby reducing the dynamic V_{SD} behaviour [12]. In addition, due to bandgap narrowing at 150 °C, the bandgap reduces which shifts the trap energy levels

closer to the conduction band, further accelerating the trapping of electrons. For stronger negative gate bias (-10 V), the channel is fully depleted, and the measured voltage drop is lower at 150 °C compared to 27 °C, while maintaining a similar steady-state trend.

Gate technology influence

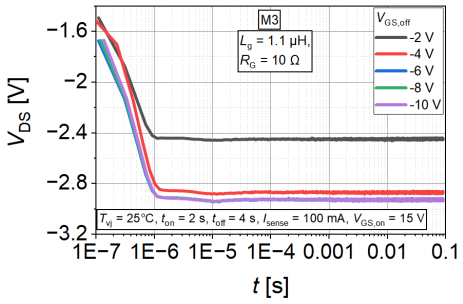


(a) V_{DS}

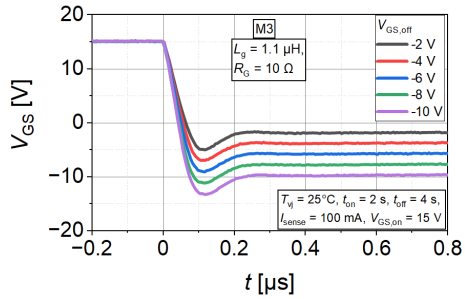


(b) V_{GS}

Fig. 21. Measured dynamic V_{SD} behaviour of the M2 device with L_g of 1.1 µH for different $V_{GS,off}$ values at a given conditions.

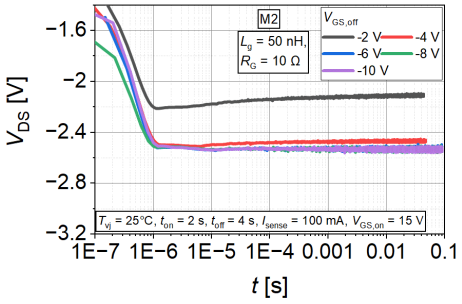


(a) V_{DS}

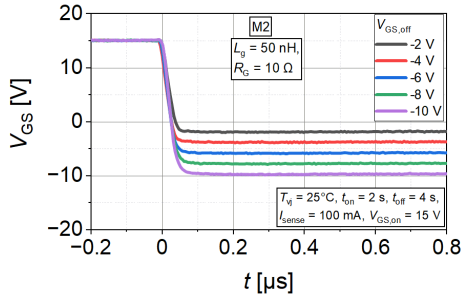


(b) V_{GS}

Fig. 22. Measured dynamic V_{SD} behaviour of the M3 device with L_g of 1.1 µH for different $V_{GS,off}$ values at a given conditions.

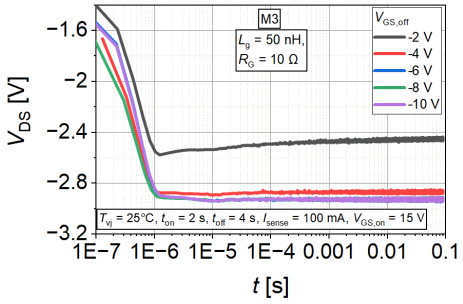


(a) V_{DS}

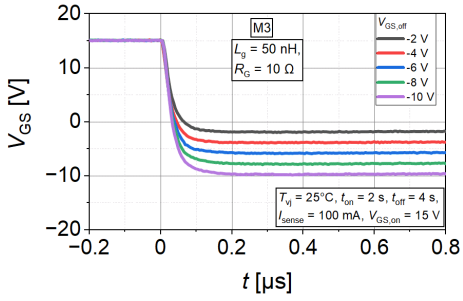


(b) V_{GS}

Fig. 23. Measured dynamic V_{SD} behaviour of the M2 device with gate loop inductance of 50 nH for different $V_{GS,off}$ values at a given conditions.



(a) V_{DS}



(b) V_{GS}

Fig. 24. Measured dynamic V_{SD} behaviour of the M3 device with gate loop inductance of 50 nH for different $V_{GS,off}$ values at a given conditions.

Figures 21 and 22 present the measured dynamic V_{SD} behaviour for the M2 and M3 devices at L_g of 1.1 µH. Compared to the M1 device, the M2 samples exhibit a slightly lower dynamic V_{SD} under partially-on channel conditions. This reduction is attributed to the smaller V_{GS} undershoot and overshoot, resulting from their relatively higher input capacitance (C_{iss}) and internal gate resistance ($R_{G,int}$). The M3 device show the weakest transient V_{SD} response among the three manufacturers. This behaviour is consistent with their highest $R_{G,int}$ and C_{iss}, which together suppress gate-voltage oscillations and thus minimize the undershoot in V_{GS}. Additionally, each manufacturer has different interface trap density. At a reduced gate-loop inductance of L_g of 50 nH, however, the dynamic V_{SD} behaviour of both M2 and M3 devices closely resembles that of the M1 device, as shown in Figures 23 and 24. These results indicate that device-specific parameters such as $R_{G,int}$ and C_{iss} have a pronounced effect on the transient V_{SD} only under high- L_g conditions, whereas their influence becomes negligible when the gate inductance is minimized.

Summary

This work systematically investigates the dynamic voltage drop (V_{SD}) behaviour of SiC MOSFET body diodes under sense-current (I_{sense}) conditions, where the devices are solely driven by gate-voltage switching without external load. Devices from three different manufacturers, encompassing different cell technologies, were analyzed under two gate-loop inductances L_g. The results demonstrate that under partially-on channel conditions in the 3rd quadrant, significant transient V_{SD} responses occur, which can introduce substantial errors in junction temperature (T_{vj}) estimation. Accurate temperature readout thus requires complete n-channel pinch-off by applying sufficiently negative gate voltages, below standard datasheet recommendations. 2D TCAD simulations elucidate the underlying mechanisms: parallel current flow between the n-channel and body diode, coupled with electron trapping, de-trapping and hole accumulation dynamics at the SiC/SiO_2 interface, strongly modulates the transient V_{SD} behaviour. High gate-loop inductance (L_g of 1.1 µH) induces pronounced V_{GS} oscillations, especially strong V_{GS} undershoots, leading to enhanced hole trapping, thus electron neutralization at the interface and a quick decay in V_{SD} shortly after turning off the device. Afterwards a slower decay is followed mostly dominated by further hole emission effects. In contrast, low gate-loop inductance (L_g of 50 nH) suppresses oscillations and V_{GS} undershoots, producing a slow exponential rise in V_{SD} primarily governed by electron de-trapping via emission. Furthermore, device-specific parameters such as input capacitance (C_{iss}) and internal gate resistance ($R_{G,int}$) strongly influence V_{GS} undershoot and, consequently, the dynamic V_{SD} response and varies with manufacturers. On top the interface quality might be strongly different. Additional factors, including reduced I_{sense} and elevated junction temperature, respectively prolong or shorten the transient V_{SD} duration, highlighting the interplay of electrical and thermal effects. Overall, this study provides a comprehensive understanding of the intrinsic and extrinsic factors controlling transient V_{SD} in SiC MOSFETs, offering critical insights for reliable temperature measurement and device characterization under dynamic gate conditions.

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