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Calculation of the Whole Interface State Density Profile in SiO_2/SiC Lateral MOSFETs

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Abstract. Silicon carbide (SiC) has emerged as a leading material for high-power applications. However, the high density of interface states (D_{it}) at the SiO_2/SiC interface still constrains the performance and reliability of MOSFET devices. In this work, lateral 4H-SiC MOSFETs subjected to post-deposition annealing (PDA) in nitric oxide (NO) of different durations were investigated through capacitance-voltage measurements, supported by an analytical model and an iterative MATLAB-based D_{it} extraction algorithm. The results demonstrate that NO PDA effectively reduces D_{it} not only near the conduction band edge but also towards the valence band, yielding improved channel mobility (μ_{FE}) and enhanced threshold voltage stability.

Introduction

Silicon carbide has emerged as the reference material for high-power and high-voltage applications thanks to its superior physical properties. In 4H-SiC MOSFETs, these properties allow for enhanced voltage and current ratings as a consequence of the high critical electric field combined with intrinsically lower conduction resistance. A major challenge, however, arises from the relatively high density of interface states (D_{it}) at the oxide/semiconductor interface, which remains significantly larger with respect to Si. Interface states have been widely recognised as a critical factor that degrades fundamental device parameters, including the field-effect channel mobility (μ_{FE}) and the on-resistance (R_{ON}) [1,2]. The impact of D_{it} on conduction is strongly dependent on the processing of the SiO_2/4H-SiC interface [3] and can be mitigated by post-oxidation annealing (POA) or post-deposition annealing (PDA) in NO ambient [4]. However, introducing nitrogen during PDA can create trapping states at the SiO_2/4H-SiC interface, potentially negatively affecting the stability of the threshold voltage (V_{th}) [5,6].

In this context, it is crucial to investigate the evolution of the D_{it} not only near the 4H-SiC conduction band but also those close the valence band, as well as the near-interface oxide traps (NIOTs) that may form during prolonged PDAs in NO.

In this work, experimental and simulated capacitance-voltage (C-V) measurements were carried out on lateral MOSFETs subjected to PDAs of different duration in NO ambient [7], in order to investigate the electrical evolution of D_{it} across the entire wide bandgap of the SiO_2/4H-SiC system. Unlike MOS capacitors, which do not allow a complete evaluation of D_{it} over the entire semiconductor band gap, lateral MOSFETs enable direct access to the full 4H-SiC band gap.

Experimental

This study is focused on lateral n-channel MOSFETs with the p-type body obtained by Al ion implantation into an n-type epitaxial layer with a doping concentration of approximately $N_D=9\cdot10^{15}$ cm^{-3}. The implantation process was optimised by adjusting both fluence and ion energy

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to achieve a uniform doping profile within the body, resulting in a final concentration in the range of N_A=2-3·10^{17} cm^{-3}. The oxide layer was subsequently deposited by Low Pressure Chemical Vapour Deposition (LPCVD), with process parameters controlled to obtain an average thickness of about 55 nm, as confirmed by capacitance measurements of MOSFETs in the accumulation regime [7]. Post-deposition annealing (PDA) was then performed for different durations, specifically 10, 20, 50 and 120 minutes, with the aim of identifying an optimal processing window that maximises the passivation effect of the treatment while avoiding secondary effects, such as defect formation induced by prolonged exposure to high temperatures in a NO ambient.

Results

The MOSFETs were characterised by measuring capacitance-voltage (C-V) curves using a CASCADE Microtech probe station equipped with a Keysight B1505A parameter analyser. *Figure 1* reports the C-V characteristics acquired at 1 kHz and room temperature, with the gate voltage swept from −20 V to +10 V, i.e. from accumulation to inversion.

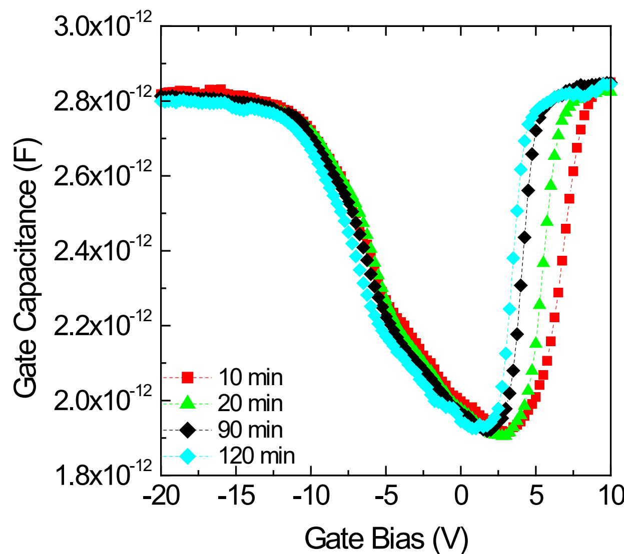

Fig. 1. C-Vs measured on the different MOSFETs subjected to different PDAs in NO.

As shown in *Figure 1*, increasing the duration of NO annealing modifies the slope of the C-V curves. Although the overall shape of the experimental curves remains similar, differences emerge in the positive gate voltage region, where a progressive increase in the slope can be observed as the annealing time extends from 10 to 120 minutes. This behaviour indicates the effectiveness of post-deposition annealing in reducing the density of interface states near the conduction band. A corresponding shift of the minimum point of the C-V curves towards more negative gate voltages is also observed with increasing annealing duration. In addition, for gate voltages below −5 V, a slight variation in the slope can be observed, which may be attributed to changes in the interface states located close to the valence band. Taken together, these features suggest the evolution of the D_{it} profile as a function of annealing in NO ambient.

Following the electrical characterisation of the MOSFETs, the density and distribution of interface states were evaluated using an analytical model. For this purpose, an in-house MATLAB algorithm was developed to extract the D_{it} profile in MOSFET structures through an iterative procedure. The model, derived from the ideal C-V response of a MOS structure without interface states, accounts for their contribution as a function of energy level and density, thereby generating a modified C-V profile that reproduces the experimental data acquired. In particular, the model iterates on a set of pre-defined level with specific energy dispersion (exponential, Gaussian etc.) in order to achieve the best fit of the experimental C-V curves.

In order to simplify the analysis, the incorporation of traps was represented using analytical mathematical profiles such as Gaussian, exponential, or linear functions, which ensure mathematical continuity for any energy value within the bandgap and allow the construction of a trap density profile across the semiconductor band gap. As a reference for this modelling, discrete energy levels reported in the literature were incorporated, including bulk defects such as carbon clusters and silicon or carbon vacancies [8], as well as interface defects associated with the incorporation of NO molecules [9], as shown in *Figure 2*.

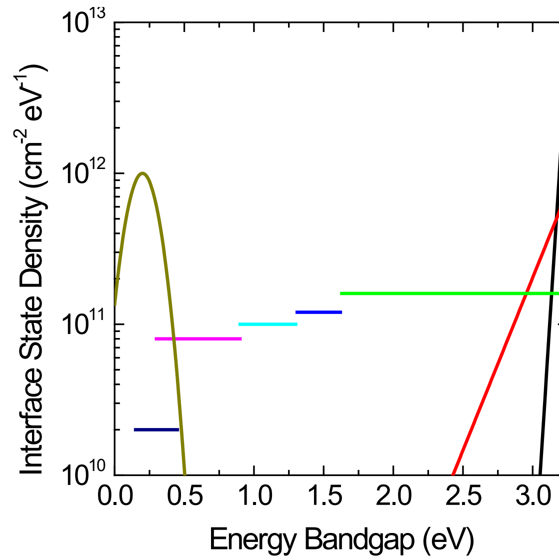

Fig. 2. Discrete levels used to calculate the Dit profile in the whole 4H-SiC band gap.

These assumptions came from the hypothesis that the bulk semiconductor levels can be mirrored at the interface with the SiO_2 insulating layer.

To provide a detailed description of the adopted approach, *Table 1* summarises the main characteristics of the interface states considered in the iterative simulation. Both the trap type (donor or acceptor) and the mathematical distribution used for their representation (Gaussian, uniform, or exponential) are reported, together with their corresponding energy position within the bandgap and their relative weight. These centres were then combined to construct the overall D_{it} profile, which was subsequently used to evaluate the modifications induced by PDA across the 4H-SiC band gap.

Table 1. Mathematical functions associated to each discrete level for the fitting of the C-V curves.

Trap Type	Distribution Shape	Energy Position (from E_V) [eV]	Length [a.u.]
Donor	Gaussian	0.2	0.1
Donor	Uniform	0.3	0.3
Donor	Uniform	0.6	0.6
Donor	Uniform	1.1	0.4
Donor	Uniform	1.5	0.4
Acceptor	Uniform	2.4	1.8
Acceptor	Exponential	3.26	0.19
Acceptor	Exponential	3.26	0.03

The constructed trap profiles were incorporated into the ideal C-V response of MOSFETs, allowing close agreement with the experimental measurements. As a representative case, *Figure 3*

presents the fitting of the C-V curve measured after 120 minutes of PDA, obtained through the MATLAB iterative loop simulation with a trap profile specifically developed for this condition. The good agreement between experiment and simulation highlights the capability of the adopted model to capture the contribution of interface states across the 4H-SiC bandgap.

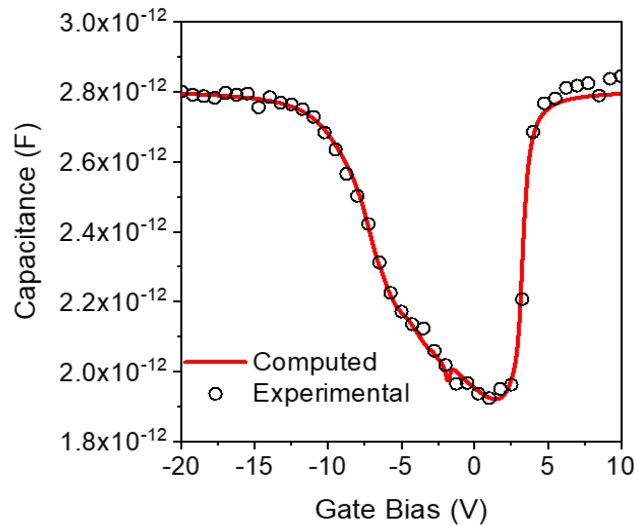

Fig. 3. Example of an experimental C-V curve (120 min of PDA) fitted by the iterative MATLAB loop.

In particular, the use of an exponential trap profile near the conduction band of the semiconductor has a significant impact on the charge accumulated in these interface states and, consequently, on the total capacitance of the device. At high trap densities, the charge stored in the trap energy levels becomes non-negligible, leading to an increase in capacitance at fixed gate bias values and resulting in a modification of the final C-V curve. Similarly, donor-like traps introduced near the valence band induce variations in the C-V characteristics, especially for gate bias values below −5 V.

By extending the analysis to all NO PDA durations, the variations induced by the different annealing times could be identified as is shown in *Figure 4*. The results show that increasing the annealing time in NO reduces the exponential tail of the D_{it} profile near the 4H-SiC conduction band edge, while also decreasing the states located below the mid-gap and close to the valence band edge.

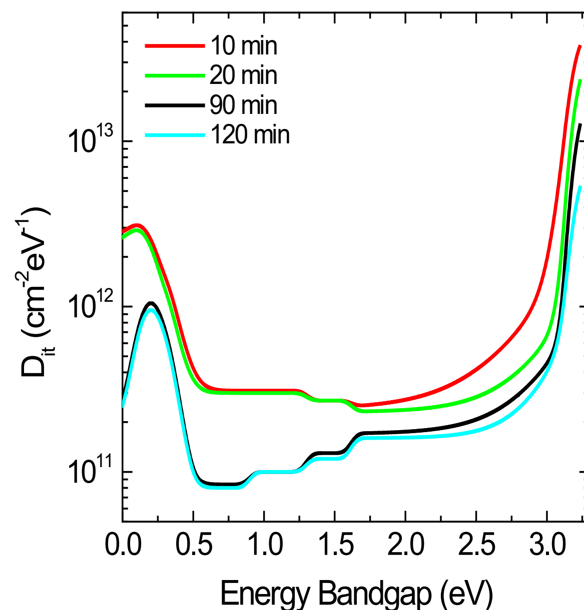

Fig. 4. Dit profiles obtained on the different MOSFETs subjected to different PDAs in NO.

These combined experimental and simulated findings are consistent with an enhancement of the field-effect channel mobility (μ_{FE}) and a reduction of V_{th} instability when the PDA is sufficiently long, as previously reported [10].

Conclusion

The results presented in this work demonstrate that NO PDA treatments induce a progressive reduction of interface states not only close to the 4H-SiC conduction band edge but also near the valence band. This finding contrasts with earlier studies that reported a detrimental effect near the valence bandgap edge [11]. The combined experimental and simulated analyses further confirm that sufficiently long PDA durations lead to an enhancement of the μ_{FE} and a reduction of V_{th} instability. Nonetheless, achieving a reliable improvement in interfacial transport properties requires a fine control of the PDA conditions in order to maximise the beneficial passivation effect while avoiding the onset of secondary mechanisms that could reintroduce defects or compromise threshold voltage stability.

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