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Investigation of the P-Body Effect on Reverse Recovery and Static Characteristics of 1.2 kV 4H-SiC Power MOSFET

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Abstract. We have introduced a new 1200V 4H-SiC MOSFET as Wolfspeed's Gen4 MOSFET, which offers compatible Rds,on, improved dynamic switching energy losses, reduced Qrr, and enhanced short circuit withstand time performance. In this study, we examine the P-body effect resulting from multi-step ion implantation and its significant impact on both the static and dynamic characteristics of SiC MOSFETs, specifically focusing on body-diode reverse recovery, short circuit withstand time (Tscwt), and observed switching energy losses in the 1.2 kV 4H-SiC power MOSFETs within this Gen4 series. Our findings are expected to contribute valuable insights into optimizing the design and operation of SiC MOSFETs, ultimately supporting the needs of modern power electronic systems that demand greater performance and efficiency.

Introduction

Silicon carbide (SiC) power metal-oxide-semiconductor field-effect transistors (MOSFETs) are recognized as advanced power semiconductor devices that enable a wide array of highly efficient, high-power electronic applications. This remarkable capability primarily arises from their wide bandgap characteristics, which enhance performance in demanding operational environments [1, 2]. As the demand for higher efficiency and reliability in power electronic systems continues to grow, recent advancements in this field focus on minimizing the on-resistance (Rds,on) of these devices to significantly reduce conduction losses. However, achieving this goal often requires careful consideration of trade-offs between key design parameters, as elaborated in our previous reports [3, 4, 5]. Based on our thorough analysis of these trade-off relationships, we have successfully launched a new 1200V 4H-SiC MOSFET as Wolfspeed's Gen4 MOSFET. This device offers competitive Rds,on, improved switching energy losses, reduced Qrr, and notably enhanced short circuit withstand time performance. Such improvements are vital for applications in sectors such as renewable energy, electric vehicles, and industrial power systems, where performance and reliability are paramount [2 – 6]. This paper aims to explore the P-body effect resulting from the multi-step ion implantation process, which significantly impacts not only the static characteristics of SiC MOSFETs but also a range of dynamic characteristics. Among these are performance metrics related to body-diode reverse recovery, short circuit withstand time (T_{scwt}), and the switching energy losses observed in the 1.2 kV 4H-SiC power MOSFETs that are part of Wolfspeed's Gen4 series. By understanding these effects, we can further optimize device performance and contribute to the next generation of high-efficiency power electronics.

1.2kV 4H SiC MOSFET structure and Experiment

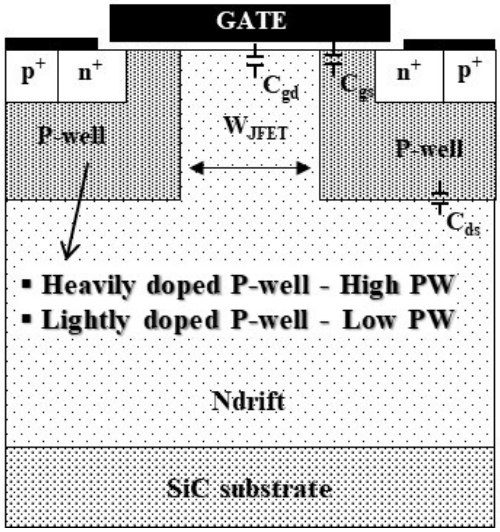

Fig. 1. Schematic cross-sectional view of 1.2 kV 4H-SiC Power MOSFETs.

Figure 1 illustrates a simplified cross-sectional view of a 1.2 kV SiC power MOSFET, clearly depicting the structural elements integral to its function. It highlights critical design parameters such as the width of the JFET (W_{JFET}), gate-drain capacitance (C_{gd}), gate-source capacitance (C_{gs}), and the influence of the n-drift region. These parameters play a crucial role in determining the overall performance of the device, impacting factors like switching speed and efficiency. In our experiments, we varied the P-well doping concentration at two distinct levels to comprehensively investigate the impact of P-well doping on the P-body effect. Specifically, we denote these configurations as High PW and Low PW, which differ in their implantation dose levels. This variation enables us to analyze how different doping concentrations influence device characteristics, such as on-resistance, switching behavior, and reliability. Furthermore, understanding these effects will provide valuable insights into optimizing the design of SiC MOSFETs for high-power applications. The outcomes of our study will contribute to enhancing the performance and efficiency of next-generation power semiconductor solutions.

Electrical Results

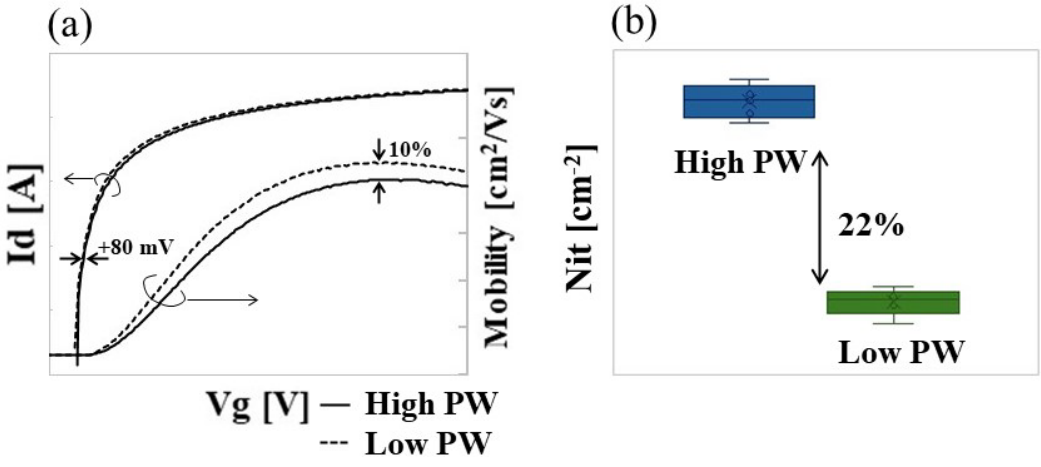

Fig. 2. (a) Id and Mobility comparison for two P-wells in lateral MOSFETs, (b) Nit between two P-wells for charge pumping test.

The experimental results, presented in Figures 2(a) and (b), depict the relationships between drain current (I_d) and both the calculated field-effect mobility (μFE) and trap density (Nit). These were meticulously measured using the charge pumping (CP) method [5], applied specifically to lateral SiC

MOSFETs. These results expose the significant impact of P-well doping on the channel properties of the MOSFET. Notably, the High PW configuration exhibits a threshold voltage (V_{th}) that is 80 mV higher than that of the Low PW configuration. In contrast, the field-effect mobility μFE is approximately 10% lower in the High PW samples. Additionally, the trap density Nit is found to be about 22% greater in samples with higher P-well doping. These findings suggest that the doping concentration of the P-well can significantly influence the channel properties through gate oxide surface effects, which extend beyond merely adjusting the channel V_{th} due to a greater implantation dose of the P-well. The interplay between doping levels and channel characteristics is critical, as it governs the overall efficiency and performance of the MOSFET. Moreover, the increased trap density associated with higher doping concentrations may lead to greater charge trapping effects, potentially impacting the reliability of the device under high-frequency and high-temperature conditions. Understanding these interactions will not only aid in optimizing device design but also provide insights into the long-term stability and efficiency of SiC MOSFETs in various applications.

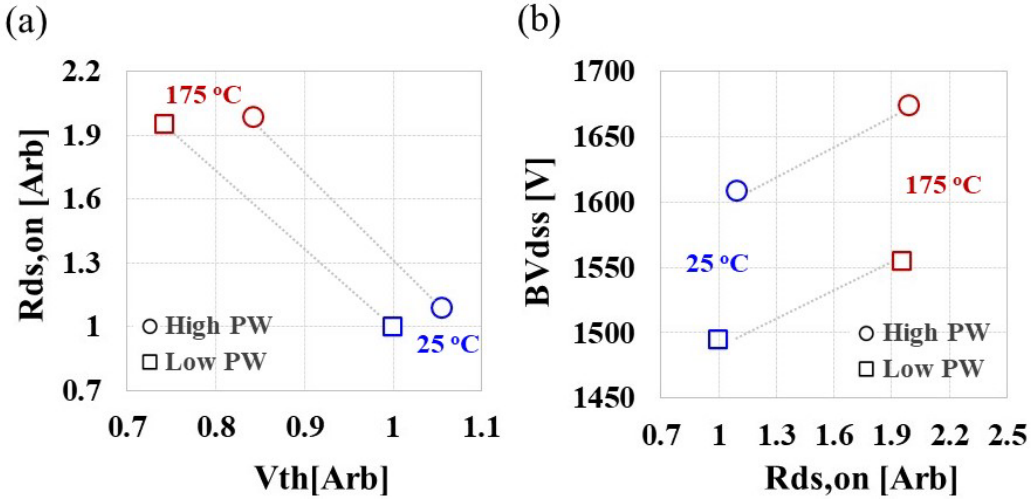

Fig. 3. Static characteristic for two P-wells at 25 and 175 ºC. (a) Normalized Rds,on versus Vth (b) BVdss versus Normalized Rds,on.

Figure 3 presents the static characteristics of the 1.2 kV 4H-SiC Power MOSFET at two temperatures: 25 °C and 175 °C. Within this figure, 3(a) and (b) depict the normalized Rds,on as a function of Vth, alongside the breakdown voltage (BVdss) versus Rds,on, respectively. As shown in Figure 3, the High PW configuration exhibits Rds,on values that are 9.32% and 13.24% greater than those of the Low PW configuration at 25 °C and 175 °C, respectively. Additionally, High PW also shows Vth values that are 5.4% and 1.8% higher than Low PW at 25 °C and 175 °C. Furthermore, High PW demonstrates around 115V greater BVdss compared to Low PW at both temperature points, primarily as a result of JFET pinching influenced by the heavy doping of the P-well. The results clearly indicate that the High PW configuration exhibits higher values for V_{th}, Rds,on, and BVdss in comparison to the Low PW configuration, which is consistent with the findings presented in Figure 2. The trends observed suggest that higher P-well doping concentrations lead to enhanced threshold voltage and on-resistance characteristics. Moreover, the rate of increase in Rds,on at 175 °C, is noted to be less pronounced compared to the behavior exhibited at 25 °C when P-well doping increases. This behavior underscores that the variation in the doping profile of the P-well is more dominant in shaping the channel property characteristics, particularly at elevated temperatures. These findings have important implications for the operation and reliability of the device under varying temperature conditions. By gaining insight into these relationships, we can better optimize design parameters to enhance performance and mitigate potential thermal degradation in high-temperature applications. Ultimately, understanding the influence of P-well doping on these key characteristics will provide a pathway to developing more efficient and reliable SiC MOSFETs for demanding applications in the power electronics landscape.

In Figure 4, the measured normalized parasitic capacitance plots (C_{iss}, C_{oss}, and C_{rss}) for both doping configurations are presented. The results indicate that for the High PW configuration, C_{iss} is approximately 5.5% higher compared to the Low PW configuration, while C_{rss} is around 33% lower. These differences can be attributed to the higher levels of P-well doping, which positively influence the device characteristics. Additionally, the changes in these capacitances also account for the increased breakdown voltage (BVdss) observed in Figure 3(b).

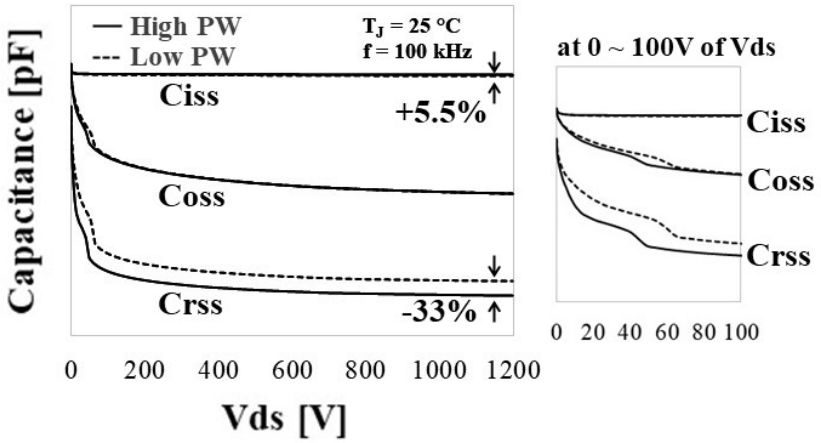

Fig. 4. C-V characteristics (C_{iss}, C_{oss}, C_{rss}) for two P-wells at 25 °C.

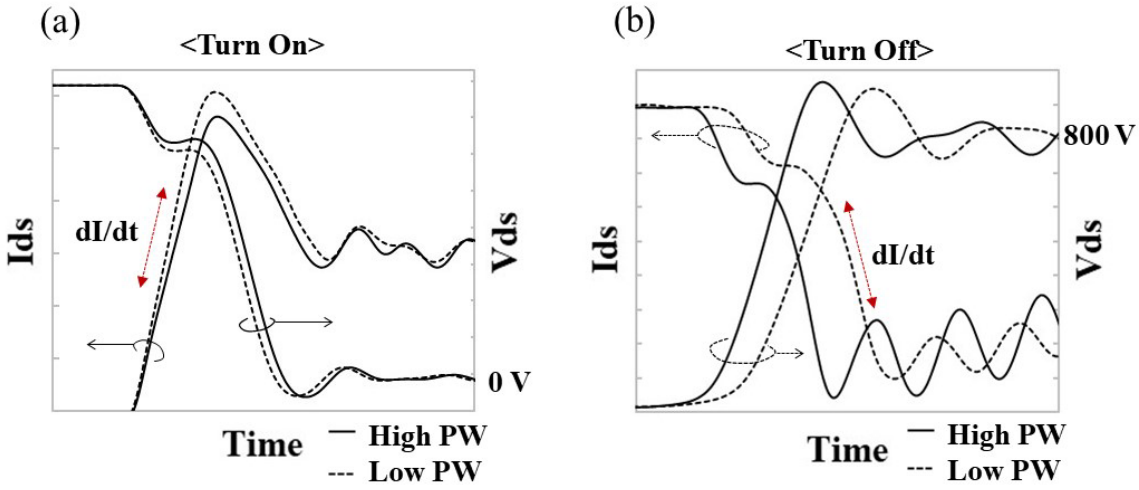

Fig. 5. Double Pulse Test (DPT) waveforms for two P-wells at 175 °C. (a) Turn on (b) Turn off.

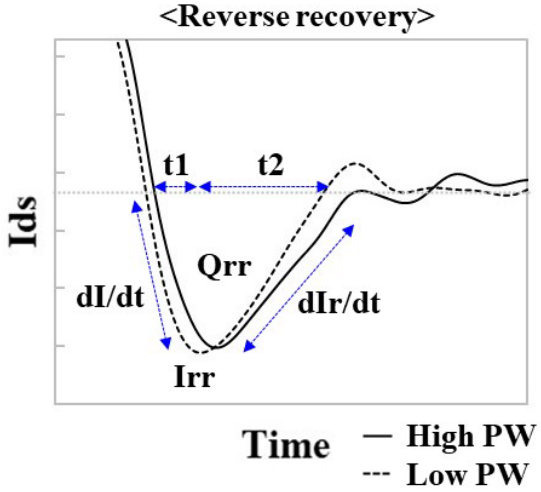

Fig. 6. Reverse recovery (Q_{rr}) waveforms for two P-wells at 175 °C.

Table 1. Normalized DPT and reverse recovery characteristics based on Fig. 5 and 6.

		Low PW	High PW
DPT	dI/dt on	1	0.862
	Eon	1	1.055
	di/dt off	1	1.103
	Eoff	1	0.708
Reverse Recovery	dI/dt	1	0.978
	dIr/dt	1	0.789
	Irr	1	0.969
	Qrr	1	1.203

Furthermore, Figure 5 illustrates the switching waveforms obtained from the double pulse test (DPT), which are essential for comparing the switching characteristics of MOSFETs with the High PW and Low PW doping levels during the Turn On process (Figure 5(a)) and the Turn Off process (Figure 5(b)). Additionally, Figure 6 presents the reverse recovery characteristics, providing a comparative analysis of the body diode performance for both doping samples. The normalized switching parameters, including dI/dt, switching energy losses (E_{on} and E_{off}), and dIr/dt, are meticulously summarized in Table 1. The High PW configuration exhibits a lower dI/dt during the Turn On phase, accompanied by a higher Eon compared to the Low PW configuration. Conversely, during the Turn Off phase, the High PW configuration demonstrates a higher dI/dt while maintaining a lower E_{off} value. These observed behaviors can be attributed to the reduced channel mobility that arises from the increased levels of P-well doping. In terms of reverse recovery characteristics, the High PW configuration displays a lower dIr/dt and reverse recovery current (I_{rr}), while also exhibiting a greater reverse recovery charge (Q_{rr}) compared to the Low PW configuration. The heavily doped P-well influences the performance, contributing to a lower softness factor in the body diode, albeit at the cost of an increased Q_{rr} value. Furthermore, it is noteworthy that the High PW configuration demonstrates a higher forward voltage drop (V_{sd}) across the body diode when the gate is fully turned off, although plots illustrating this aspect are not included here. These insights into the switching and recovery characteristics underscore the complex trade-offs associated with varying doping levels in MOSFET designs. Understanding these relationships is essential for optimizing device performance in specific applications, particularly where fast switching and efficient energy management are critical. The findings provide a solid foundation for future studies aimed at refining doping strategies and enhancing overall MOSFET performance in high-power and high-frequency applications.

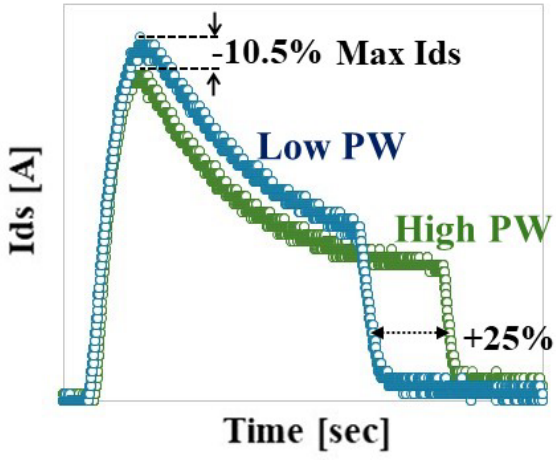

Fig. 7. T_{scWT} waveform (V_{ds}=800V) comparison at 175ºC for two P-wells.

In Figure 7, a comparison of short-circuit current waveforms is presented at a drain-source voltage (V_{ds}) of 800 V. The findings indicate that the High PW configuration exhibited a peak drain current reduction of 10.5% during these events. This decrease in peak drain current during short-circuit incidents is associated with a remarkable improvement in the short-circuit withstand time (T_{scwt}), which is observed to be 25% longer with the heavily doped P-well configuration. These results substantiate the notion that channel mobility, combined with the straggle effects associated with P-well implantation due to elevated doping levels, plays a vital role in enhancing T_{scwt} in these devices. The improved T_{scwt} is critical for ensuring the reliability and robustness of the MOSFETs in demanding applications. Additionally, the reduction in peak drain current not only contributes to better thermal management during faults but also reduces the stress on the device, potentially prolonging its operational life. Overall, the relationship between P-well doping and short-circuit performance highlights the importance of optimizing doping strategies to achieve superior device reliability and performance under extreme conditions.

Conclusion

This study explores the influence of P-well doping levels on the performance of 4H-SiC Power MOSFETs, revealing critical insights into operational efficiency and reliability. The results indicate notable differences between High PW and Low PW configurations in terms of threshold voltage (V_{th}), field-effect mobility (μFE), and trap density (Nit). Specifically, the High PW configuration exhibits a higher V_{th} and trap density, which corresponds to a reduction in μFE. These findings highlight the need for optimizing P-well doping concentrations to enhance device performance while managing associated effects.The static characteristics show that the High PW configuration has increased on-resistance (Rds,on) and breakdown voltage (BVdss) compared to Low PW, with less sensitivity to temperature changes in Rds,on. Such insights are vital for ensuring stable performance in high-temperature applications. Additionally, our analysis of switching characteristics indicates that higher P-well doping results in trade-offs in dynamic performance. The High PW configuration experiences reduced peak drain current during short-circuit events, contributing to a significant improvement in short-circuit withstand time (T_{scwt}). This enhancement is crucial for device reliability in demanding environments.

In conclusion, this research underscores the complex relationship between P-well doping and key MOSFET performance parameters. A deeper understanding of these interactions enables better optimization of device design and doping strategies, leading to more efficient and reliable SiC MOSFETs suitable for high-power and high-frequency applications. Future studies should continue refining doping techniques to further enhance device performance under diverse operational conditions.

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