Key Engineering Materials
ISSN: 1662-9795, Vol. 1055, pp 21-27
doi:10.4028/p-6iQUYo
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Submitted: 2025-09-26
Revised: 2025-12-22
Accepted: 2026-01-31
Online: 2026-05-19

# High-Voltage Performance Evaluation of 6.5 kV 4H-SiC JBSFET Architectures and MOSFET with Enhanced 3rd Quadrant Conduction

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**Keywords:** 4H-SiC, JBSFET, MOSFET, High Voltage, Power Devices, 3rd Quadrant Conduction.

**Abstract.** This paper reports on the comparative analysis of several 6.5 kV-rated 4H-SiC Junction Barrier Schottky integrated MOSFETs (JBSFETs) and 4H-SiC MOSFET to assess their forward conduction, 3rd quadrant behavior, and blocking characteristics. Among different JBSFET architectures, the Island P+ JBSFET achieved nearly identical specific on-resistance ($R_{on,sp}$) to the nominal MOSFET while delivering superior 3rd quadrant conduction and maintaining a high breakdown voltage. Further optimization of Schottky width demonstrated a trade-off between leakage suppression and 3rd quadrant conduction efficiency that underscores the Island P+ JBSFET's potential as a reliable high-voltage SiC power device for next-generation applications.

## Introduction

4H-SiC has become a leading material for next-generation high-voltage power electronics owing to its wide bandgap and high critical electric field. These properties enable thinner and more heavily doped drift layers compared to traditional silicon devices, while still maintaining the same voltage blocking capability. Consequently, 4H-SiC power devices can achieve significantly lower on-resistance at voltage ratings above 600 V, making them highly attractive for high-efficiency and high-power applications [1]. However, the approximately three times higher built-in potential across PN junctions in 4H-SiC results in a larger forward voltage drop in the intrinsic body diode of MOSFETs during 3rd quadrant conduction. To mitigate this, external Junction Barrier Schottky (JBS) diodes are often co-packaged as a freewheeling diode [2,3]. While effective, the use of external diodes increases package area.

In high-voltage SiC power devices, the use of thick epitaxial drift layers leads to an increase in basal plane dislocation (BPD) density, thereby worsening bipolar degradation. As drift resistance ($R_{drift}$) dominates in high-voltage devices, a relatively large JBS diode is required to effectively prevent body diode conduction. This is crucial, as bipolar current not only slows switching speed but also accelerates the growth of BPDs into stacking faults (SFs), which degrade the MOSFET's static characteristics [4]. To improve conduction efficiency, reliability, and area efficiency, the integration of the JBS diode directly into the MOSFET structure has been proposed, resulting in Junction Barrier Schottky integrated MOSFETs (JBSFETs) [5]. This architecture combines unipolar conduction with improved third-quadrant performance, greatly reducing dependency on the body diode and enhancing device robustness under high-stress conditions [6]. Moreover, this introduced Schottky path mitigates the BPD-induced degradation, which poses a critical reliability concern for SiC devices [7].

While JBSFETs may exhibit higher specific on-resistance ($R_{on,sp}$) due to increased cell pitch, structural innovations with efficiently integrated JBS diode enhance the forward conduction, achieving performance comparable to that of MOSFET [8]. Although such performance has been demonstrated in low-voltage devices, replicating this in high-voltage architectures remains challenging. Building on prior work where Stripe JBSFET showed reduced 3rd quadrant forward voltage drop ($V_F$) compared to nominal MOSFET [6], this study extends the technique to enhance the 3rd quadrant conduction, while offering the same $R_{on,sp}$ for high voltage devices. A comparative analysis of JBSFET structures and MOSFET is presented, focusing on structural evolution, trade-offs

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in $R_{on, sp}$, $V_F$, and the role of Schottky width in reducing leakage current for enhanced high-voltage device reliability.

**Device Design and Fabrication**

Fig. 1 illustrates the structural differences between the Stripe JBSFET, Island P+ JBSFET, and the Nominal MOSFET. The Nominal MOSFET, where a P+ source is placed in the orthogonal direction, within the linear topology of the unit cell [9], has a reduced cell pitch compared to the conventional stripe MOSFET approach, with a cell pitch of 6 µm. The Stripe JBSFET features a wide cell pitch of 11 µm to accommodate the integration of the linear Schottky region. The Schottky area is allocated in the x-direction along with the MOSFET cell by interrupting the p-well. The nature of the linear stripe pattern of the JBSFET structure creates long linear Schottky regions along with the MOSFET cell in the *y*-direction. In the Island P+ JBSFET, the Schottky opening is placed in the orthogonal direction, similarly to the MOSFET layout, and is shielded solely by the P-well in the X-direction [8]. As a result, a cell pitch of 6.8 µm was achieved for the Island P+ JBSFET. The structural parameters of each device design are summarized in Table 1.

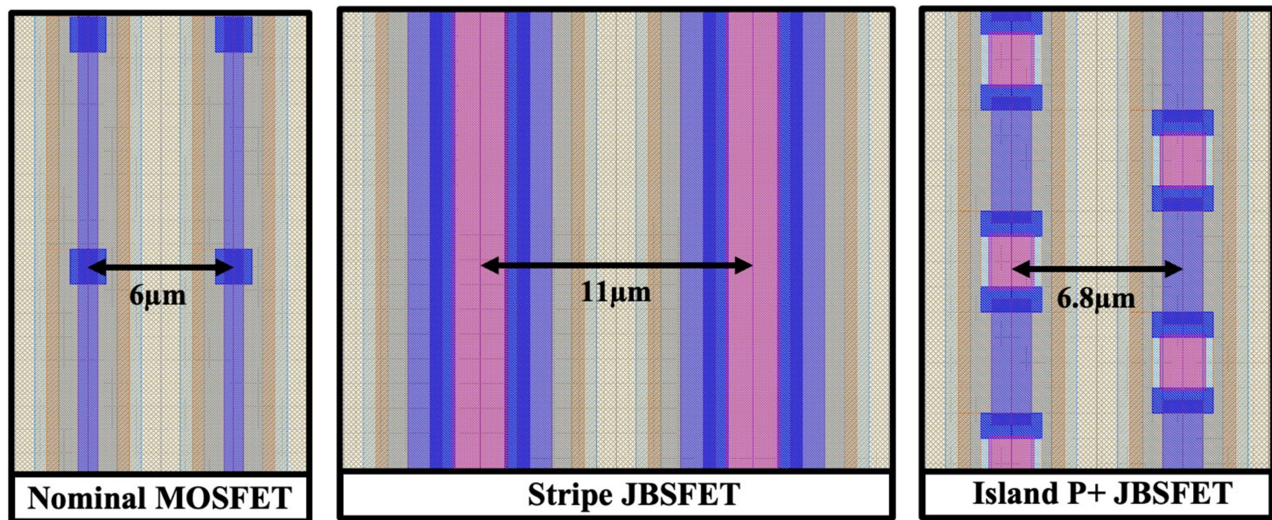


**Fig. 1.** Top layout views of the Nominal MOSFET, Stripe JBSFET, and Island P+ JBSFET structures analyzed in this study.

**Table 1.** Structural parameter summary of each device studied.

| Device Type | Cell Pitch (µm) | Active Area [$mm^2$] | Half JFET Width [µm] | Schottky Open in X-axis [µm] | Shielding in X-axis |
|---|---|---|---|---|---|
| Nominal MOSFET | 6 | 1.70 | 0.8 | N/A | N/A |
| Stripe JBSFET | 11 | 1.70 | 0.8 | 2 | P+ |
| Island P+ JBSFET | 6.8 | 1.70 | 0.8 | 1.6 | P-well |
| | 5.2 | 0.32 | 0.4 | 0.8 | P-well |

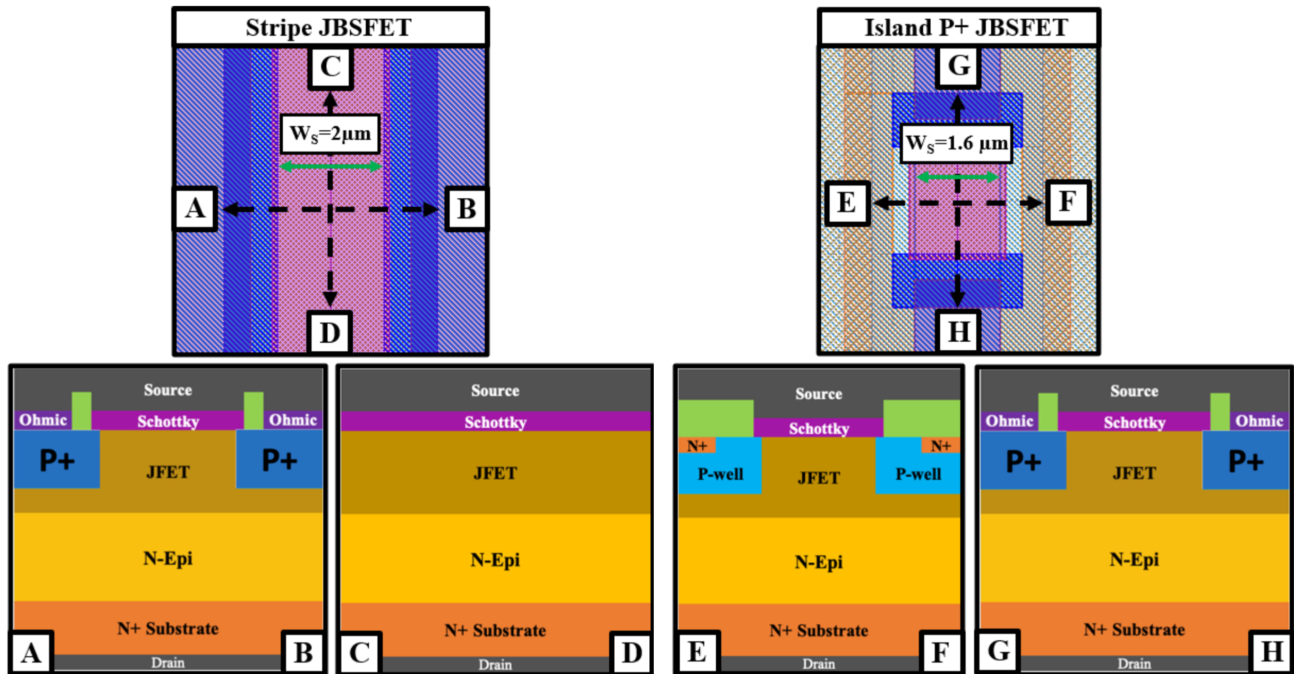


**Fig. 2.** Top layout and cross-sectional views of the Schottky contact regions are presented for the Stripe JBSFET (left) and the Island P+ JBSFET (right), featuring Schottky widths ($W_S$) of 2 μm and 1.6 μm, respectively, as indicated by the green arrows.

Fig. 2 illustrates the Schottky region in the Stripe and Island P+ JBSFET featuring a Schottky width ($W_S$) of 2 μm and 1.6 μm, respectively. Cross-sectional views along the X-direction (A–B and E–F) illustrate how the Schottky region is effectively shielded by the P+ region in the Stripe JBSFET and by the P-well region of the MOSFET in the Island P+ JBSFET. The exclusion of the $P^+$ region in the X-direction leads to a significant reduction in cell pitch, resulting in a compacted JBSFET design, which is slightly larger than that of the nominal MOSFET [8]. In the Y-direction (G–H), the Schottky region in the Island P+ JBSFET is shielded by the P+ region. To ensure a fair comparison, all devices were fabricated with the same active area, JFET width, and channel length of 1.70 $mm^2$, 1.6 μm, and 0.5 μm, respectively. An additional Island P+ JBSFET was evaluated to investigate the impact of a reduced Schottky width (0.8 μm) and a corresponding cell pitch of 5.2 μm on device performance.

A 60 μm thick, $1\times10^{15}$ $cm^{-3}$ doped n-type epi-layer on a 4-inch, N+ 4H-SiC substrate was used to fabricate the JBSFETs, and the Nominal MOSFET. Aluminum ions were implanted to make the P-well and P+, where the Nitrogen ions were implanted to make the N+ source, respectively. Implantation steps were followed by a 1650°C 10 min activation anneal with a carbon cap. A 50 nm thick gate oxide was formed, followed by a POA in nitric oxide ambient. An interlayer dielectric was deposited and etched using the reactive ion etch process by using the gate pad opening mask to open the ohmic and Schottky regions to avoid an additional mask layer. Ni was deposited on the frontside and patterned, followed by 2-min RTA at 1000°C. Back-side metal contact was also formed by Ni deposition and the same RTA process. A Ti/Al stack was then deposited to form the Schottky contacts on the N-epitaxial drift layer and also as a top metal for the source metal and gate pad. Front-side was passivated by nitride and polyimide. Finally, a solderable metal stack was deposited on the backside.

## Results and Discussion

Fig. 3 shows the forward conduction of the Nominal MOSFET, Stripe JBSFET, and Island P+ JBSFET. The specific on-resistance ($R_{on,sp}$), extracted at $I_{ds}$ = 0.15 A and $V_{gs}$ = 20 V, is 42.9 mΩ·cm² for the Stripe JBSFET, 39.9 mΩ·cm² for the Island P+ JBSFET, and 39.7 mΩ·cm² for the nominal MOSFET. Due to the reduced cell pitch of the Island P+ JBSFET, a specific on-resistance ($R_{on,sp}$) comparable to the MOSFET was able to be achieved while also reducing the $R_{on,sp}$ by 7.5% when compared to the Stripe type JBSFET. Therefore, the adoption of the Island P+ cell architecture is successfully able to improve the JBSFET output characteristics for higher voltage applications,

similar to their lower voltage rating counterparts. Even though the ohmic region is reduced, the specific on-resistance ($R_{on,sp}$) of Island P+ JBSFET greatly improved due to the utilization of the entire channel region as a conduction path [8].

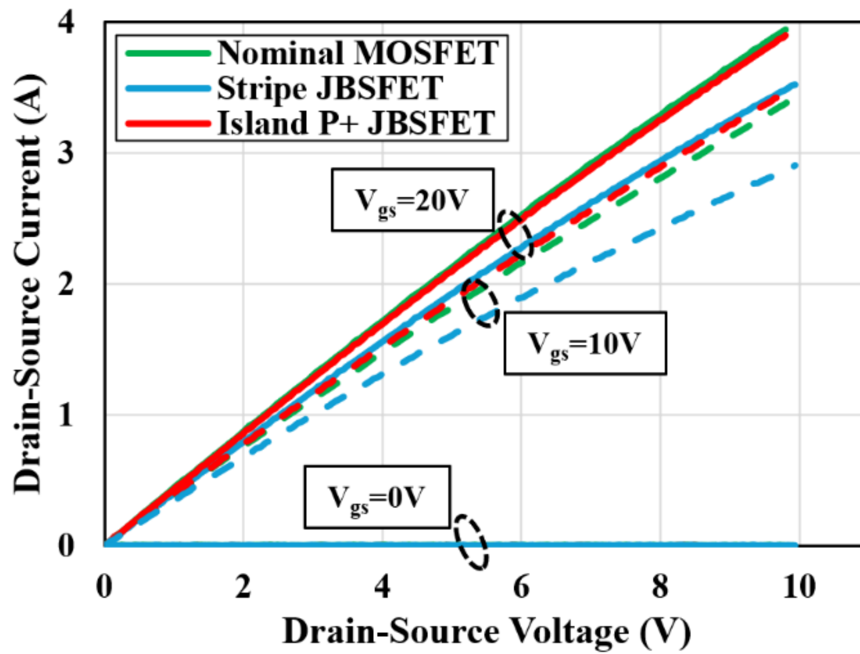


**Fig. 3.** Representative output characteristics of the Nominal MOSFET, Stripe JBSFET, and Island P+ JBSFET were plotted at gate biases of $V_{gs}$ = 0V, 10 V, and 20 V.

Fig. 4 shows the 3rd quadrant characteristics of the Nominal MOSFET, Stripe, and Island P+ JBSFET, measured at a gate bias of $V_{gs}$ = 0 V and -5 V. With a $V_{gs}$ = 0 V, the forward voltage drops ($V_F$), extracted at $I_{ds}$ = 0.5 A, are 6.60 V for the nominal MOSFET, 2.55 V for the Stripe JBSFET, and 2.25 V for the Island P+ JBSFET. A gate bias of $V_{gs}$ = -5V is applied to suppress channel conduction and isolate the body-diode and Schottky paths. Notably, despite the discontinuity of the Schottky region in the Island P+ JBSFET, the aggressive cell pitch design increases Schottky density,

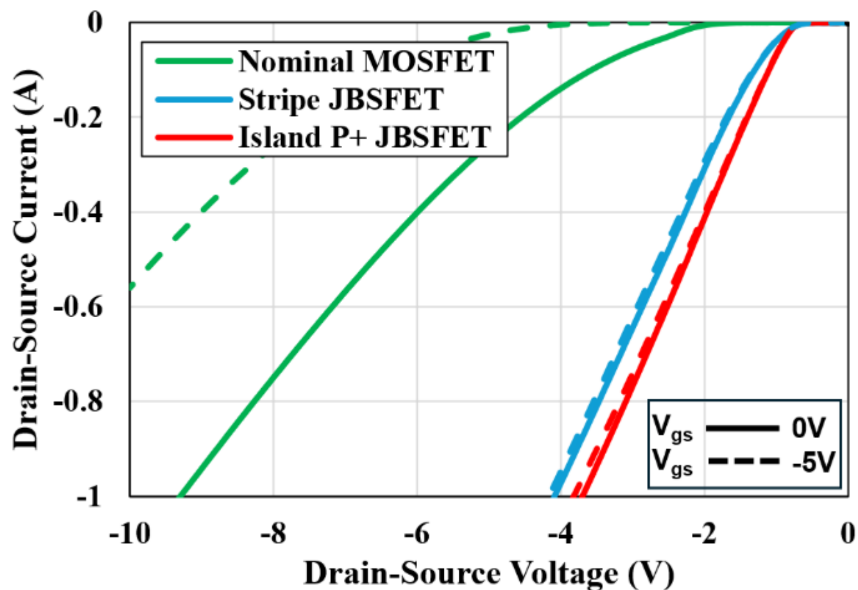


**Fig. 4.** The 3rd quadrant characteristics of the Nominal MOSFET, Stripe, and Island P+ JBSFET structures were plotted at a gate bias of $V_{gs}$ = 0 V and -5 V.

resulting in highly efficient unipolar current conduction and a substantial reduction in $V_F$. These results confirm that Island P+ JBSFET exhibits a lower $V_F$ than the Stripe JBSFET and outperforms the MOSFET during the 3rd quadrant operation.

Fig. 5 shows the forward blocking output characteristics of the Nominal MOSFET, Stripe, and Island P+ JBSFETs, measured at a gate bias of $V_{gs}$ = -5V to minimize any leakage through the channel. The Stripe JBSFET exhibits the highest leakage current due to the strong electric field beneath its large Schottky region [8], which leads to a soft breakdown. In contrast, the Island P+ JBSFET demonstrated significantly lower Leakage current, largely attributed to the fully surrounded Schottky contact, effectively shielding the contact during the blocking mode of operation [10]. However, the Island P+ JBSFET still demonstrated an increased leakage when compared to the nominal MOSFET. Both the nominal MOSFET and the Island P+ JBSFET exhibited avalanche breakdown at approximately 8.3 kV, confirming the superior blocking capability of the Island P+ design compared to the Stripe JBSFET.

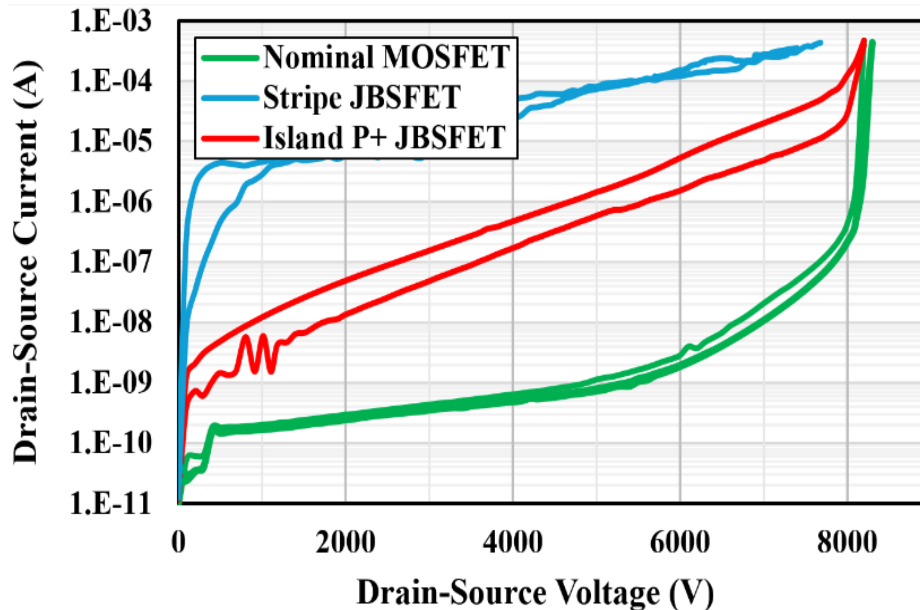


**Fig. 5.** Forward blocking output characteristics of the Nominal MOSFET, Stripe, and Island P+ JBSFETs were measured at a gate bias of $V_{gs}$ = -5V to minimize any leakage through the channel.

Due to the larger leakage current observed within the Island P+ JBSFET, further designs were investigated with the goal of suppressing the overall leakage current during the blocking mode of operation. For this, an alternative Island P+ design with a reduced Schottky width of 0.8 µm was investigated. The resulting forward blocking and 3rd quadrant output characteristics for the Island P+ JBSFETs with Schottky widths ($W_S$) of 1.6 µm and 0.8 µm are compared in Fig. 6. By reducing the

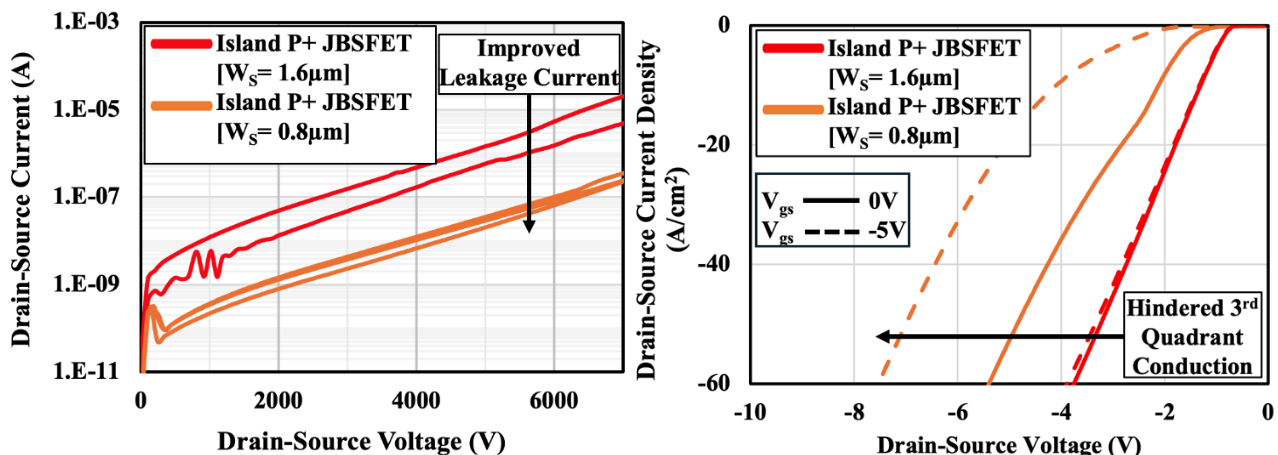


**Fig. 6.** The 3rd quadrant (left) and the forward blocking (right) characteristics of the Island P+ JBSFET structure with $W_S$=1.6 µm and 0.8 µm.

Schottky width to 0.8 µm, a significant decrease in the leakage current was observed, due to the increased shielding over the Schottky contact. However, this reduction also impacts 3rd quadrant conduction and requires further optimization of Schottky width and process conditions to balance leakage performance with conduction efficiency.

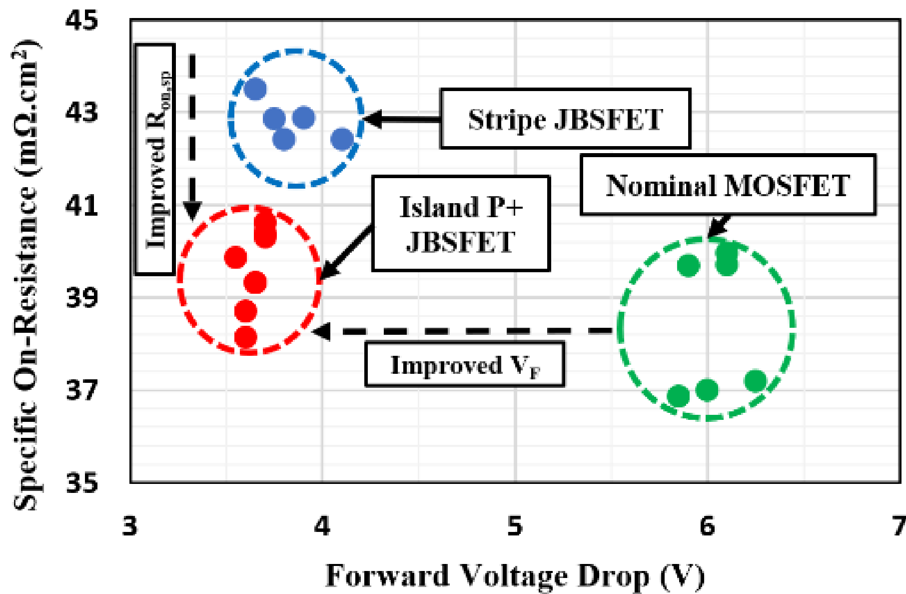


**Fig. 7.** The trade-off between specific on-resistance ($R_{on,sp}$) and forward voltage drop ($V_F$) was analyzed for the Nominal MOSFET, Stripe, and Island P+ JBSFETs, with forward voltage drop extracted at $V_{gs}$ = 0V and $I_{ds}$ = 0.5 A.

Fig. 7 summarizes the trade-off between specific on-resistance ($R_{on,sp}$) and forward voltage drop ($V_F$) for the nominal MOSFET, Stripe JBSFET, and Island P+ JBSFET. The Stripe JBSFET structure demonstrates improved 3rd quadrant performance but suffers from the highest $R_{on,sp}$, and leakage current. In contrast, the Island P+ design achieves the lower $R_{on,sp}$ than the Stripe structure, which offers almost the same $R_{on,sp}$ as the nominal MOSFET. The superior 3rd quadrant performance of the Island P+ structure is due to the design innovation that achieves a smaller cell pitch. Despite a slightly larger cell pitch than the MOSFET, the Island P+ JBSFET demonstrates well-balanced performance in forward conduction, 3rd quadrant behavior, and leakage current, underscoring its strong potential as a next-generation high-voltage, reliable power device.

**Summary**

This work compared 6.5 kV-rated 4H-SiC JBSFET architectures with a nominal MOSFET in terms of forward conduction, third-quadrant behavior, and blocking capability. The Stripe JBSFET improved third-quadrant conduction but suffered from the highest $R_{on,sp}$, leakage current, and cell pitch. In contrast, the Island P+ JBSFET achieved nearly identical $R_{on,sp}$ to the MOSFET, superior third-quadrant performance, and a high breakdown voltage of 8.3 kV. Reducing Schottky width to 0.8 µm further suppressed leakage, though at the expense of third-quadrant conduction, emphasizing the need for design trade-offs. Overall, the Island P+ JBSFET offers the best balance of conduction efficiency, leakage suppression, and blocking robustness, highlighting its promise as a reliable high-voltage 4H-SiC power device. Future work will focus on optimizing Schottky width and process conditions, scaling to higher voltage ratings, and validating long-term reliability under dynamic switching stress.

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