Key Engineering Materials
ISSN: 1662-9795, Vol. 1055, pp 29-36
doi:10.4028/p-JFK9oG

Submitted: 2025-09-25
Revised: 2025-12-28
Accepted: 2026-01-31
Online: 2026-05-19

Demonstration of Integrated 3.3kV 4H-SiC Bidirectional Conventional DMOSFETs at Cryogenic Temperatures

Zhaowen He[a*], Giorgian Borca-Tasciuc[b] and T. Paul Chow[c]

Rensselaer Polytechnical Institute, Troy, New York 12180, U.S.A

[a]hez5@rpi.edu, [b]borcag2@rpi.edu, [c]chowt@rpi.edu

Keywords: High Voltage, 4H-SiC, Power MOSFET, Bidirectional, Cryogenic.

Abstract. We have demonstrated an integrated 3.3 kV 4H-SiC vertical planar bidirectional (BD) conventional (Conv) power DMOSFET in common-drain (CD) configuration using two commercially available power DMOSFET dies and study its operation down to 77 K (-196 °C) to evaluate its cryogenic static and switching performance. The BD conduction and blocking are achieved down to 77 K. The measured specific on-resistance ($R_{ON,sp}$) of the BD MOSFET at room temperature (RT) is 26 mΩ-cm^2, approximately twice that of the unidirectional device. It increases by 54% when cooled to 77 K due to a substantial increase in channel and possibly JFET on-resistance components. In addition, the extracted specific switching losses ($E_{ON,sp}$ and $E_{OFF,sp}$) increases by 33% (13%) at 195K (–77 °C) and by 83% (88%) at 77 K, relative to their RT values. These increases are primarily attributed to the substantial rise in $R_{ON,sp}$ at 77 K. As a result, the implemented BD Conv DMOSFET exhibits degradation in both on-state and switching performance under cryogenic operation, driven mainly by the significant increase in channel and JFET resistance components.

Introduction

Cryogenic-capable bidirectional (BD) AC-to-AC power switches are essential for extraterrestrial space missions as well as for superconducting and quantum computing applications. Also, these power switches enable more compact systems and improved integrations, critical for applications where mass, volume, and thermal management constraints are stringent. Compared to the Si counterparts, 4H-SiC BD power DMOSFETs may be a good candidate for such applications owing to the wide bandgap of 3.26 eV, high critical electric field, and superior thermal conductivity.

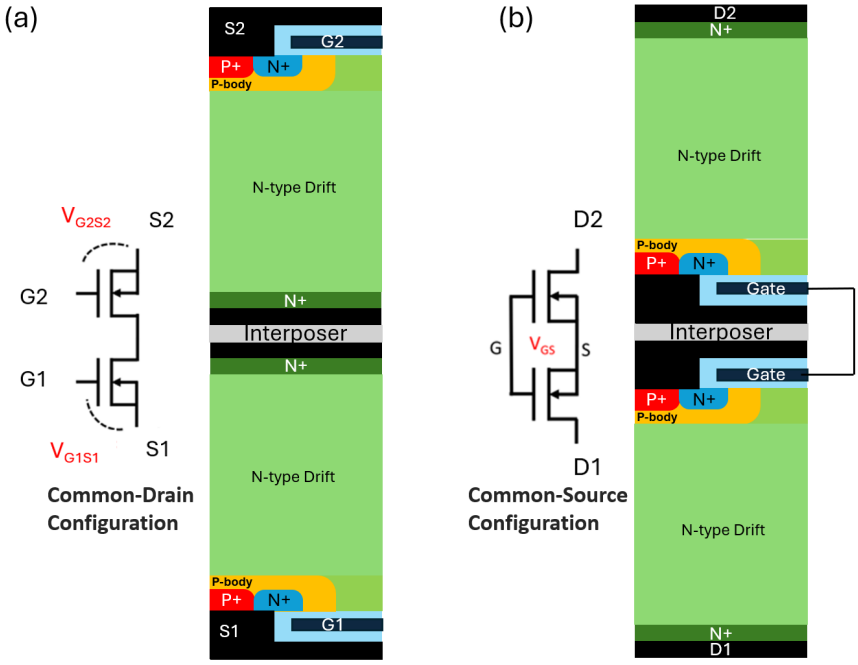

Fig. 1. Half-cell schematic cross-sections of vertical BD Conv DMOSFETs in (a) Common-drain (CD) configuration. (b) Common-source (CS) configurations.

However, several studies have reported anomalous temperature dependence [1-3] of the specific on-resistance ($R_{ON,sp}$) in unidirectional (UD) commercial 4H-SiC DMOSFETs at cryogenic temperatures, potentially degrading on-state performance. In addition, switching performance degradation at low temperatures has also been documented in the literature [4, 5]. These findings highlight the need to investigate and evaluate the cryogenic performance of high-voltage 4H-SiC BD conventional (Conv) DMOSFETs. In this paper, an integrated 3.3 kV 4H-SiC BD conventional (Conv) DMOSFET is demonstrated and studied down to 77 K (-196 °C) to evaluate its cryogenic static and switching performance.

Device Structure and Integration

The vertical BD power DMOSFET can be realized in either common-drain (CD) or common-source (CS) configurations, as illustrated in Fig. 1. In the CD configuration, the drains of the two planar DMOSFETs are tied together, while the gate of the high-side transistor is biased with a floating power supply to keep the channel on. In the CS configuration, the sources and gates of both devices are connected. The CD configuration simplifies packaging for discrete unidirectional (UD) power transistors but requires separate gate drivers, whereas the CS configuration reduces driver count to one at the expense of more packaging complexity.

Traditional BD functionality is often achieved through hybrid package implementations (Fig. 2) using discrete devices [6]. For example, an anti-series connection of two MOSFETs is used to achieve this, which doubles the on-resistance (R_{ON}) compared to a single device. To mitigate this increase, two identical anti-series pairs can be placed in parallel, but this quadruples the total chip area.

In addition, integrated BD DMOSFETs can be realized using a die-bonded approach (Fig. 2). In this method, two power device dies are bonded back-to-back in a BD package with a metallic interposer. As demonstrated in [7], two 1.2-kV 4H-SiC Conv DMOSFETs in a CD configuration achieve the same chip area as a UD device. This die-bonded approach retains the simplicity of hybrid packaging while enabling a more compact footprint for power module integration.

Monolithic implementations, often in CD configurations, further reduce device count and bond-wire connections. In a true monolithic BD Conv DMOSFET, a shared drift region with dual gates enables bidirectional blocking, cutting R_{ON} roughly in half for high-voltage (>3 kV) applications where drift resistance dominates. In 4H-SiC, this implementation was demonstrated in [8] with the BiDFET device (Fig. 2), which achieves a blocking voltage of ±1200 V. The BiDFET consists of two 1.2-kV vertical Conv DMOSFETs in a common-drain configuration, each integrated with a JBS diode. Two drift regions are employed—one for each blocking direction—connected through an N+ substrate and backside drain metallization. While this design benefits from full on-chip integration, it incurs penalties of doubled chip area and doubled specific on-resistance due to the dual drift regions.

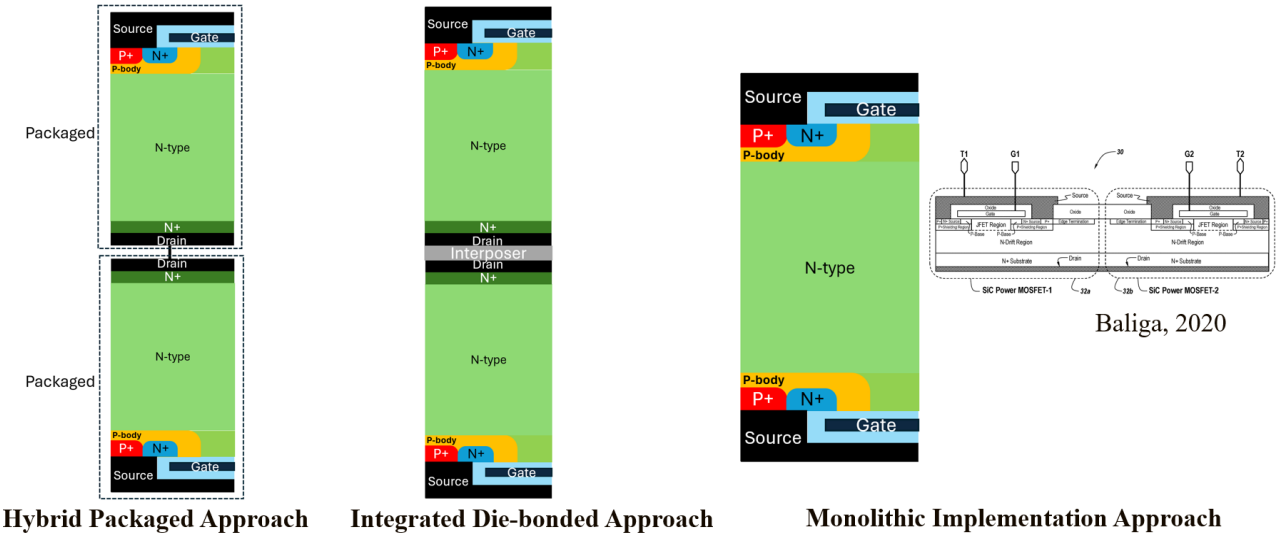

Fig. 2. Three approaches for implementing vertical BD Conv DMOSFETs in CD configurations.

On the other hand, Chowdhury *et al.* [9] demonstrated a compact, vertical implementation of monolithic BD 4H-SiC IGBT with shared drift region via the double-sided lithography processes on a free-standing 4H-SiC substrate [10]. The initial prototype devices experimentally achieved blocking voltages of up to 7 kV. This work presents a promising approach for the vertical monolithic integration of 4H-SiC BD DMOSFETs. However, such implementation requires double-sided processes, which increases complexity and cost in fabrication and chip manufacturing.

In this work, the 3.3 kV 4H-SiC BD Conv DMOSFET prototype is vertically implemented in the CD configuration via integrated die-bonded approach using two commercially available Wolfspeed (CPM3-3300-R050A) SiC Gen3 MOSFET dies, as schematically shown in Fig. 3(a). Fig. 3(b) shows the BD DMOSFET chip in a customed BD package. This BD chip is fabricated by joining the drain metal contacts of the two dies using a commercially available nanoparticle silver paste, followed by a 200 °C sintering process. The custom package is constructed by sandwiching the BD die between two through-hole G10 substrates, sealed with silicone for mechanical and environmental protection. A 30 µm Parylene layer and hard baked photoresist layer are used to passivate the exposed die sides, surfaces, and bonding wires.

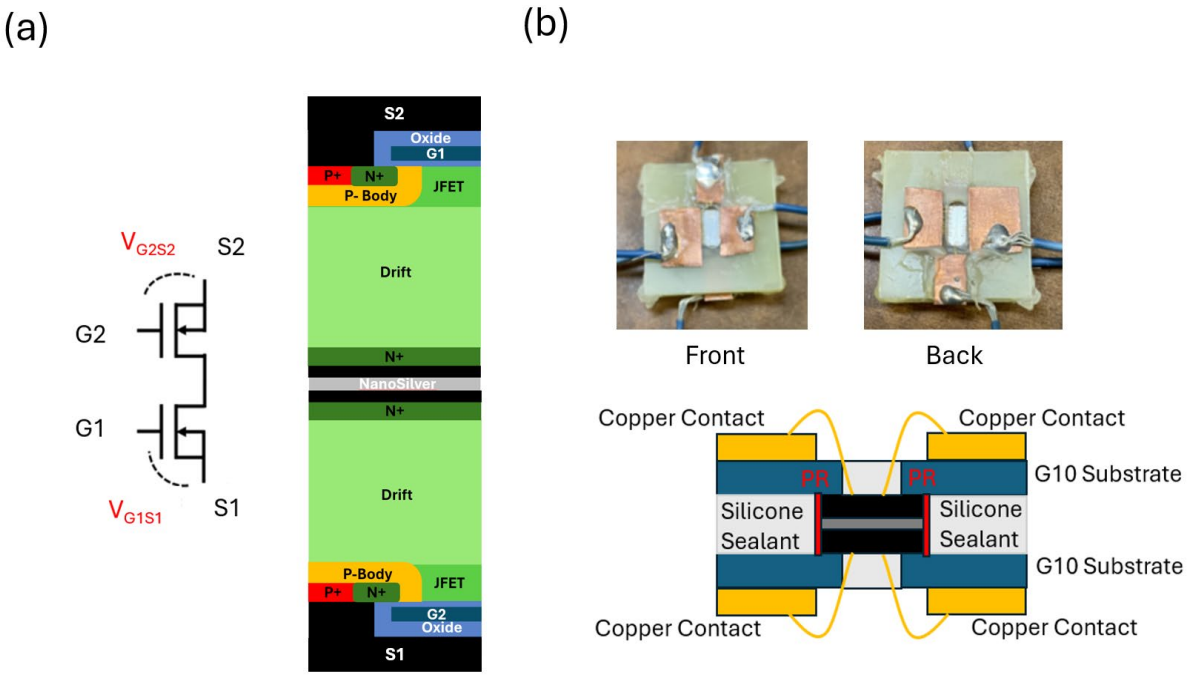

Fig. 3. (a) Circuit schematics and schematic cross-section of the implemented 3.3 kV 4H-SiC Conv BD DMOSFET in Common-drain configuration. (b) Photo and cross-section of the custom BD DMOSFET package.

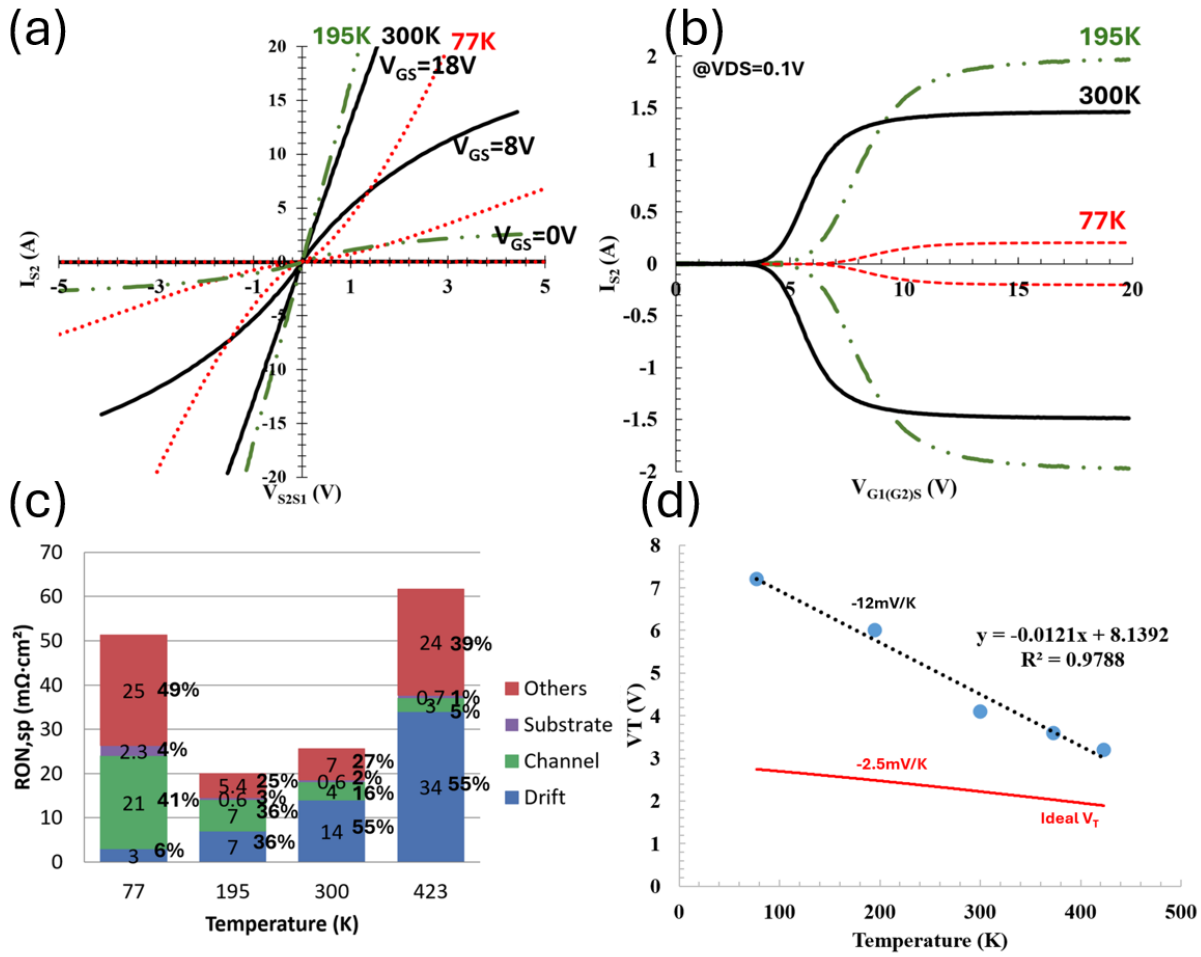

Fig. 4. Temperature-dependent on-state characteristics. (a) Output I–V curves measured at 77, 195, and 300 K for VGS = 0, 8, and 18 V. (b) Transfer characteristics at VDS = 0.1 V over the same temperature range. (c) Estimated specific on-resistance ($R_{ON,sp}$) components—drift, channel, substrate, and others—extracted at 77, 195, 300, and 423 K. (d) Threshold voltage (V_T) as a function of temperature, exhibiting a linear dependence with a temperature coefficient of –12 mV/K.

Results and Analysis

On-state characteristics were measured using a Tektronix 370A curve tracer. An Agilent B1505A power device analyzer equipped with an N1268A ultra-high-voltage expander was used to characterize BV_{DSS}.

Inductive load switching is performed using a customized inductive load (12 mH) double pulse test (DPT) setup (Fig.6) at 200 V and 5 A with a 100 Ω gate resistance (R_G). A 1.2-kV Rohm SiC commercial Schottky diode (SCS120KGC) was used as the flyback diode to suppress reverse recovery effects. The power supply was set to 200 V, and the gate pulse width was adjusted to achieve a switching current of 5 A. Because the CD configuration requires independent gate drivers, only one device was actively switched, while the other device's gate was held at 18 V.

Fig.4(a) shows the output I-V characteristics of our prototype BD MOSFET at 77 (-196 °C), 195 (-77 °C), and 300 K (27 °C). The output I-Vs show symmetric BD conduction at all three testing temperatures. Extracted $R_{ON,sp}$ of the BD device (V_{GS}=18 V) at room temperature (RT) is 26 mΩ-cm^2, which is doubled of the $R_{ON,sp}$ of the UD device (13 mΩ-cm^2). Measured $R_{ON,sp}$ increased by 54% at 77 K and decreased by 23% at 195 K, showing a "bathtub-shaped" temperature dependence. This is consistent with trends previously reported for UD commercial conventional 4H-SiC DMOSFETs [1,2]. Estimated major resistance components at 77, 195, 300, and 423 K (150 °C) are plotted in Fig. 4(c). The drift-region resistance component increases monotonically with temperature. Although significant carrier freeze-out occurs at 77 K, the drift resistance still decreases markedly to

21% of its room-temperature value, owing to approximately 20 times increase in bulk electron mobility, as estimated using the temperature-dependent model reported in [16]. On the other hand, estimated channel resistance component exhibits a well-known negative temperature coefficient due to mobility degradation from high interface trapping and increase in threshold voltage at cryogenic temperatures. Interestingly, estimated other lumped resistance components show a non-linear temperature dependence from 77 to 423 K. This non-linear temperature dependence could originate from non-linearity of JFET resistance component from the DMOS structure. According to a reported study of 4H-SiC JFET performance at cryogenic and high temperature [17], the JFET resistance increases with temperature above 200 K, primarily due to the temperature dependence of bulk mobility. Under cryogenic conditions, both [3] and [17] have shown that a shift in the JFET threshold voltage from channel pinch-off, along with carrier freeze-out in the quasi-neutral region, are responsible for the substantial rise in JFET resistance. Due to such reasons, this increase in JFET resistance is predicted to be more pronounced for smaller pitch planar DMOSFETs at 77 K [3]. Therefore, channel and JFET resistance components are likely to dominate in this device at cryogenic temperatures.

The transfer I-V characteristics at V_{DS}=0.1 V are shown in Fig.4(b). Extracted threshold voltages are 7.2, 6, and 4.1 V at 77, 195, and 300 K, respectively, exhibiting a monotonic decrease with temperature. To assess the temperature dependence, threshold voltages were extracted up to 423 K. A linear fit across the 77–423 K range yields a negative slope of –12 mV/K, consistent with previously reported trends [2]. The ideal threshold voltages from 77 to 423 K, shown as the red curve in Fig. 4(d), were calculated assuming a fixed oxide charge density of 2e12 cm^{-2}, yielding a slope of –2.5 mV/K. The deviation between measured and ideal values becomes more pronounced at lower temperatures, suggesting that the discrepancy could originate from increased filled interface charge (Q_{it}) at SiO_2/SiC interface at lower temperatures.

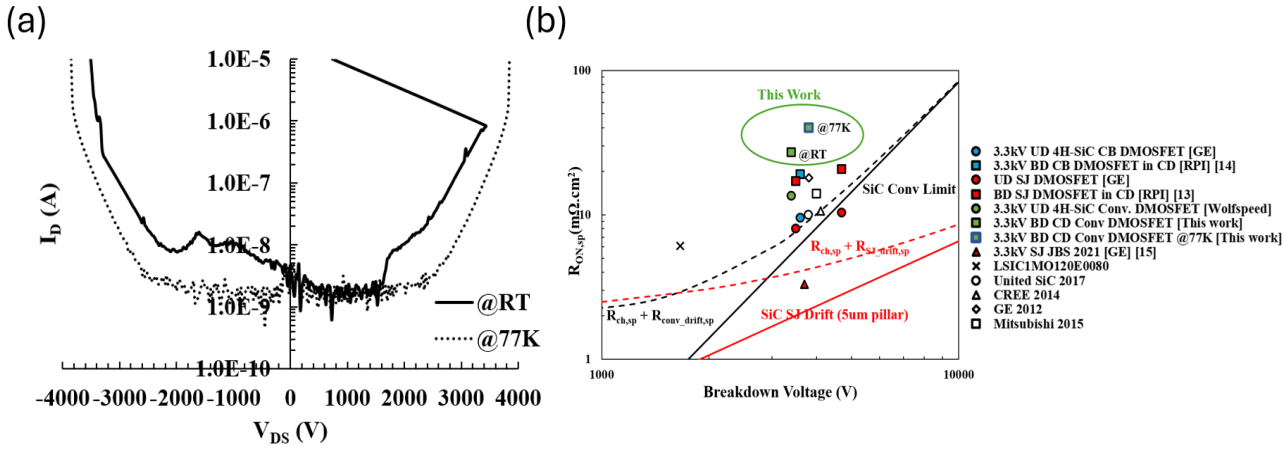

Fig. 5. (a) Blocking IVs at 77 and 300 K. (b) $R_{ON,sp}$ vs. BV trade-off comparison of the implemented 3.3-kV 4H-SiC BD Conv DMOSFET at room temperature (RT) and 77 K. For reference, the authors' prior works on high-voltage 4H-SiC BD superjunction (SJ) [13] and charge-balanced (CB) [14] devices are included, demonstrating improved trade-offs compared to the Conv BD device reported in this work. Commercial high-voltage 4H-SiC UD DMOSFETs are also shown for benchmarking.

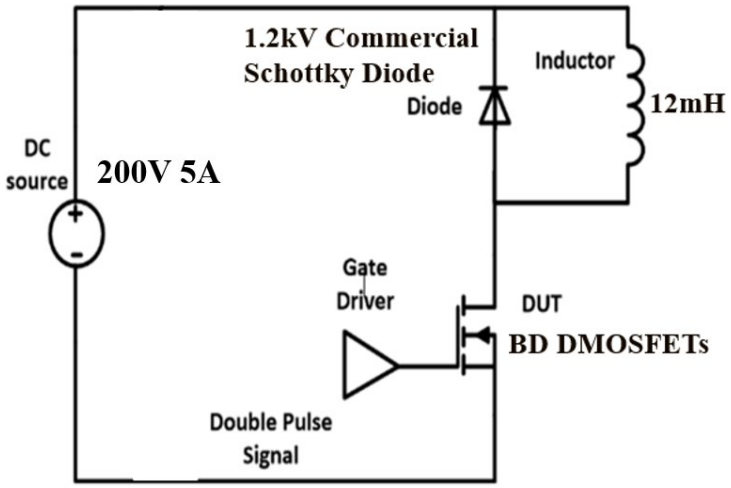

Fig. 6. Customized inductive load double pulse test (DPT) setup for switching characterization.

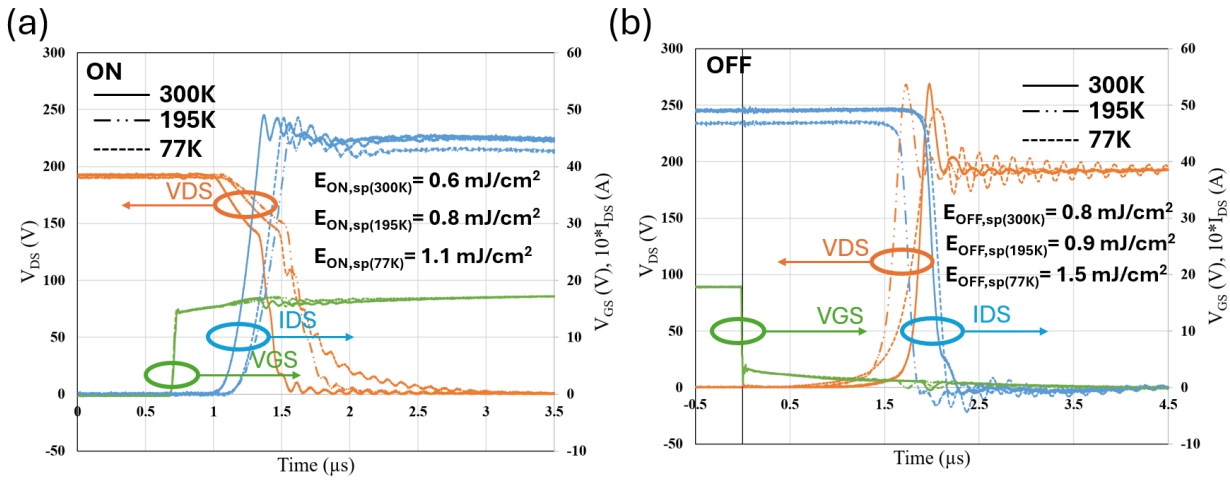

Fig. 7. Switching waveforms at 77, 195, and 300 K of the implemented 3.3 kV BD Conv DMOSFET (a) Turn-on waveforms. (b) Turn-off waveforms.

The blocking I-V characteristics at RT and 77 K are shown in Fig. 5(a). Over 3.4 kV and 3.8 kV BD blocking is achieved at RT and 77K, respectively. An anomalous increase in BV_{DSS} is observed at 77 K. In both the literature [11] and our prior work [12] on commercial packaged UD 4H-SiC DMOSFETs, the BV_{DSS} has consistently shown a positive temperature coefficient, as expected when breakdown is limited by the intrinsic avalanche mechanism. This behavior arises from the reduced ionization path length at elevated temperatures. Hence, better termination performance could be one of the possible explanations for this anomalous increase in BV_{DSS} at 77 K.

At 77 K, $R_{ON,sp}$ increases by 54% while BV_{DSS} improves by only ~10%, resulting in a degraded $R_{ON,sp}$ vs. BV_{DSS} trade-off for this device (Fig. 5(b)). Consequently, static performance of the testing device is expected to deteriorate under cryogenic operation.

Fig. 7 compares the switching performance of the implemented 3.3kV BD Conv DMOSFET at 77, 195, and 300K. During turn-on (Fig.7(a)), the specific energy loss ($E_{ON,sp}$) increases from 0.6 mJ/cm² at 300 K to 1.1 mJ/cm² at 77 K, showing an 83% increase in turn-on losses at cryogenic temperatures. In addition, the turn-off waveforms (Fig. 7(b)) also show an increase in energy loss, with $E_{OFF,sp}$ rising from 0.8 mJ/cm² at 300 K to 1.5 mJ/cm² at 77 K, exhibiting an 88% increase. This increase in both turn-on and turn-off switching energy is attributed to significant increase of $R_{ON,sp}$ at 77K. Hence, V_{DS} waveforms at 77 K during turn-on and turn-off exhibiting a noticeable slow tail and head while I_{DS} is still high. Overall, the results demonstrate that while BD Conv DMOSFETs maintain functional

switching operation across the full temperature range, both turn-on and turn-off losses increase significantly at cryogenic temperatures, leading to a degradation in dynamic performance.

Summary

An integrated 3.3 kV 4H-SiC vertical BD Conv DMOSFET is successfully demonstrated to maintain bidirectional conduction and blocking capability down to cryogenic temperatures. At 77 K, the channel resistance and possibly JFET resistance from DMOS structure becomes the dominant component, primarily due to inversion electron mobility degradation caused by increased Coulombic scattering. Consistent with UD 4H-SiC DMOSFETs, the implemented BD Conv DMOSFET exhibits degradation in both on-state and switching performance at 77 K, primarily due to the significant increase in channel and JFET on-resistance components.

Acknowledgement

The authors would like to thank Wolfspeed, Inc. for providing the 3.3kV 4H-SiC commercial Conv power DMOSFET dies used in the bidirectional implementation of this work.

References

[1] K. Hong *et al.*, “Experimental investigations into temperature and current dependent on-state resistance behaviors of 1.2 kV SiC MOSFETs”, *IEEE Journal of the Electron Devices Society*, no.7, pp. 925-930, 2019.

[2] S. Chen *et al.*, “Cryogenic and high-temperature performance of 4H-SiC power MOSFETs”, *28th Annual IEEE APEC*, 2013, pp. 1277-1283.

[3] S. Chowdhury *et al.*, “Comparative evaluation of commercial 1200 V SiC power MOSFETs using diagnostic IV characterization at cryogenic temperatures”, *Mat. Sci. Forum*, vol 897, pp. 545-548, 2017.

[4] Y. Wei *et al.*, “Cryogenic performances comparisons among Si MOSFET, SiC MOSFET, cascode GaN, and GaN devices,” *IOP Conference Series: Materials Science and Engineering*, vol. 1241, pp. 012042, 2022.

[5] K. Tian *et al*., "Comprehensive characterization of the 4H-SiC planar and trench gate MOSFETs from cryogenic to high temperature," *IEEE Transactions on Electron Devices*, vol. 66, no. 10, pp. 4279-4286, Oct. 2019.

[6] J. Huber and J. W. Kolar**,** “Monolithic bidirectional power transistors,” *IEEE Power Electronics Magazine*, vol. 10, no. 1, pp. 28–38, Mar. 2023.

[7] C. Hitchcock and T. P. Chow, “Common-drain bidirectional 1200 V SiC MOSFETs,” *Materials Science Forum*, vol. 1004, pp. 882–888, 2020.

[8] K. Han *et al.*, “Monolithic 4-terminal 1.2 kV/20 A 4H-SiC bi-directional field effect transistor (BiDFET) with integrated JBS diodes,” *Proc. 32nd Int. Symp. Power Semiconductor Devices and ICs (ISPSD)*, Vienna, Austria, Sept. 2020, pp. 242–245.

[9] S. Chowdhury *et al.*, “Operating principles, design considerations, and experimental characteristics of high-voltage 4H-SiC bidirectional IGBTs,” *IEEE Transactions on Electron Devices*, vol. 64, no. 3, pp. 888–896, Mar. 2017.

[10] S. Chowdhury *et al.***,** “Characteristics of 4H-SiC P-i-N diodes on lightly doped free-standing substrates,” *Proc. 27th Int. Symp. Power Semiconductor Devices and ICs (ISPSD)*, May 2015, pp. 353–356.

[11] P. Steinmann *et al.*, “Temperature dependence of avalanche breakdown in 4H-SiC devices,” *Journal of Applied Physics*, vol. 133, no. 23, pp. 235705, 2023.

[12] Z. He *et al.*, "Comparative performance evaluation and analysis of high voltage superjunction, charge-balanced, and conventional 4H-SiC DMOSFETs at cryogenic and high temperatures," *Proc. 37th Int. Symp. Power Semiconductor Devices and ICs (ISPSD)*, 2025.

[13] Z. He *et al.*, "Experimental demonstration and analysis of 4.5 kV bidirectional superjunction power DMOSFETs in 4H-SiC," *Proc. 37th Int. Symp. Power Semiconductor Devices and ICs (ISPSD)*, 2025.

[14] Z. He et al., "Experimental comparative demonstrations and analysis of 3.3 kV 4H-SiC common-drain and common-source bidirectional charge-balanced power DMOSFETs switching," *Proc. 36th Int. Symp. Power Semiconductor Devices and ICs (ISPSD)*, 2024, pp. 140-143.

[15] R. Ghandi *et al.*, "Scalable ultrahigh voltage SiC superjunction device technologies for power electronics applications," *Proc. IEEE Int. Electron Devices Meeting (IEDM)*, San Francisco, CA, USA, pp. 9-1.

[16] S. Kagamihara *et al.*, "Parameters required to simulate electric characteristics of SiC devices for n-type 4H–SiC," *J. Appl. Phys.*, vol. 96, no. 23, pp. 5601-5606, 2004.

[17] Cheng *et al.*, "Cryogenic and high temperature performance of 4H-SiC vertical junction field effect transistors (VJFETs) for space applications," *Proc. 17th Int. Symp. Power Semiconductor Devices and ICs (ISPSD)*, Santa Barbara, CA, USA, 2005, pp. 231-234.