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Comparative Study of 1.2kV 4H-SiC Bi-Directional MOSFET (BiD-MOS) Design Approaches: 2-Chip vs Monolithic Integration

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Abstract. Several 1.2kV 4H-SiC Bi-Directional MOSFETs (BiD-MOS) design approaches were successfully fabricated and evaluated based on their electrical characteristics. Both monolithic integration design approaches exhibited negligible differences in conduction, blocking, and switching characteristics when compared to their 2-Chip counterpart. However, during the short-circuit withstand time testing, severe gate oscillations were observed in the 2-Chip design, which was not an issue present in either monolithic configuration. As a result of its robust electrical behavior, monolithic integration emerges as a promising design approach for developing efficient and reliable Bi-Directional Switches.

Introduction

With the global shift toward electrification, the demand for highly efficient AC-AC and AC-DC converters capable of conducting current and blocking voltage in both forward and reverse directions is rapidly increasing. Conventional power conversion systems (PCS) that employ Bi-Directional switches typically rely on multiple MOSFETs and diode components, which introduce substantial switching losses and increase overall system complexity [1]. Therefore, implementing a single Bi-Directional switch offers the potential to simplify the system architecture, reduce the total number of components, and improve both switching efficiency and overall device performance, making it an attractive solution for modern power electronics applications. In line with this approach, several demonstrations of 4H-SiC Bi-Directional Field Effect Transistors (BiDFETs) as monolithically integrated, single-chip devices have been reported [2,3]. However, when using vertical MOSFET technology, the larger chip area required for monolithic integration raises concerns about yield loss and manufacturing efficiency, motivating the exploration of more area-efficient alternatives [4]. While these designs offer promising reductions in chip area even when considering yield losses due to chip size [5], their electrical performance remains insufficiently characterized, leaving questions about trade-offs between integration, efficiency, and reliability. This study investigates the electrical performance of various Bi-Directional MOSFET (BiD-MOS) designs, providing a comprehensive assessment of the feasibility and advantages of monolithic integration for high-performance Bi-Directional switching applications.

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Device Design and Fabrication

Fig. 1 shows the top and cross-sectional views of three BiD-MOS design approaches evaluated in this study. These include: (1) a 2-Chip solution using two discrete MOSFETs, (2) a monolithic design with two MOSFETs side-by-side on a single chip and matching the area of the 2-Chip solution, and (3) a monolithic design featuring a shared channel stop integrated within the edge termination to reduce die area [4,5]. These designs are referred to as the 2-Chip, Mono, and Mono SN+ BiD-MOS, respectively. The monolithic designs, fabricated as single chips on the wafer, are inherently restricted to the Common-Drain configuration. In contrast, the 2-Chip solution, being composed of separate device components, can be implemented in either Common-Source or Common-Drain form. To ensure a consistent basis for comparison, the 2-Chip solution was also evaluated in the Common-Drain configuration for this study.

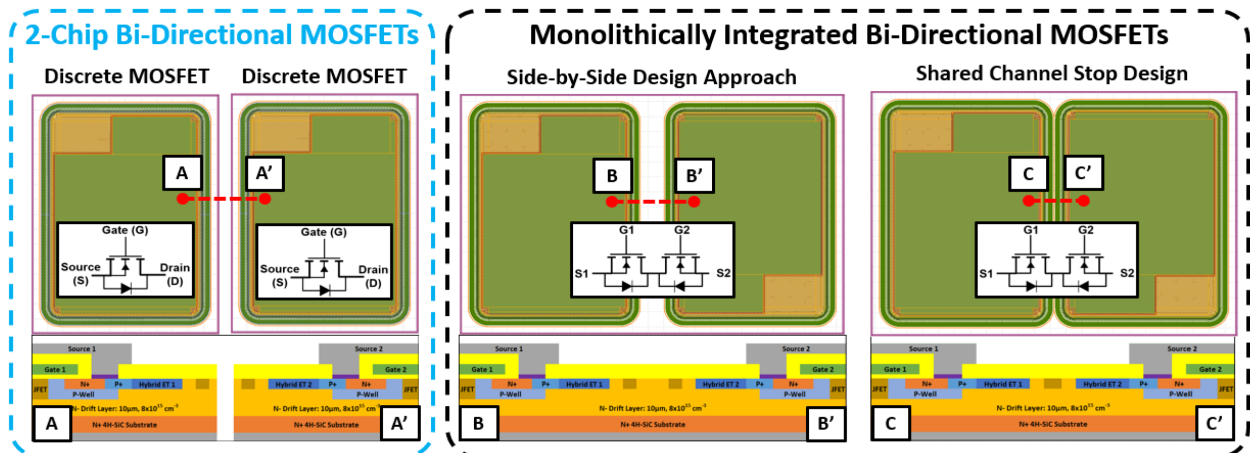

Fig. 1. Top layout and simplified cross-sectional views of the three Bi-Directional MOSFET (BiD-MOS) design approaches examined within this study. The 2-Chip BiD-MOS approach utilizes two individual MOSFET components, whereas the Monolithically integrated BiD-MOS designs employ a single chip solution.

In addition to all devices adopting the Common-Drain configuration, the individual MOSFETs used in the monolithic BiD-MOS and the discrete MOSFET components shared the same design and layout. To maximize device performance, 2D electrical simulations were conducted to optimize both the active and edge termination regions. For the active area cell design, the channel length and JFET width were set to 0.5µm and 1µm, respectively. The subsequent active area of each MOSFET component was designed to be $0.44mm^2$ to achieve the desired current rating. To achieve the 1.2 kV voltage rating, a Hybrid-JTE edge termination was employed to ensure reliable blocking behavior and low leakage current for all devices [6]. In the Mono SN+ design, the channel stop at the end of the termination was shared by both MOSFETs along their common side, thereby reducing die area by enabling the individual MOSFET components to be placed closer together.

The MOSFETs used in the 2-Chip design, along with all monolithic BiD-MOS designs, were fabricated on the same wafer at X-FAB, USA, under identical process conditions. To achieve the targeted 1.2 kV voltage rating, a 10 µm-thick N-type epitaxial drift layer with a doping concentration of $8x10^{15}$ cm^{-3} was grown on top of a heavily doped, N+ 4H-SiC substrate. Nitrogen and aluminum ion implantation were employed to form the JFET/N^+ and P-Well/P^+/JTE regions, respectively, followed by a 10-minute activation anneal at 1650 °C. After the implantation steps, a 50 nm-thick gate oxide was then grown, followed by the deposition of polysilicon. Both layers were then patterned and etched to form the gate regions. This was followed by deposition and patterning of an interlayer dielectric (ILD), enabling the sequential formation of ohmic and gate contacts. A Ti/TiN/AlCu metal stack was subsequently deposited to establish ohmic contacts with the 4H-SiC substrate and the polysilicon gate. The metal stack was then patterned to form the gate and source pads within each device.

To complete the fabrication process, a thick SiN and polyimide layer was deposited and patterned to provide surface passivation. After fabrication, both the 2-Chip and monolithic BiD-MOS designs were packaged in a SOT-227 module for evaluation, as shown in Fig. 2.

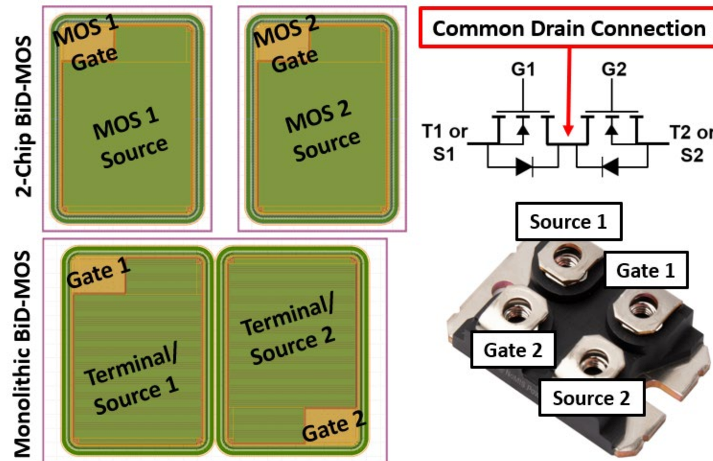

Fig. 2. Top views of the 2-Chip and Monolithic BiD-MOS design approaches (Top and bottom left, respectively) with the key device regions labeled. Due to the shared substrate limitations of the monolithic designs, both approaches utilize a common-drain configuration and are packaged inside a SOT-227 package (right) with the assistance of NoMIS Power.

Results and Discussion

The measured output of each BiD-MOS design approach in both the forward (S2 → S1) and reverse (S2 ← S1) directions are shown in Fig. 3. For these measurements, the high-side gate ($V_{G2–S2}$ for the forward direction and $V_{G1–S1}$ for the reverse direction) was set to either 20 V or –5 V, while the opposite gate was gradually increased to allow current conduction either through both channel regions or through the body diode of the first MOSFET and the channel region of the second MOSFET. Regardless of the BiD-MOS conduction mode, each design approach exhibited nearly identical output characteristics. When both MOSFET channels were in the on-state ($V_{G2–S2}$=$V_{G1–S1}$=20 V), the average R_{on} values were 169.8 mΩ, 169.1 mΩ, and 166.1 mΩ for the 2-Chip, Mono, and Mono SN+ design approaches, respectively. Although minimal, it is important to note that the Mono design, and to a larger extent the Mono SN+ design, resulted in a slightly lower R_{on} when compared to the 2-Chip solution counterpart.

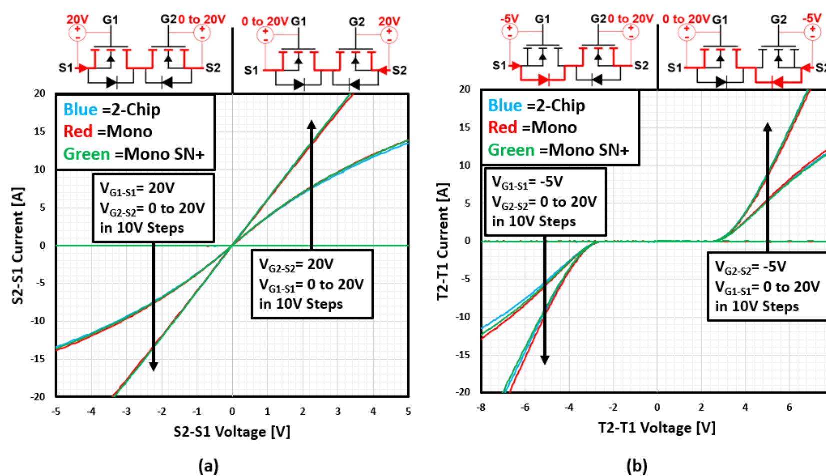

Fig. 3. Measured output characteristics for each BiD-MOS design approach in both the forward (S2→S1) and reverse directions (S2←S1), with a gate bias of V_{G2-S2}=20 V and V_{G1-S1}=20 V applied for the forward and reverse directions, respectively (a), and with a gate bias of V_{G2-S2}= -5 V and V_{G1-S1}= -5 V applied for the forward and reverse directions, respectively (b). Minimal differences between each BiD-MOS design are observed for each conduction mode of operation.

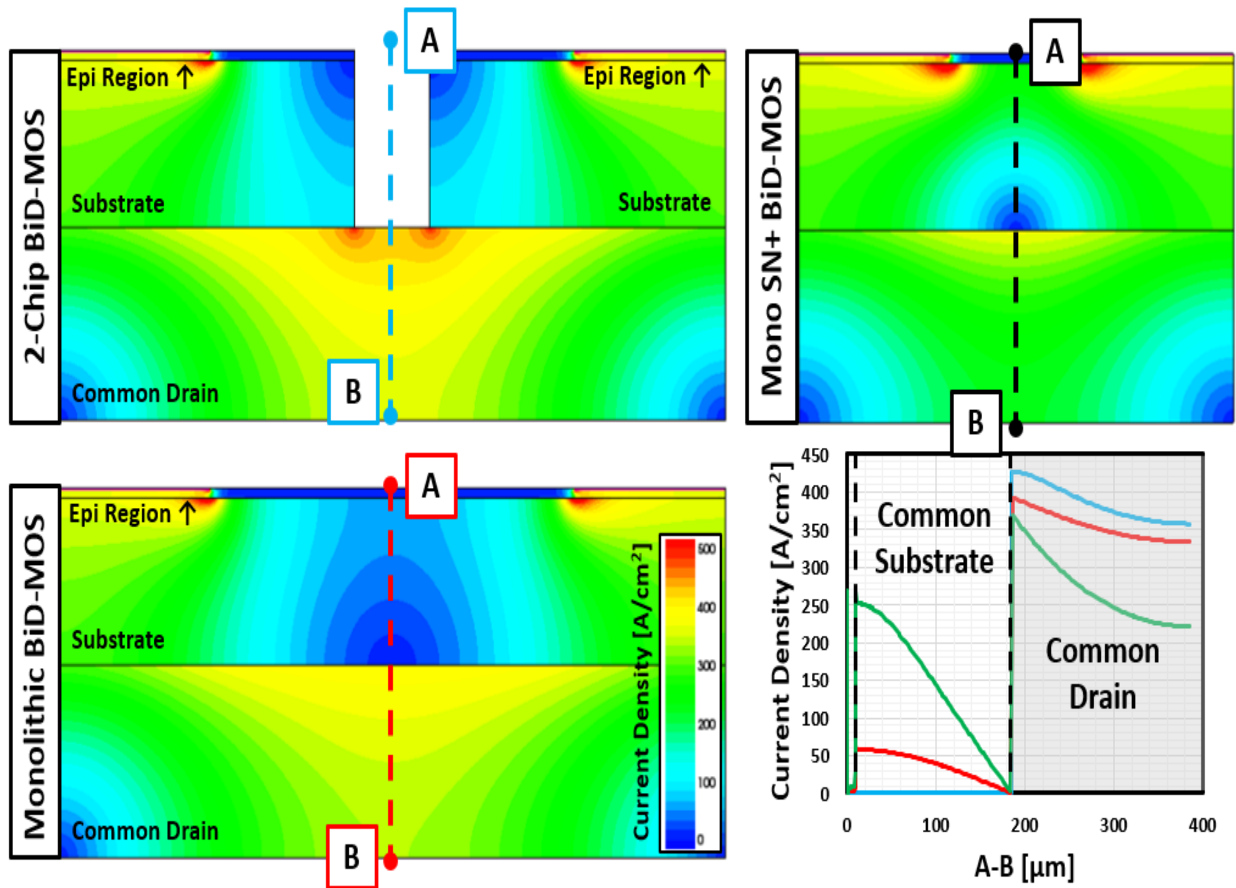

Fig. 4. Simulated current density of the 2-Chip, Mono, and Mono SN+ BiD-MOS design approaches. Both monolithic designs demonstrate conduction through the common epitaxial drift and substrate layers, subsequently increasing the overall current flow.

To further examine the conduction behavior of the various BiD-MOS design approaches, simplified 2D electrical simulations were performed to highlight potential trends between the structures, as shown in Fig. 4. These simulations reveal that current conduction occurs primarily through the common drain of each BiD-MOS. However, for the Mono design, and more prominently for the Mono SN+ design, current conduction also occurs through the common epitaxial drift and substrate layers. Specifically, the current conduction through the epitaxial drift layer, substrate, and common drain is 0.74%, 9.15%, and 90.11% for the Mono BiD-MOS, and 3.66%, 32.22%, and 64.12% for the Mono SN+ BiD-MOS, respectively, for these simulations. In contrast, due to the layout of the 2-Chip design, current conduction is restricted exclusively to the common drain. The presence of additional conduction pathways in the monolithic designs helps reduce current crowding and slightly improve conduction behavior, resulting in a 1.6% improvement between the Mono and 2-Chip designs. Furthermore, by bringing the MOSFET components closer together in the Mono SN+ design, the conduction pathway is shortened, and overall resistance is reduced, leading to a 7.8% improvement over the 2-Chip design.

The measured blocking characteristics of each BiD-MOS design in both the forward (S2 → S1) and reverse (S2 ← S1) directions are shown in Fig. 5. For these measurements, both the high- and low-side gates of the BiD-MOS were set to 0 V. All three BiD-MOS designs exhibited similar blocking behavior, with a breakdown voltage of approximately 1620 V and a leakage current below 1nA at $V_{S2\text{-}S1}$=1200 V. As illustrated in Fig. 6, the blocking capability of each BiD-MOS is determined by the edge termination structure of the low-side device, as this MOSFET operates in its forward-blocking mode. In contrast, the high-side device has no impact on blocking performance. Since all BiD-MOS designs employ the same edge termination, their blocking performance is nearly identical.

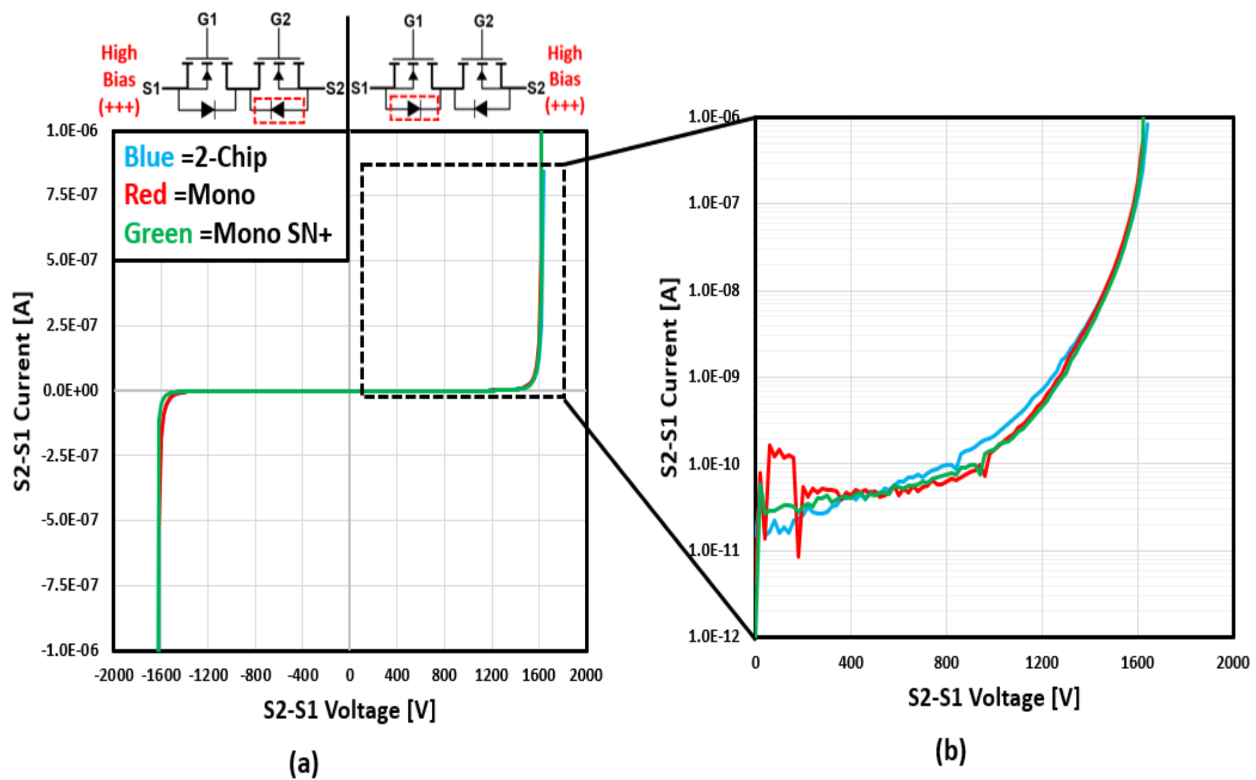

Fig. 5. Typical measured blocking characteristics of each BiD-MOS design approach in both the forward (S2→S1) and reverse directions (S2←S1) (a), along with the leakage current in the forward direction (b). Minimal differences between each BiD-MOS design approach are observed.

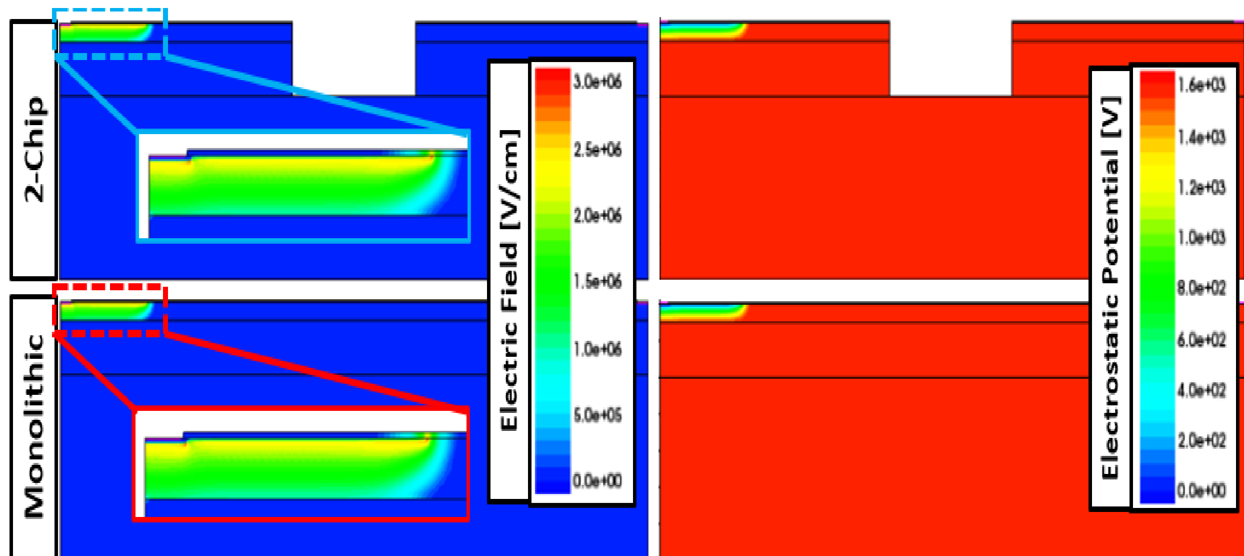

Fig. 6. Simulated electric field and electrostatic potential of the 2-Chip and Monolithic BiD-MOS design approaches during the blocking mode. In both cases, the blocking characteristics are governed by the edge termination of the low-side device, resulting in comparable blocking performance.

The switching characteristics of the various BiD-MOS designs were evaluated using a double-pulse test (DPT) setup, with the turn-on and turn-off waveforms shown in Fig. 7. For this analysis, the high-side gate (V_{G2-S2} for the forward direction and V_{G1-S1} for the reverse direction) was set to 20 V, and switching was performed on the low-side component. Similar to the conduction and blocking measurements, only minimal differences were observed among the design approaches, with the resulting turn-on, turn-off, and total switching losses measuring approximately 0.81 mJ, 0.69 mJ, and 1.50 mJ, respectively, for each design.

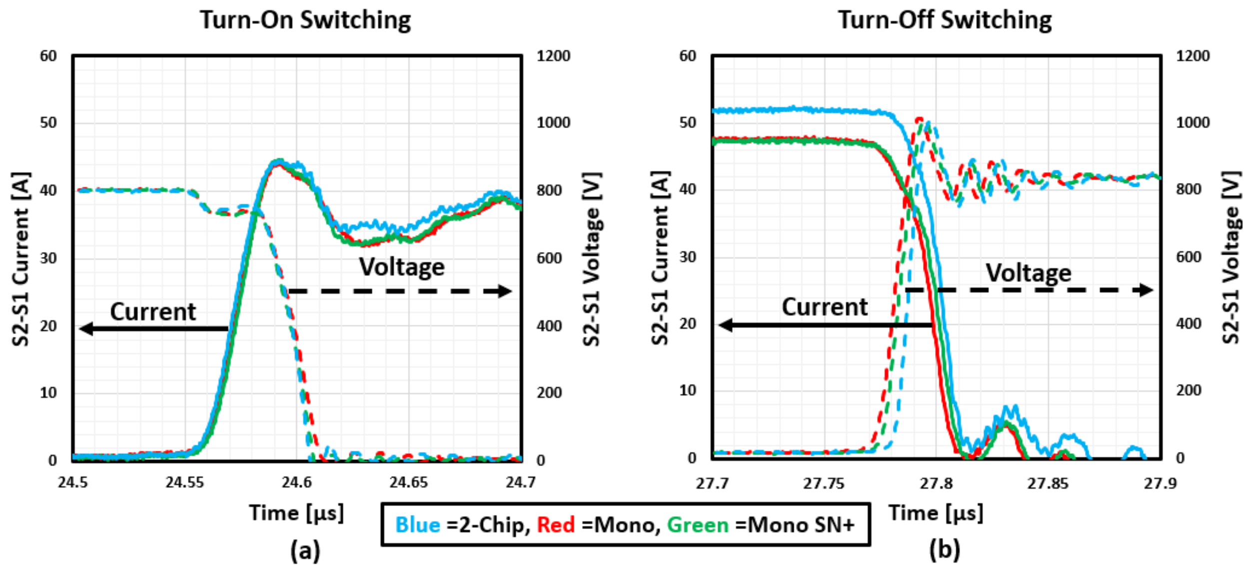

Fig. 7. Measured turn-on (a) and turn-off (b) switching waveforms for each BiD-MOS design approach using a double-pulse test (DPT) setup. During the measurements, $V_{G2–S2}$= 20V was applied, with the following parameters: gate resistance = 10Ω, on-state gate voltage $V_{G1–S1}$= 20V, off-state gate voltage $V_{G1–S1}$= –5V, switching current $I_{S2–S1}$= 50A, and blocking voltage $V_{S2–S1}$= 800V.

To further the evaluation of the various BiD-MOS design approaches, several Short Circuit Withstand Time (SCWT) tests were conducted. Unlike the previous analysis, a noticeable difference can be observed between the 2-Chip and monolithic design approaches, as seen in Fig. 8. Under modified test conditions of V_{S2-S1}=100 V, with a 2 µs pulse, the 2-Chip BiD-MOS exhibited significant oscillations in the gate turn-off waveforms, which were absent in both monolithic configurations. These oscillations were consistent for all 7 measured 2-Chip BiD-MOS samples. Since the gate could not be properly turned off, the resulting SCWT for the 2-Chip approach was unable to be fully determined. However, under typical SCWT evaluation conditions (i.e. V_{D2-S1}=800 V), the Mono and Mono SN+ designs demonstrated comparable SCWTs of 3.82 µs and 3.67 µs, respectively.

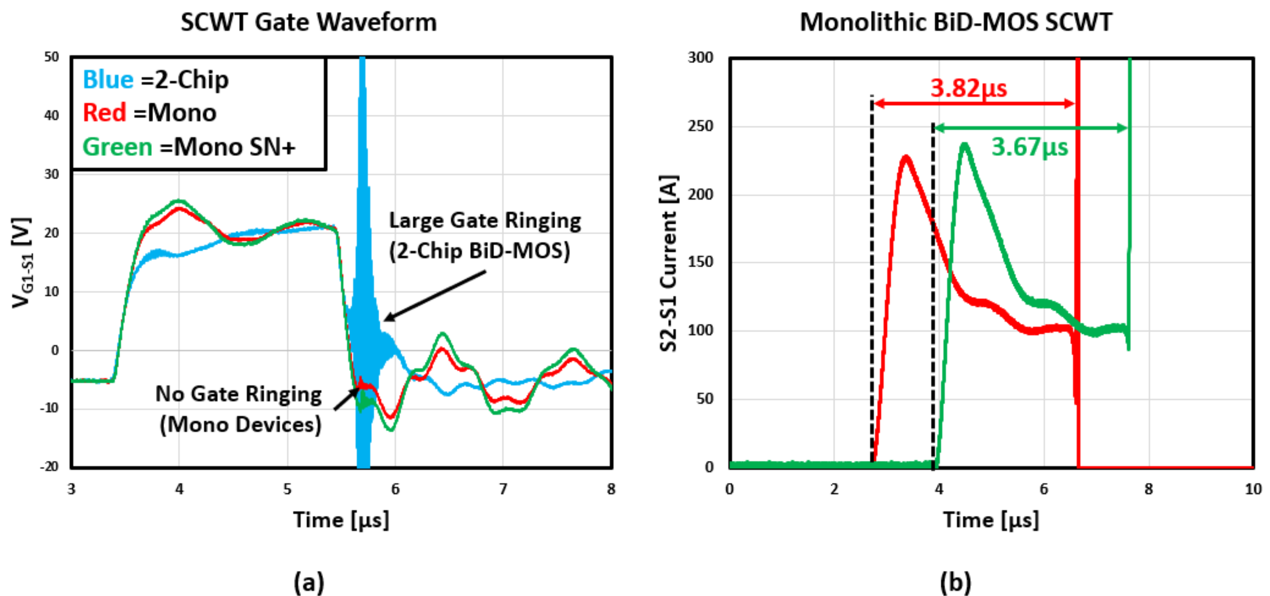

Fig. 8. V_{G1-S1} waveforms during the SCWT test in which V_{S2-S1}= 100 V, SWCT pulse= 2 µs, and V_{G2-S2}= 20 V were used (a), and typical SCWT test (i.e. V_{S2-S1}= 800 V, and V_{G2-S2}= 20 V) for both monolithic BiD-MOS designs (b). Large oscillations are seen within the V_{G1-S1} turn-off waveform for the 2-Chip approach that is not present in either of the monolithic designs.

The results of all measurements conducted for each BiD-MOS design are summarized in Table 1. In terms of conduction, blocking, and switching characteristics, the different approaches exhibited nearly identical performance. Under SCWT testing, however, the 2-Chip BiD-MOS showed pronounced gate oscillations that were not observed in the monolithic counterpart. This difference is hypothesized to arise from variations in parasitic inductance between the 2-Chip and monolithic designs, as parasitic inductance has been shown to negatively affect device SCWT [7,8]. However, further analysis is needed to confirm the root cause of these oscillations in the 2-Chip design.

Table 1. Summary of measurement results for the various BiD-MOS design approaches.

BiD-MOS Design Approach	Ron [mΩ]	Breakdown Voltage [V]	Leakage Current @1.2kV [nA]	Turn-On Loss [mJ]	Turn-Off Loss [mJ]	Total Switching Loss [mJ]	SCWT [µs]
2-Chip	169.8	1640	0.73	0.81	0.67	1.48	< 2*
Monolithic	169.1	1620	0.52	0.83	0.71	1.54	3.82
Mono SN+	166.1	1640	0.46	0.79	0.69	1.48	3.67

*Due to high gate oscillations, the actual SCWT of the 2-Chip approach could not be determined.

Summary

Several Common-Drain BiD-MOS design approaches were successfully fabricated and evaluated in terms of electrical performance. The static and switching characteristics were found to be nearly identical across the different designs. However, under the SCWT test, the 2-Chip approach exhibited reliability issues that were not observed in either monolithic counterpart. Given the unhindered electrical performance, monolithic integration emerges as a promising design approach for achieving an efficient and reliable Bi-Directional Switch.

Acknowledgement

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