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Design Optimization of 600V 4H-SiC Lateral Bi-Directional MOSFET (L-BiD-MOSFET) with 3D TCAD Simulation

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Abstract. This paper presents the fabrication and characterization of a cell-to-cell integrated SiC lateral bi-directional MOSFET (L-BiD-MOSFET), with blocking performance analyzed through correlation of experimental results and 3D TCAD simulations. The fabricated devices exhibit a breakdown voltage of 600 V, notably lower than the 900 V predicted by 2D simulations. To address this discrepancy, 3D TCAD simulations were performed, which identified electric field crowding at the finger edges as the dominant factor limiting the breakdown voltage. To mitigate this effect, an extended P-top edge design was introduced, which increases the simulated breakdown voltage by more than 10%. Experimental results on devices incorporating the proposed design confirm improved breakdown capability, demonstrating good agreement with simulations. These results highlight the importance of accurate 3D simulation for edge effects in lateral structures. Overall, the proposed design strategy provides valuable guidance for the development of high-performance lateral bi-directional SiC power devices.

Introduction

Bi-directional power devices, capable of conducting and blocking current in both forward and reverse directions, are essential building blocks for emerging applications such as current source inverters (CSIs) and matrix converters. Various approaches to implementing bi-directional power devices have been reported, including package-level integration and monolithic two-chip integration [1-3]. Recently, our research group successfully demonstrated a cell-to-cell integrated SiC lateral bi-directional power MOSFET (L-BiD-MOSFET) [4, 5]. Cell-to-cell integration not only enables exploration of novel device architectures but also provides considerable area savings by sharing the central drift region. Compared with vertical device structures, lateral structures offer a distinct advantage for cell-to-cell integration, as they can be realized through layout design without requiring complex backside processing.

However, lateral power device structures in wide-bandgap materials require careful electric-field management during high-bias blocking operation. Because these materials exhibit high critical electric fields, achieving a uniform field distribution within relatively small dimensions is essential. This challenge is further pronounced in lateral devices, which contain corner and edge regions where field crowding is more likely to occur. Without proper structural optimization, local field crowding can become severe, ultimately resulting in premature breakdown. In our previous study, the measured breakdown voltage of fabricated devices was lower than simulated predictions, highlighting the need for improved design strategies. To enhance the blocking performance of cell-to-cell integrated lateral bi-directional devices, it is therefore essential to examine layout designs using 3D TCAD simulations to capture electric field concentrations accurately [6, 7].

In this work, we correlate the measurement results of fabricated L-BiD-MOSFETs with 3D TCAD simulations. The 3D analysis reveals significant electric field crowding at finger edges, and we propose an extended P-top design to mitigate these effects, thereby improving breakdown voltage. Simulation results are compared with measured device performance, demonstrating the effectiveness of the proposed design and providing insights for further optimization of high-performance SiC lateral bi-directional devices.

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Device Design and Fabrication

Fig. 1(a) illustrates the schematic structure and symbol of the SiC L-BiD-MOSFET device. It features a common-drain configuration, in which two back-to-back connected MOSFET unit cells share the central n-drift region without a dedicated drain terminal. The sources and gates of the MOSFETs are labeled as Source1 (S1), Source2 (S2) and Gate1 (G1), Gate2 (G2), respectively. The interdigitated S1 and S2 fingers are shown in Fig. 1(b). It should be noted that finger edges are present for each S1 and S2 finger unless alternative isolation techniques, such as mesa etching, are employed.

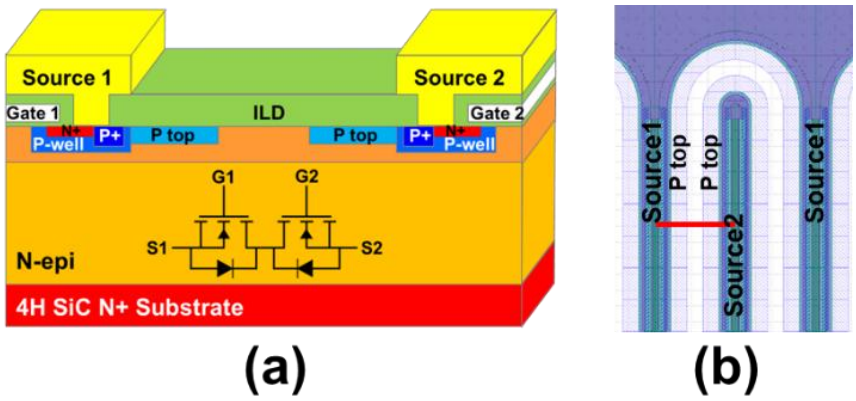

Fig. 1. (a) Cell structure of the common-drain SiC lateral bi-directional MOSFET (L-BiD-MOSFET), with the 4-terminal symbol included. (b) Top-view layout showing the designed interdigitated finger structure of the device.

The L-BiD-MOSFET devices were successfully fabricated at Clas-SiC Wafer Foundry, UK. A 10 µm thick drift layer with N- type doping concentration of 1×10^{16} cm^{-3} on an N+ 4H-SiC substrate was used. Aluminum and Nitrogen ion implants were used to form the P-well / P+ source / P-top, and JFET / N+ source, respectively. At the conclusion of all the implantation steps, an activation anneal with a carbon cap was conducted. A 50 nm thick gate oxide was formed, followed by a post-oxidation annealing (POA). An N-type polysilicon was deposited and patterned for the formation of the gate. After, an interlayer dielectric (ILD) was deposited, patterned and etched to make ohmic contact regions. After the formation of ohmic contacts, the source and gate metal, based on Aluminum, were

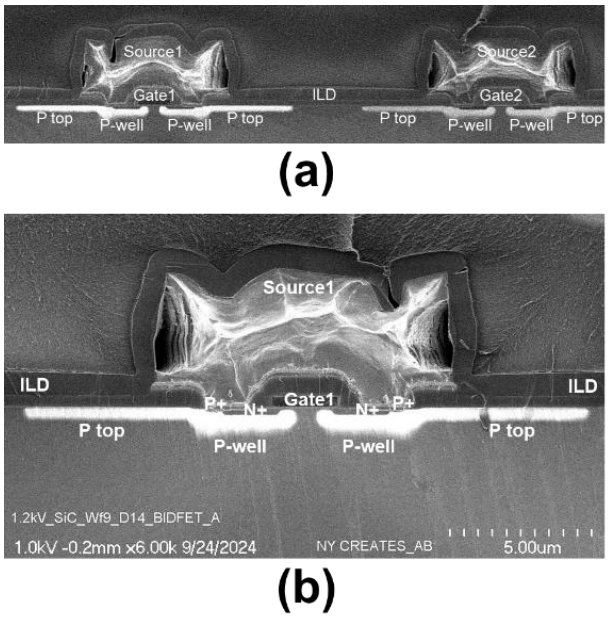

Fig. 2. Cross-sectional SEM images of the fabricated L-BiD-MOSFET. (a) Two interdigitated fingers (S1 and S2). (b) Enlarged view of the S1 finger.

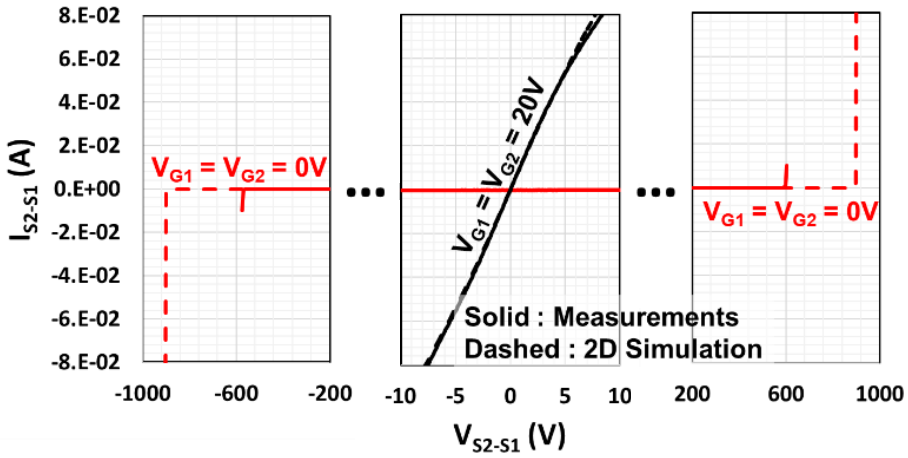

Fig. 3. Measured and simulated output and blocking characteristics of the fabricated L-BiD-MOSFET. The black curves correspond to the both-gates-on state (bi-directional conducting), while the red curves represent the both-gates-off state (bi-directional blocking). Simulations were performed using a 2D cross-sectional device structure.

deposited, patterned, and etched. For the passivation, Silicon Nitride was deposited, patterned, and etched.

Fig. 2 shows cross-sectional SEM images of the fabricated L-BiD-MOSFET devices. The symmetric finger structures are well defined and consistent with the design. It should be noted that the device was fabricated entirely using the foundry's baseline SiC planar MOSFET process.

The measured and simulated output and blocking characteristics are presented in Fig. 3. The curves correspond to two operating conditions: both gates on ($V_{G1} = V_{G2} = 20$ V) and both gates off ($V_{G1} = V_{G2} = 0$ V). These results clearly demonstrate the bi-directional and symmetric conducting and blocking behavior of the device. The measured on-state characteristics show good agreement with the simulation results; however, the fabricated devices exhibit a breakdown voltage (BV) of approximately 600 V, which is lower than the 900 V predicted by the 2D TCAD simulations.

3D TCAD Simulation

To investigate the discrepancy between the 2D simulation and the experimental results, we performed 3D TCAD simulations using Synopsys Sentaurus, focusing on the finger-edge structures that cannot be accurately captured in a 2D environment. Two edge designs were modeled (Fig. 4): (a) a conventional finger-edge structure, in which the P-top width is consistent with that of the finger

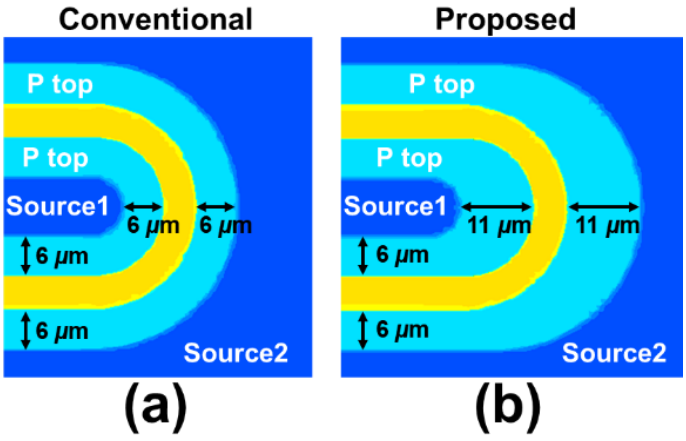

Fig. 4. Top-view diagrams showing (a) the conventional and (b) the proposed finger-edge designs generated using 3D TCAD simulations.

body, and (b) a proposed structure, where the P-top is widened by 5 μm at the finger edge to mitigate electric field crowding under reverse bias. Identical implantation and process conditions were applied in SProcess [8] to generate 3D doping profiles for both structures.

Accurate device simulation required careful meshing optimization. While fine box meshing was initially applied near the interface to resolve implantation profiles, this approach led to convergence issues in SDevice simulations. To address this, we adopted an adaptive meshing strategy that preserved fine resolution in the critical interface region while gradually coarsening the mesh deeper into the MOSFET structure, enabling stable and reliable device simulations.

Results and Discussion

As summarized in Table I, the 3D simulation of the conventional finger-edge structure under V_{S2} sweep conditions (outside high bias) yields a BV of 740 V—significantly lower than both the 2D simulation result and the BV obtained under the opposite bias condition (inside high bias). This confirms that the finger edge is the weak point with respect to electric field crowding in the outside high bias case, thereby preventing the BV from reaching the ideal 2D value.

The proposed finger-edge design achieves a notably improved BV of 818 V (about 10% increase), demonstrating that the extended P-top region effectively suppresses electric field concentration at the edge and consequently enhances the BV. The corresponding electric field distributions are shown in Fig. 5. As expected, the finger edge exhibits a stronger electric field during blocking mode; however, the proposed structure significantly mitigates this crowding. A slightly elevated—though reduced—field remains at the edge compared to the finger body, which likely accounts for the residual gap between the 3D and 2D simulated BVs.

Table 1. Simulated breakdown voltages for each structure and condition.

Bias Conditions	2D Structure	3D Conventional	3D Proposed
V_{S1} Sweep	903 V	888 V	883 V
V_{S2} Sweep	901 V	740 V	818 V

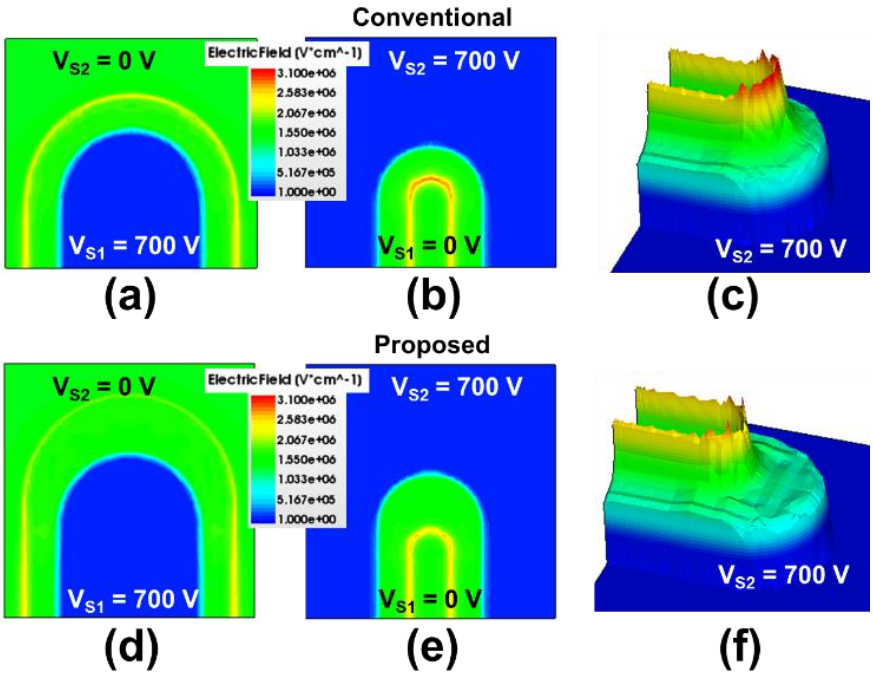

Fig. 5. Electric field distribution at a depth of 0.6 μm from the surface for (a)–(c) the conventional and (d)–(f) the proposed finger-edge designs. Bias conditions are V_{S1} = 700 V and V_{S2} = 0 V for (a) and (d), and V_{S1} = 0 V and V_{S2} = 700 V for (b), (c), (e), and (e). (c) and (f) show surface plots of the electric field at the 0.6 μm depth.

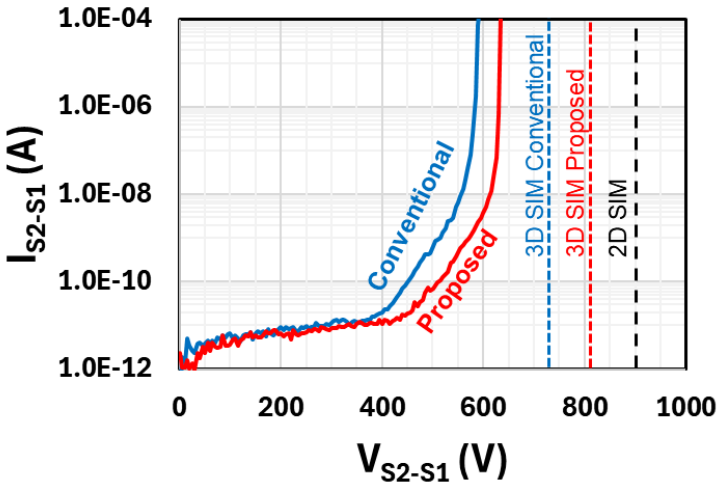

Fig. 6. Measured blocking characteristics of the fabricated devices with conventional and proposed finger-edge designs. Simulated breakdown voltages for each structure are shown as dashed lines for comparison.

Measurement results for the fabricated devices with the conventional and proposed finger-edge structures are presented in Fig. 6. The improvements observed experimentally show good correlation with the 3D simulation results, although a gap between the measured and simulated values still remains. This discrepancy appears to be common to both structures, suggesting a mismatch between the simulated and the actual fabricated devices.

Several possible causes can be considered. The most likely contributors are variations in the net P-top dose and width. Because the present design employs a P-top structure analogous to a single-zone junction termination extension (JTE), the BV is highly sensitive to these parameters [9]. Although the simulations reproduce the process flow and account for factors such as implant profiles and SiC consumption, discrepancies in the actual P+ / P-top dimensions or in SiC surface consumption could lead to deviations between simulation and experiment. To address this, calibration through a series of split experiments varying dose and width will be required, and future designs should aim to be less sensitive to such variations. Additional factors may also play a role, including the influence of SiC/oxide interface states and structural differences in the implanted regions near corners.

Note that GaN lateral bi-directional power devices at the 600 V class have been demonstrated for nearly two decades and recently commercialized by several vendors [10, 11]. Compared with GaN-based solutions, SiC L-BiD-MOSFETs can offer complementary advantages in applications where robust avalanche characteristics and high-temperature operation are emphasized. The use of a thermally grown SiO_2 gate dielectric further supports stable MOS-gated device operation within SiC processing platforms. In addition, lateral SiC device structures can be oriented toward future integration with SiC CMOS technologies, enabling increased functionality at the chip level.

Summary

In this work, we investigated and improved the blocking performance of a cell-to-cell integrated SiC lateral bi-directional MOSFET (L-BiD-MOSFET) through combined experimental characterization and 3D TCAD simulation. The fabricated devices exhibited a breakdown voltage of 600 V, notably lower than the 900 V predicted by 2D simulations, due to electric field crowding at finger edges. To address this limitation, an extended P-top edge design was proposed, which reduced field concentration and improved the simulated breakdown voltage by more than 10%. Experimental measurements of devices with the proposed design confirmed enhanced blocking capability, in good agreement with the 3D simulation results. The remaining gap between the measured and simulated breakdown voltages may be attributed to process and structural mismatches between the simulated and fabricated devices—particularly variations in the P-top dose and width, as well as differences in

the SiC/oxide interface states. These findings highlight the importance of accurate 3D TCAD analysis to capture edge effects that cannot be represented in 2D simulations. Overall, the proposed edge-engineering approach provides effective design guidance for advancing high-performance lateral bi-directional SiC power devices.

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