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Design of the Robust Edge Termination Applied to 4.5 kV SiC SBD Embedded MOSFET against Humidity

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Keywords: edge termination, field limiting rings (FLRs), SBD embedded MOSFET, HV-H^{3}TRB.

Abstract. In high-voltage class SiC devices, maintaining sufficient robustness against humidity and fabrication processes has become a major concern when minimizing the edge termination size. Previous research has shown that suppressing the maximum electric field on the SiC surface in the termination region improves durability in HV-H^{3}TRB tests for 3.3 kV SBDs. In this study, we investigated the impact of the FLR design on the electric field distribution in the termination region. Simulation results showed that the termination length can be reduced without changing the maximum electric field on the SiC surface and the breakdown voltage. Furthermore, the fabricated 4.5 kV SiC SBD-embedded MOSFETs exhibited good reverse leakage characteristics, which were consistent with the simulation results.

Introduction

Silicon carbide (SiC) is a promising material for power devices owing to its excellent properties such as a wide bandgap, a high critical electric field, and high thermal conductivity. Thus, 3.3 kV-class SiC power devices are currently applied to railways [1], and 4.5 kV-class and higher devices are expected for HVDC and power grids [2-3]. However, as the power class becomes higher, the edge termination size increases, leading to larger chip sizes and higher manufacturing costs.

Previous research indicated that field limiting rings (FLRs) exhibit high robustness against Al implantation dose variations [4-5]. Furthermore, another study showed that reducing the maximum electric field on the SiC surface ($E_{\text{surface max}}$) in the termination region improves durability in high voltage high humidity high temperature reverse bias (HV-H^{3}TRB) test for 3.3 kV Schottky Barrier Diodes (SBDs) [6].

In this paper, we investigated the impact of the FLR design on the electric field distribution in the termination region using TCAD simulation and evaluated the fabricated 4.5 kV SiC SBD-embedded MOSFETs.

Simulation Setup

Figure 1 shows a cross-sectional schematic of the simulated FLR region. The substrate and drift layer are n-type 4H-SiC (0001). The p-doped layer has a simulated Al implantation profile. Each FLR pitch (P_{FLR}) is uniform, and the ring spacing of the FLRs is designed to increase as it moves outward according to the outermost ring spacing (W_{N}). Positions (x) and (y) indicate the innermost and outermost FLR positions, respectively.

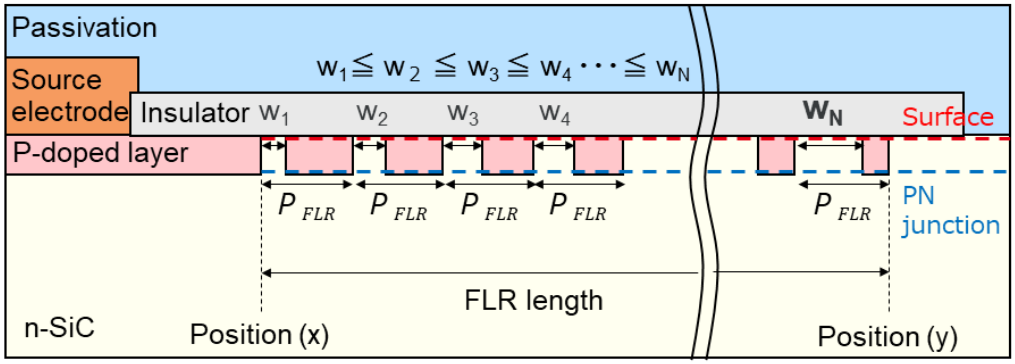

Fig. 1. Cross-sectional schematic of the simulated FLR region.

Results and Discussion

Figure 2 (a)-(c) show the simulated 2-D electric field distributions in the termination region. P_{FLR} is fixed at 9.0 µm. W_N values are set to (a) 7.2 µm, (b) 4.5 µm, and (c) 1.8 µm. The applied Drain-Source voltage is 3.6 kV, corresponding to typical HV-H^{3}TRB test conditions. As W_N decreases, the depletion layer extends further outward, causing the position of the maximum electric field to shift outward as well. The electric field distributions on the SiC surface and at the PN junction were investigated in detail. Figure 3 shows the extracted distributions. When W_N is 4.5 µm, $E_{surface\ max}$ and the maximum electric field at PN junction ($E_{PN\ max}$) reach their minimum values of approximately 1.3 MV/cm and 2.3 MV/cm, respectively. The position of the $E_{surface\ max}$ is further outward than that of $E_{PN\ max}$, which is located at the center of the FLR. It is found that $E_{surface\ max}$ should be located slightly outward from the center of the FLR structure to suppress its value.

Figure 4 compares the light emission positions and the simulated $E_{PN\ max}$ positions of PN diode TEGs with W_N values of (a) 7.2 µm, (b) 4.5 µm, and (c) 1.8 µm when avalanche breakdown occurred. As W_N decreases, the emission position shifted outward, and all emission positions correspond closely to the simulated $E_{PN\ max}$ positions.

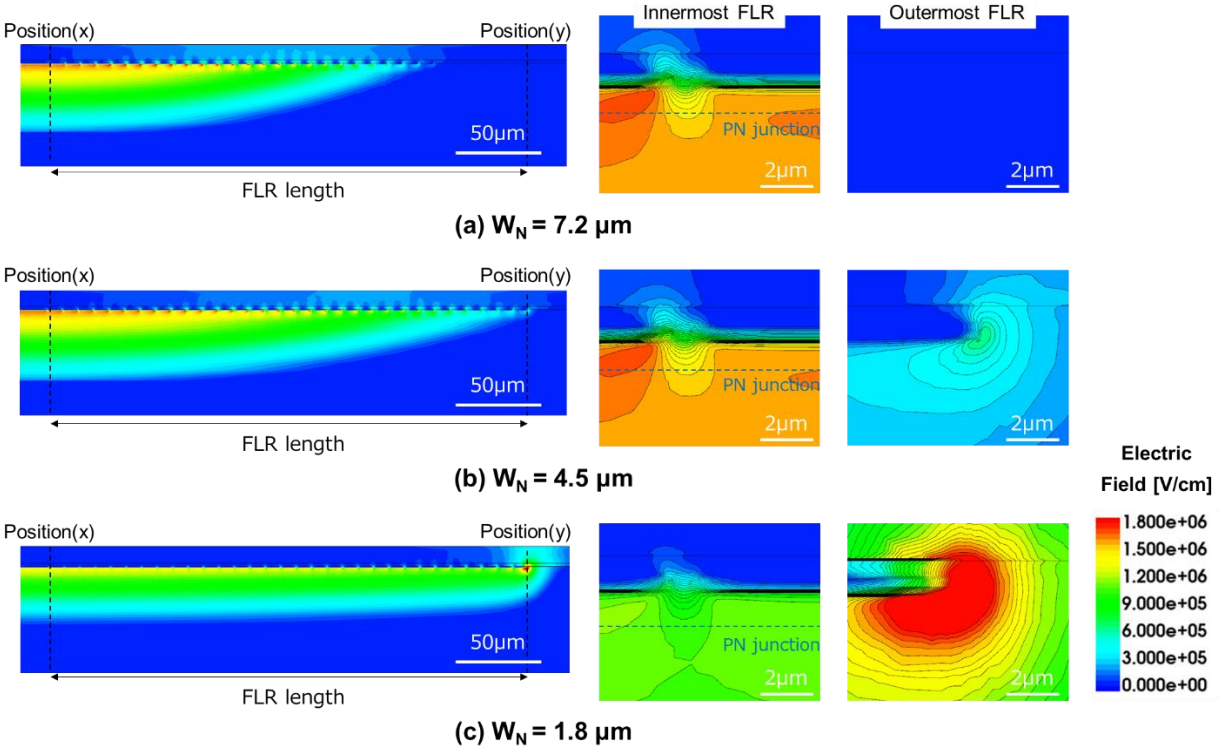

Fig. 2. Simulated 2-D electric field distributions for termination region.

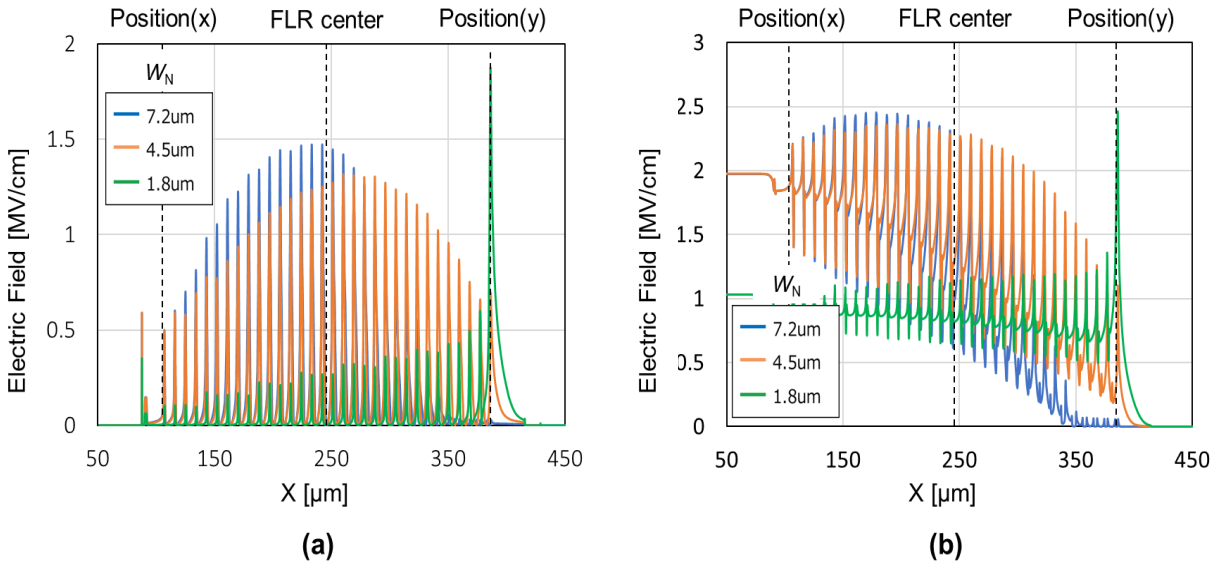

Fig. 3. Relation between electric field distribution and W_N on (a) SiC surface (b) PN junction.

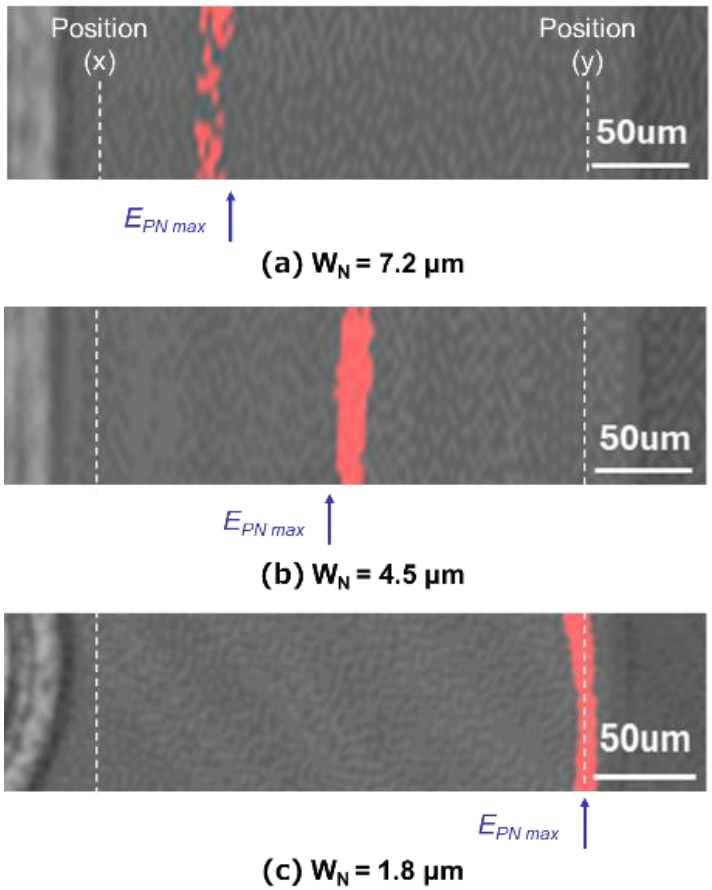

Fig. 4. Comparison between light emission and simulated $E_{PN\ max}$ position of PN diode TEGs.

We investigated the W_N at which $E_{surface\ max}$ is minimized when varying the P_{FLR} values. Figure 5 shows the relationship among W_N, $E_{surface\ max}$ and BV. The optimal W_N values vary according to P_{FLR}, with values of 3.5, 4.2, and 4.5 μm corresponding to P_{FLR} values of 5.0, 7.0, and 9.0 μm, respectively. At these values, BV doesn't decrease and there is sufficient margin for variations in W_N.

Furthermore, we investigated the dependence of $E_{surface\ max}$ and BV when varying FLR length with the optimal W_N values. As shown in Fig. 6, by reducing P_{FLR} with the optimized W_N values, the FLR length can be shortened while maintaining a low $E_{surface\ max}$ and an equivalent BV.

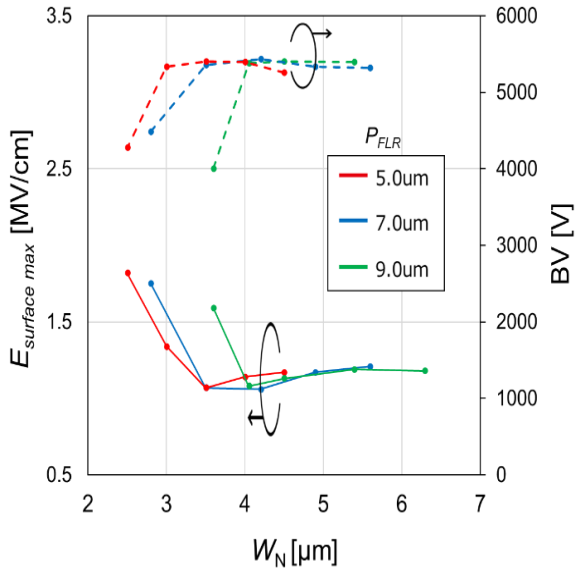

Fig. 5. Relation among W_N, $E_{surface\ max}$ and BV.

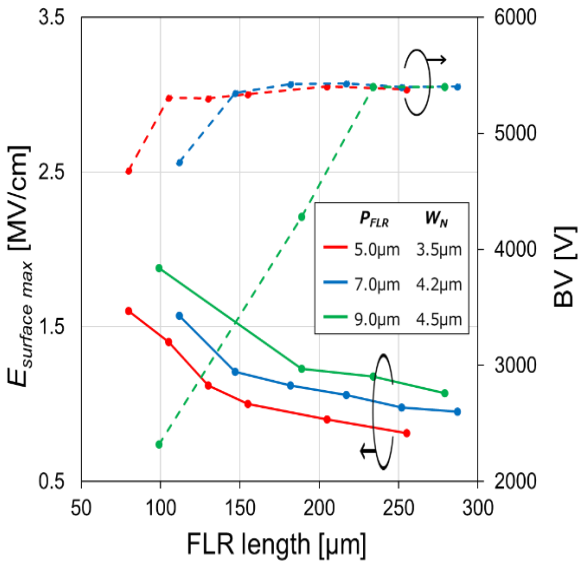

Fig. 6. Dependence of $E_{surface\ max}$ and BV when varying FLR length using the optimal W_N values.

Figure 7 shows the relationship among Al dose, BV, and $E_{surface\ max}$ for the three termination designs (A-C), which have equivalent $E_{surface\ max}$ but different termination lengths. The parameters of terminations (A-C) are presented in Table 1. Even with a short FLRs length of 155 μm, a wide margin of Al dose ranging from 1.5 to 2.5 x 10^{13} cm^{-2} was confirmed. When the Al dose exceeds 2.5x10^{13} cm^{-2}, $E_{surface\ max}$ significantly increases. This increase is attributed to the electric field concentration at the outermost FLR.

We fabricated SBD-embedded MOSFETs with the three simulated terminations (A-C). Figure 8 shows typical reverse leakage current characteristics at 25 °C with Gate-Source voltage of -7 V. The experimental BV and reverse leakage characteristics exhibited no significant differences among the three termination designs. The experimental BV matched the simulated values of approximately 5.4 kV well.

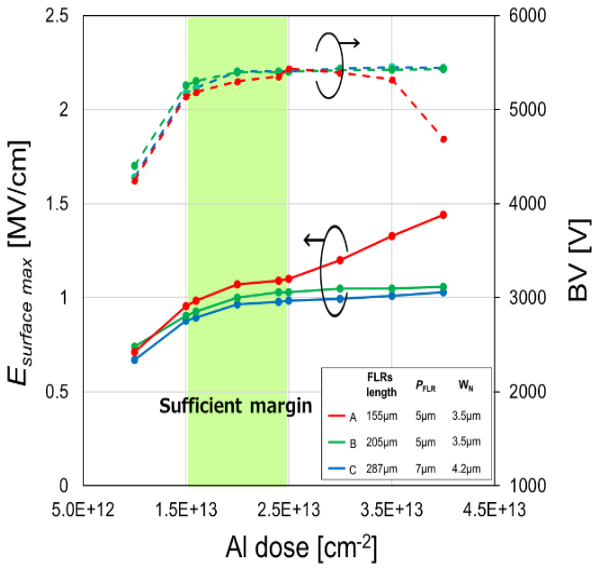

Fig. 7. Dependence of BV and $E_{surface\ max}$ on Al dose.

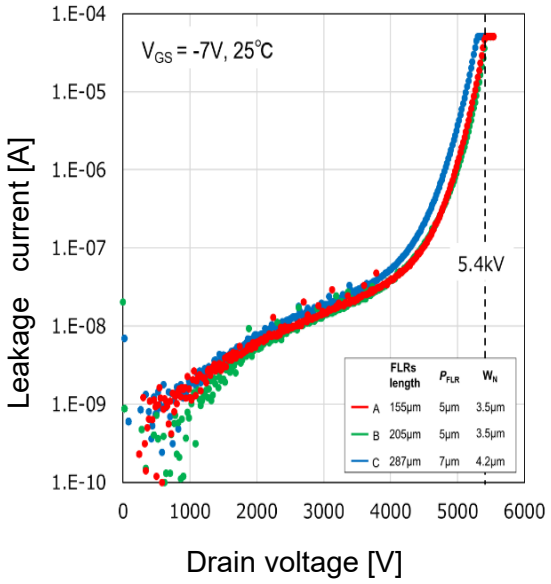

Fig. 8. Reverse leakage current characteristics of fabricated SBD-embedded MOSFET.

Table 1. Parameters of selected three termination structures.

Termination structure	FLR length [μm]	P_{FLR} [μm]	W_N [μm]
A	155	5	3.5
B	205	5	3.5
C	287	7	4.2

Summary

We investigated termination designs for 4.5 kV SiC devices from the points of cost-effectiveness, humidity-tolerance and process-robustness using simulation and fabricated 4.5 kV SiC SBD-embedded MOSFETs. By optimizing W_N, the electric field peak on the SiC surface shifts slightly outward from the center of the FLRs and $E_{surface\ max}$ reached its minimum value. By reducing the P_{FLR} with the optimized W_N, the FLR length can be shortened while maintaining $E_{surface\ max}$ low and an equivalent BV. Even with a short FLR length of 155 μm, a wide margin of Al dose ranging from 1.5 to 2.5 x 10^{13} cm^{-2} was confirmed. Furthermore, the fabricated devices exhibited almost the same BV as the simulation and showed no difference in leakage characteristics.

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