Key Engineering Materials
ISSN: 1662-9795, Vol. 1055, pp 63-68
doi:10.4028/p-Rd95Vt
© 2026 The Author(s). Published by Trans Tech Publications Ltd, Switzerland.
Submitted: 2025-09-04
Revised: 2025-12-12
Accepted: 2026-03-16
Online: 2026-05-19

JTE-Based Termination Design and Technology Considerations for 1500 V 4H-SiC Superjunction MOSFETs

Zihan Zhang[1,a], Lei Yuan[1,4,b*], Kaiyu Chen[2,c], Xiaowen Wang[2,d], Xuesong Liu[3,e], Tongxiao Hou[3,f], Bo Peng[1,g], Guibao Wang[4,h], Miao Yu[4,i], Renxu Jia[1,4,j] and Yuming Zhang[1,k]

[1]Faculty of Integrated Circuit, Xidian University, Xi’an 710071, China

[2]Alkaidsemi Electronic Technology Ltd., Shanghai, China

[3]Beijing BJAST Holdings Co., Ltd., Beijing, China

[4]Hangzhou Institute of Technology, Xidian University, Hangzhou 311231, China

[a]24251111422@stu.xidian.edu.cn, [b*]yuanlei@xidian.edu.cn, [c]gary_chen@alkaidsemi.com, [d]xiaowen_wang@alkaidsemi.com, [e]lxs6721@126.com, [f]644988605@qq.com, [g]boopeng@xidian.edu.cn, [h]wangguibao@xidian.edu.cn, [i]yumiao@xidian.edu.cn, [j]rxjia@mail.xidian.edu.cn, [k]zhangym@xidian.edu.cn

Keywords: edge termination, silicon carbide (SiC), superjunction (SJ), junction termination extension (JTE), process robustness, charge-imbalance.

Abstract. A charge-imbalanced P-pillar distribution termination (D3) is proposed for 1500 V-class 4H-SiC superjunction (SJ) devices. By combining a junction termination extension (JTE)-based termination with gradually widened P-pillar spacing, the design effectively suppresses edge electric field crowding and enhances device reliability. TCAD simulations show that D3 achieves comparable blocking capability while exhibiting significantly improved robustness against charge imbalance, oxide charge density, and JTE dose deviations, demonstrating superior process margin and reliability. With relaxed process sensitivity and an efficient structure, D3 presents a promising approach for high-voltage 4H-SiC SJ device fabrication.

Introduction

With the evolution of electric vehicle voltage platforms from 400 V to 800 V and even 1000 V, the demand for higher-voltage power devices continues to grow [1, 2]. Among them, 1500 V silicon carbide (SiC) metal-oxide-semiconductor field-effect transistors (MOSFETs) have attracted increasing attention, since 1200 V devices provide insufficient voltage margin at the 1000 V platform, while 1700 V devices result in unnecessary cost and overdesign [1]. Nevertheless, the intrinsic trade-off between breakdown voltage (BV) and specific on-resistance ($R_{on,sp}$) remains a major challenge in developing 1500 V SiC MOSFETs with high voltage capability, high current density, fast switching, and low power loss [3]. By employing charge compensation effect, superjunction (SJ) technology breaks the conventional BV ~ $R_{on,sp}$ trade-off, allowing for higher drift doping concentrations under high breakdown conditions and thus offering significant potential for low-loss, high-voltage device operation [4]. However, the charge balance in SJ devices, realized by periodically alternating heavily doped N-pillars and P-pillars, demands highly precise process control, significantly increasing fabrication complexity, especially in the termination region [5-8]. Notably, studies on SiC SJ terminations remain limited, and most using uniform P-pillar distributions, with few analyzing the impact of P-pillar distribution on termination performance [2, 9, 10].

In this work, we propose a novel charge-imbalanced P-pillar distribution structure for JTE-based 4H-SiC SJ terminations (D3) for 1500 V 4H-SiC SJ-MOSFETs. The design more effectively suppresses edge electric fields by gradually widening the P-pillar spacing, and achieves more efficient lateral depletion of the superjunction by JTE structure. We evaluate the impact of P-pillar distribution on the performance and process robustness of JTE-based 4H-SiC SJ terminations.

This article is an open access article under the terms and conditions of the Creative Commons Attribution (CC BY) license (https://creativecommons.org/licenses/by/4.0)

Design and Simulation

Figures 1(c)–1(e) show three termination designs with different P-pillar distributions: D1 with uniform spacing (N/P balanced), D2 with a non-uniform distribution (N-rich center, P-rich edges), and D3 transitioning from P-rich to N-rich. It is worth noting that in JTE-based SJ terminations, the JTE region sustains the surface electric field while the SJ pillars support the bulk field, and their combined action provides effective protection for the MOSFET cell region. The top-view layout is shown in Figure 1(a). The corresponding breakdown voltages, shown in Fig. 1(b), all exceed 1700 V, satisfying the 1500 V voltage device requirement. The electric field distribution at 1500 V is shown in Fig. 2. D1 exhibits higher P-pillar utilization efficiency, with the P-pillars near complete depletion at the edge of the termination due to the relatively small uniform spacing.

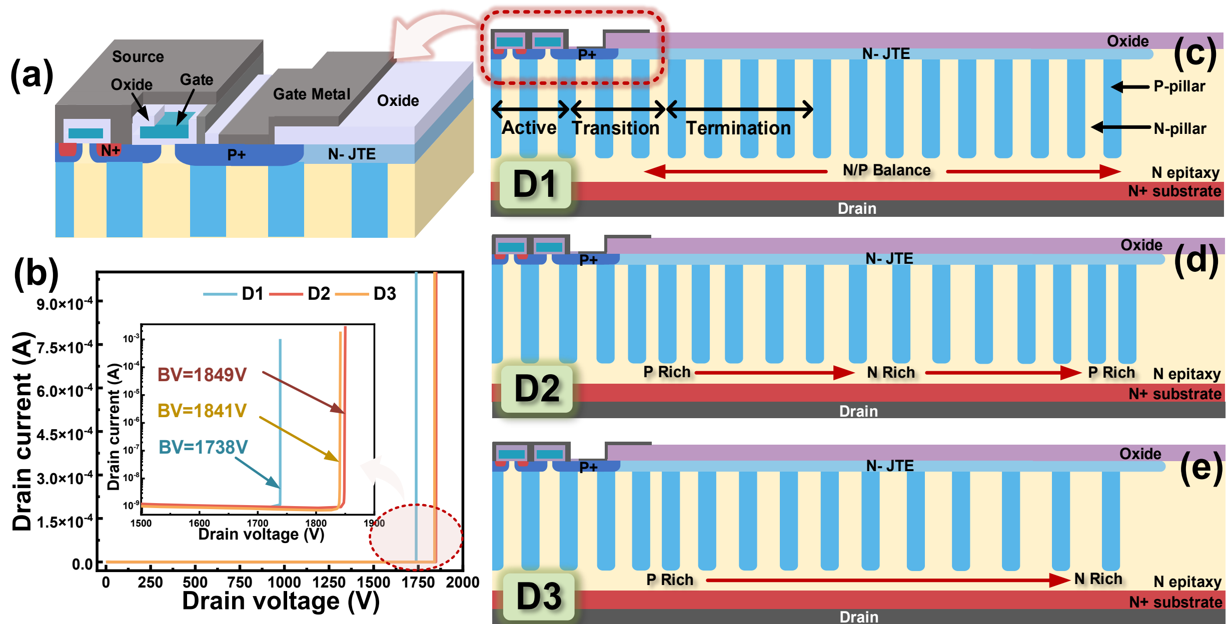

Fig. 1. SJ termination structures including (a) top-view layout, (b) reverse blocking performance, and (c) N/P balanced, (d) N-rich center with P-rich edges, and (e) P-rich to N-rich transition designs.

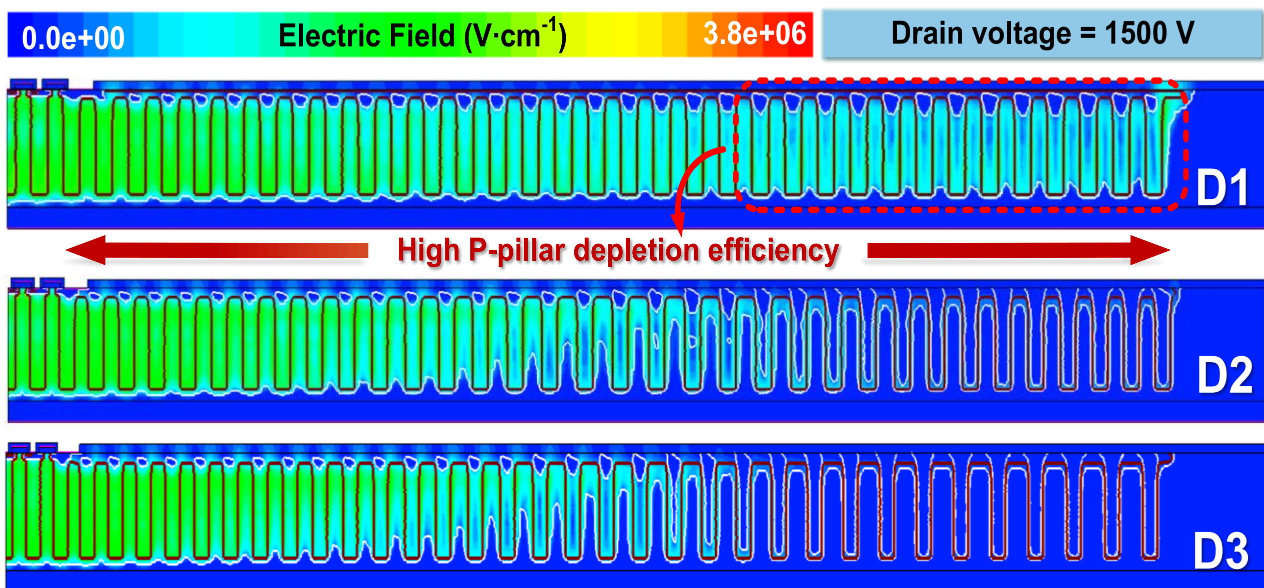

Fig. 2. Electric field distributions of D1–D3 under 1500 V blocking voltage, showing higher termination efficiency for D1.

Fig. 3 further analyzes the electric field distribution along different cutlines (C1~C3) at a blocking voltage of 1500 V. Significant electric field peaks appear near the terminal surface at C1 and C2 in D1, exceeding the bulk field level, while a sharp field drop is observed at the edge (C3). Such insufficient redistribution of the bulk field induces edge field crowding, potentially threatening long-term reliability despite meeting the 1500 V blocking requirement. In D2, the electric field peak at C1 and C2 degrade device reliability, even though their peaks are below the bulk field level. By comparison, D3 demonstrates a highly uniform field profile, indicating improved prospects for long-term device stability. In the D3 structure, the lateral charge-compensation gradient transitions gradually from a P-rich region near the source to an N-rich region toward the edge. This graded profile enables a smoother lateral depletion process, allowing the electric field to spread across a wider effective termination width rather than concentrating near the gate-oxide surface.

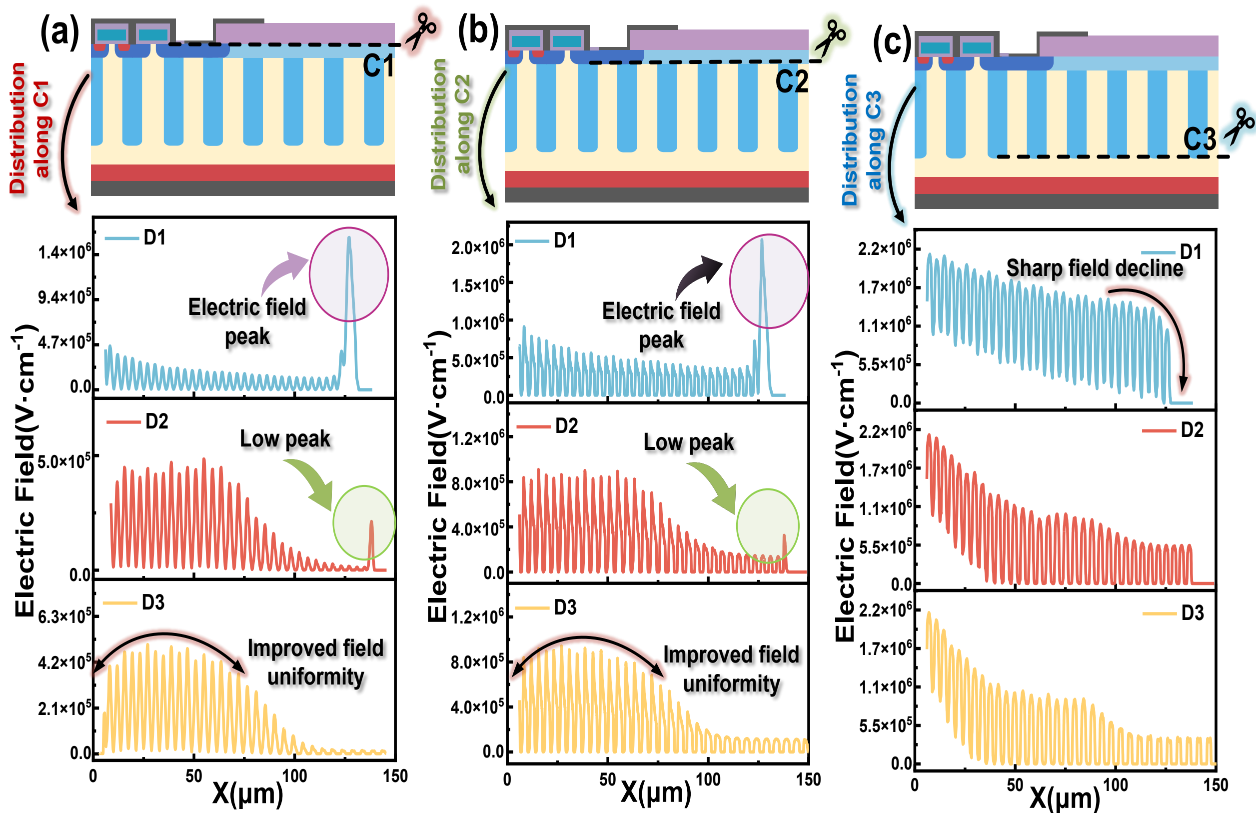

Fig. 3. Electric field distributions along (a) C1, (b) C2, and (c) C3 cutlines under 1500 V drain bias for different termination designs.

Process Robustness Evaluation

Breakdown Voltage Dependence on charge imbalance.

The reliance of SJ structures on precise charge balance makes them highly sensitive to process variation, posing a major challenge to device fabrication. Fig. 4(a) shows the impact of P-pillar dose errors on termination performance. It is observed that D3 maintains 1500 V blocking capability with an error window exceeding ±8 %, showing a clear advantage, especially under P-rich conditions. The improved robustness is attributed to the widened P-pillar spacing at the edge, which reduces the effect of charge imbalance on termination performance.

Breakdown Voltage Dependence on oxide charge density.

The impact of oxide charge located at the SiO_2/SiC cannot be ignored in the manufacturing of SiC devices [11]. The sensitivity of the termination blocking capability to the oxide charge density (N_{OX}) is illustrated in Fig. 4(b), with the calculation range of N_{OX} selected according to representative values

previously reported in the literature [12, 13]. Both positive and negative interface charges affect the BV, with higher densities markedly degrading the terminal blocking capability. For positive oxide charge, all three structures exhibit nearly identical blocking performance, while D3 shows a broader blocking range under negative oxide charge. With a tolerance window of 1.1×10^{13} cm^{-2} at 1500 V blocking, D3 achieves a 51% improvement compared with D1. The breakdown current distribution at a negative N_{OX} of 5×10^{12} cm^{-2} is shown in Fig. 5. The breakdown location of D3 shifts inward compared to D1 and D2, indicating its potential to withstand higher negative oxide charge density.

Breakdown Voltage Dependence on JTE dose error.

The impact of JTE concentration variation on termination blocking capability was investigated in Fig. 4(c), considering the dose sensitivity of JTE structures. The blocking capability of D1 degrades markedly once the JTE dose exceeds the optimum. By contrast, D2 and D3 exhibit low sensitivity within a ±15% dose variation, thereby relaxing implantation accuracy requirements and resulting in a significantly wider tolerance window. Fig. 4(d) shows that under a 5% JTE dose deviation with a termination length of 140 μm, D1 suffers from pronounced edge field crowding, whereas D3 reduces the edge electric field by 92% along cutline C2, even though both designs exhibit comparable blocking capability.

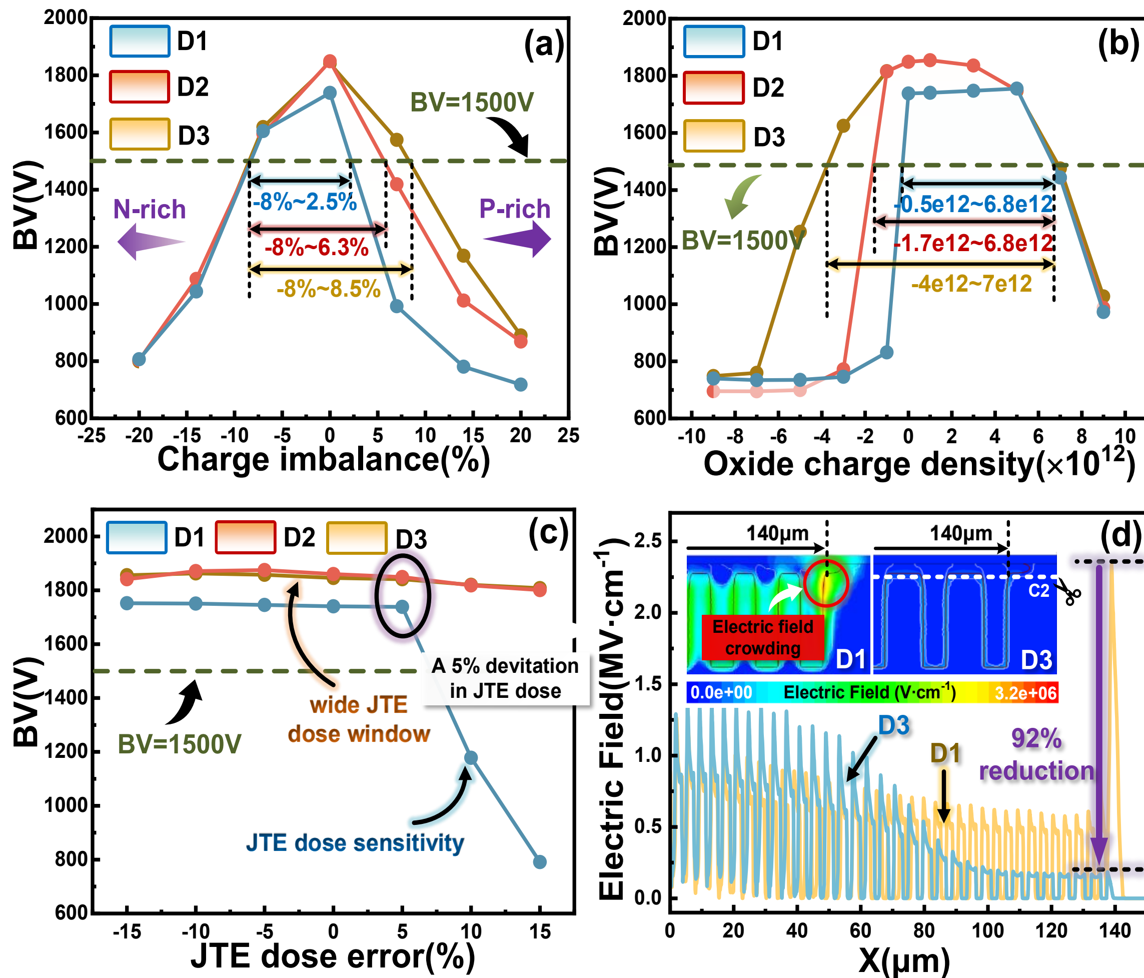

Fig. 4. Impact of (a) charge imbalance, (b) oxide charge density, and (c) JTE dose error on breakdown voltage for D1, D2, and D3, and (d) electric field distributions under a 5% JTE dose deviation.

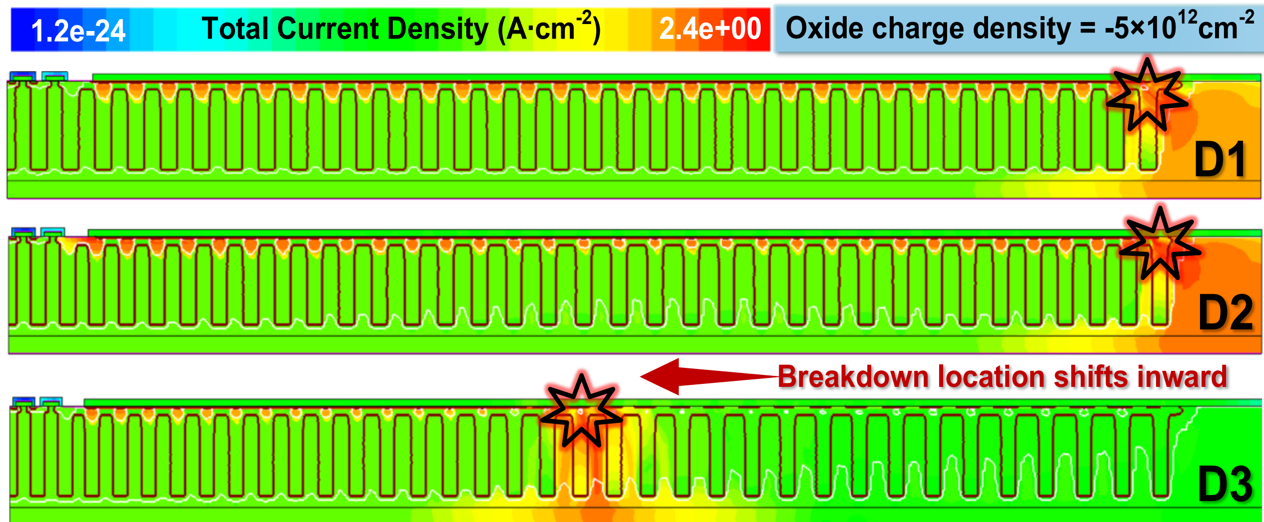

Fig. 5. Breakdown current density distribution of D1–D3 at $N_{OX} = -5\times10^{12}$ cm^{-2}, with D3 showing breakdown closer to the active region, indicating a higher tolerance to negative charge density.

The enhanced robustness of D3 originates from the lateral P-rich to N-rich pillar arrangement, which promotes smoother lateral depletion and suppresses edge field concentration, thereby reducing the impact of charge imbalance, oxide charges, and JTE-dose variations.

Summary

In this work, the impact of P-pillar distribution on JTE-based terminations for 4H-SiC SJ MOSFETs was systematically investigated. TCAD simulations of three representative designs (D1–D3) demonstrated that the D3 structure with a non-uniform P-pillar distribution provides the most uniform electric field profile and superior robustness against process-induced variations, including superjunction charge imbalance, interfacial oxide charges, and JTE dose deviations. These results indicate that the D3 termination is a promising solution for high-voltage SiC SJ devices, offering both enhanced breakdown capability and improved process tolerance.

References

[1] Information on https://www.componentbuy.com/newsroom/byd-unveils-1500v-sic-module-on-super-e-platform.

[2] Information on https://sichainsemi.com/products/2.html.

[3] B.J. Baliga, Fundamentals of Power Semiconductor Devices, Springer, New York, 2010.

[4] T. Masuda, T. Hatayama, S. Harada, and Y. Saitou, Edge termination design with strong process robustness for 1.2 kV-class 4H-SiC super junction V-groove MOSFETs, C. International Symposium on Power Semiconductor Devices & ICs (ISPSD). (2020) 166-169.

[5] R. Ghandi, C. Hitchcock, T. Saha, E. Delgado, S. Kennerley, 5-kV SiC Deep-Implanted Superjunction MOSFETs, J. IEEE Electron Device Lett. 46 (2025) 533-555.

[6] M. Okada, S. Kyogoku, T. Kumazawa, J. Saito, T. Morimoto, M. Takei, S. Harada, Superior short-circuit performance of SiC superjunction MOSFET, C. International Symposium on Power Semiconductor Devices & ICs (ISPSD). (2020) 70-73.

[7] Tawara, Takeshi, Kensuke Takenaka, Syunki Narita, Mitsuru Sometani, Kunihide Oozono, Shiyang Ji, Tadao Morimoto, Shinsuke Harada, Effect of the column design and fabrication method on the reverse recovery characteristics of 1.2 kV SiC-superjunction-MOSFETs, J. Materials Science in Semiconductor Processing. 176 (2020).

[8] Y. Kobayashi, S. Kyogoku, T. Morimoto, T. Kumazawa, Y. Yamashiro, M. Takei, S. Harada, High-temperature performance of 1.2 kV-class SiC superjunction MOSFET, C. International Symposium on Power Semiconductor Devices & ICs (ISPSD). (2019) 31-34.

[9] Wang R, Qiao M, Wang Y, Li Z, Zhang B, Novel high-tolerance termination with resistive field plate for 600 V super-junction vertical double-diffused MOSFET, J. IEEE Electron Device Letters. 43 (2022) 1093-1096.

[10] Kang H, Du F, Yuan H, Bai B, Zhou Y, Li J, Han C, Tang X, Song Q, Zhang Y, Analysis and fabrication of a SiC super-junction termination structure in a state of charge imbalance, J. Science China Information Sciences. 68 (2025).

[11] Feng, Gan, Jun Suda, Tsunenobu Kimoto, Space-modulated junction termination extension for ultrahigh-voltage pin diodes in 4H-SiC, J. IEEE transactions on electron devices. 59.2 (2011) 414-418.

[12] D. Okamoto, H. Yano, K. Hirata, T. Hatayama, T. Fuyuki, Improved Inversion Channel Mobility in 4H-SiC MOSFETs on Si Face Utilizing Phosphorus-Doped Gate Oxide, J. IEEE Electron Device Letters. 31 (2010).

[13] Dhar S, Feldman LC, Wang S, Isaacs-Smith T, Williams JR, Interface trap passivation for SiO_2 /$(000\bar{1})$ C-terminated 4H-SiC, J. Journal of Applied Physics. 98 (2005).