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# 2x Current Boosting Scheme in 3300 V 4H-SiC VDMOSFET

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**Keywords:** 3300 V, silicon carbide, low specific on-resistance, on-current improvement, p-well bias.

**Abstract.** We experimentally demonstrated a ~2x on-current enhancement in VDMOSFET fabricated in a standard 3300 V-rated 4H-SiC process. The on-current improvement is achieved by applying a positive bias to the p-well region when the VDMOSFET is in the on-state. A $5x10^3$-$10^4$ ratio between the on-current gain and the p-well current gain is shown. TCAD simulations are performed to study the underlying mechanisms of the on-current gain.

## Introduction

Wide bandgap (WBG) semiconductors, such as silicon carbide (SiC), have been increasingly utilized in high-voltage, high-power applications due to advantages in electrical and thermal properties over silicon. Low conduction losses is one of the requirements of power semiconductor applications and therefore there are many efforts to improve the on-current and specific on-resistance of SiC devices, for example through process improvements [1-3], cell topologies [4], and charge modulations [5]. Previously, we demonstrated a >2.5x on-current improvement in 1200 V-rated 4H-SiC based MOSFET through the application of p-well voltage [6]. 3300 V-rated devices have received significant interest for solid-state transformers, industrial and traction applications. In this work, we demonstrated a ~2x on-current enhancement resulting from p-well voltage biasing in 3300 V-rated 4H-SiC based VDMOSFET.

Figure 1(a) illustrates a schematic cross-sectional view of our VDMOSFET device, which is fabricated in a standard 3.3 kV 4H-SiC process on 150 mm wafers. The details of the fabrication process are described in [7] and a breakdown voltage of 3950 V is achieved (Figure 1(b)).

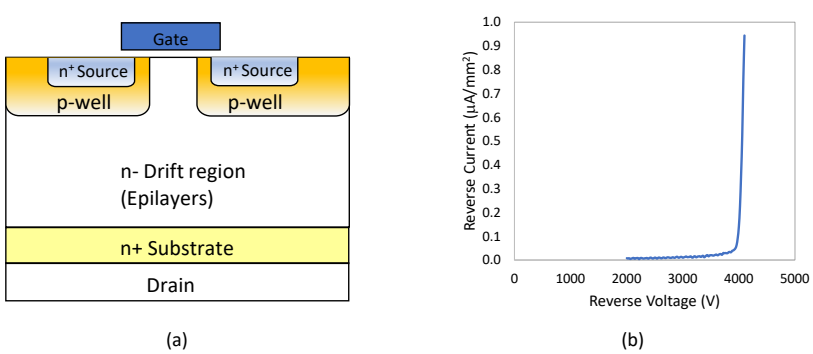
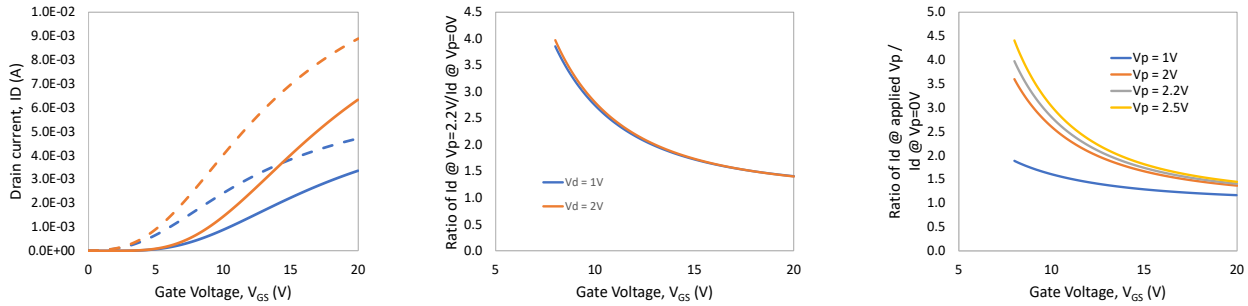



**Fig. 1. (a)** Cross-sectional view of device structure, **(b)** Breakdown characteristic of a typical 3300V device.

Separate contacts are formed for the p-well and source regions, allowing for independent biasing of both regions (p-well contact is not shown in Figure 1(a)). A positive bias is applied to the p-well region when the VDMOSFET is in the on-state and removed when it is in the off-state. In a conventional VDMOSFET, the p-well and source regions are shorted and typically connected to a common ground.

## Results and Discussion

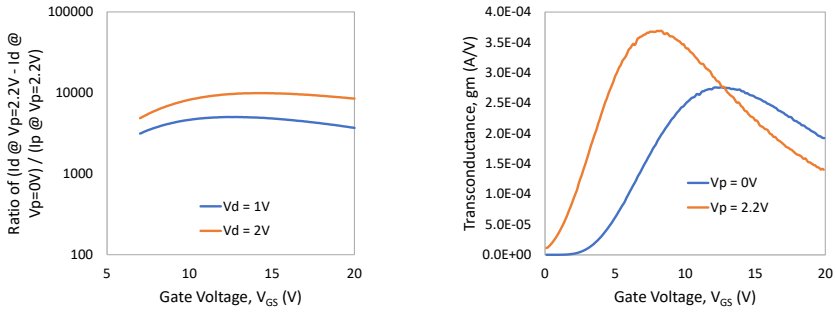
Figure 2(a) shows the Id-Vg curves measured from a test structure having a JFET width of 15 μm for different Vp and drain voltage (Vd). The ratio of the drain current with Vp=2.2V and Vp=0V for a range of gate voltage (Vg) is shown in Figure 2(b), demonstrating ~2x on-current when Vp=2.2V is applied compared to conventional VDMOSFET (with Vp=0V). The ratio of the on-current as a function of applied Vp bias is also shown in Figure 2(c), indicating that the current flow across the VDMOSFET can be controlled by both Vg and Vp. When the VDMOSFET is turned off, the positive Vp bias is removed and the off-state characteristics return to those with Vp=0V applied. In addition, the application of Vp bias has been shown to reduce both the variability of the threshold voltage and the time-dependent threshold voltage drift [8, 9].




(a) (b) (c)

**Fig. 2. (a)** Id-Vg characteristics of VDMOSFET for Vd=1V and 2V with Vp=0V (solid) and Vp=2.2V (dashed), **(b)** Ratio of drain current with Vp=2.2V and Vp=0V applied, **(c)** Ratio of drain current at different applied Vp and Vp=0V for Vd=2V.

Kimoto and Watanabe have previously shown that the drift resistance accounts for ~80% of the on-resistance of 3300 V SiC power MOSFET [10]. The p-well current is measured to study whether the significant on-current gain can be attributed to the vertical BJT device. Figure 3(a) provides the ratio of the on-current gain to the p-well current (i.e. the BJT gain). A high ratio of $5x10^3$-$10^4$ is observed, demonstrating that the large current gain does not require a large p-well current. The improvement in the channel resistance is investigated by measuring the transconductance (gm). Figure 3(b) shows a ~30% higher peak gm with Vp=2.2V. The Id-Vg and gm show that threshold voltage (Vt) shift and gm contribute to the on-current gain.




(a) (b)

**Fig. 3. (a)** Ratio of current gain (the difference between drain current with Vp=2.2V and 0V) and p-well current for Vd=1V and 2V, **(b)** Transconductance (gm) for Vd=2V with Vp=2.2V and 0V.

TCAD simulations are performed to further study the underlying mechanisms of the drain on-current gain. The TCAD simulations have been calibrated using the experimental results from the 1.2 kV 4H-SiC process and adjusted to account for the differences between the 3.3 kV and 1.2 kV processes. Figure 4 illustrates a comparison of the Id-Vg characteristics of the 3.3 kV device under Vp=0V and Vp=2.2V bias conditions. As shown in Figure 4, TCAD simulations also show a ~2x on-current, consistent with the experimental results.

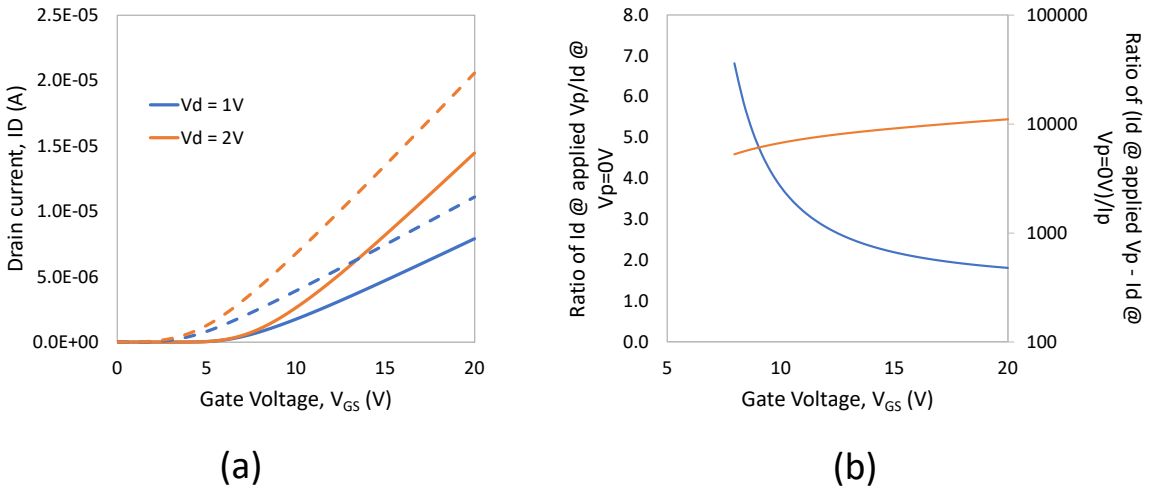



**Fig. 4. (a).** TCAD simulation Id-Vg characteristics of VDMOSFET for Vd=1V and 2V with Vp=0V (solid) and Vp=2.2V (dashed), (b) TCAD optimization results showing drain current gain (left axis) and the ratio of current gain to p-well current (right axis).

Figure 5(a) illustrates a cross section of the energy band diagram along the source/p-well/drift region junctions with Vp=0V and Vp=2.2V bias applied. Applying a positive Vp bias lowers the energy barrier between the source and the p-well regions, increasing current flow through the p-well region. A comparison of the current density plots shows that a higher current density is observed throughout the source junction region and is not limited to only the area near the surface channel when a positive bias is applied to the p-well. Electron flow in the region away from the surface area is not limited by the poor channel mobility of SiC, and as a result, a higher effective mobility, $\mu_{eff}$ is obtained, as observed by the higher transconductance shown in Figure 3(b). This is similar to the effect of on-resistance improvement through the formation of current spreading layer (CSL) or deep JFET layer shown by Jang et al. [11] and Kim et al. [12], respectively.

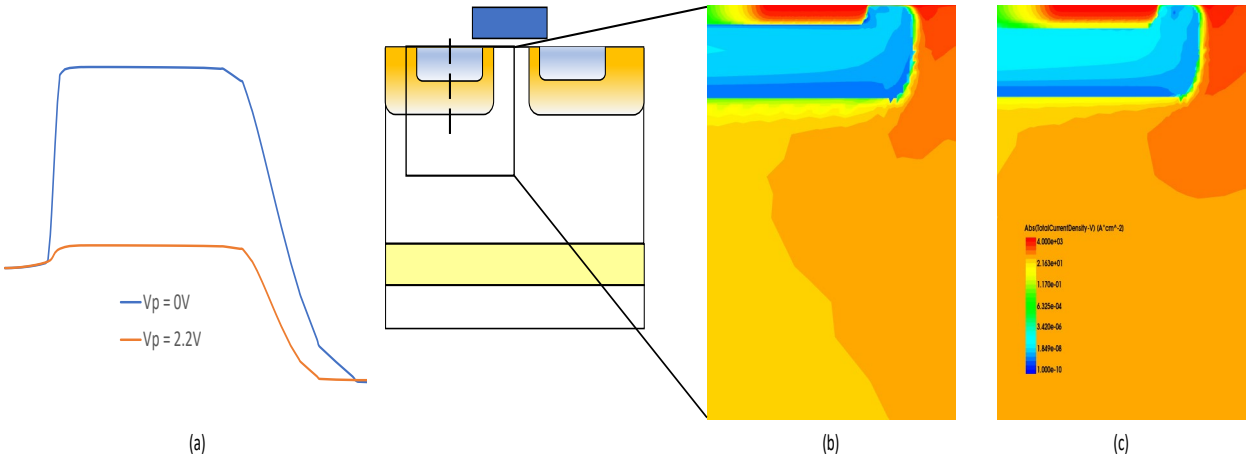



**Fig. 5.** TCAD simulation results showing (a) the energy band diagram across the region indicated by the dashed line, and total current density in the VDMOSFET region enclosed by the box for (b) Vp=0V and (c) Vp=2.2V.

TCAD simulations are also used to further optimize the 3.3 kV device. As shown in Figure 4(b), a higher on-current can be achieved through further device structure optimizations, while maintaining $5x10^3$-$10^4$ ratio between on-current gain and the p-well current. This is accomplished by further increasing the conduction area to encompass a larger portion of the source area.

The specific on-resistance is shown in Figure 6 alongside selected 3.3 kV results [13-15] and our previous 1.2 kV results [6], demonstrating that the p-well biasing results approach the SiC limit [16].

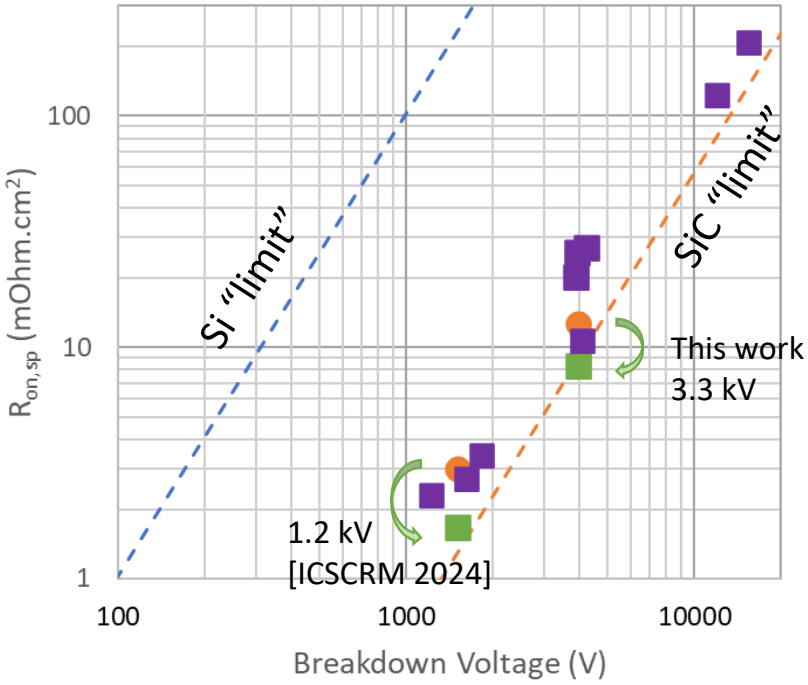



**Fig. 6.** Specific on-resistance vs. breakdown voltage, showing p-well boosting approaches the SiC limit.

## Summary

A ~2x improvement in the on-current of 3300 V-rated 4H-SiC VDMOSFETs has been demonstrated. The current gain is achieved through the application of a positive bias to the p-well region. The application of the p-well bias does not result in significant increase in the p-well current, where a ratio of $5x10^3$-$10^4$ between the on-current gain and the p-well current is observed. The specific on-resistance demonstrates that the p-well biasing yield results approaching the SiC limit. TCAD simulations are performed to understand the current boosting mechanism and to investigate further optimizations.

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## Author Contribution

YW: conceptualization (equal), writing – original draft (lead), formal analysis (lead), writing – review and editing (equal).
VN: conceptualization (equal), formal analysis, writing – review and editing (equal).
OM: formal analysis, writing – review and editing (equal).
AA: conceptualization (equal), formal analysis, writing – review and editing (equal).
NX: data curation (equal), investigation – simulation (equal), writing – review and editing (equal).

TD: data curation (equal), investigation – simulation (equal), writing – review and editing (equal).
DB: data curation (equal), investigation – simulation (equal), writing – review and editing (equal).
SR: data curation (equal), investigation – device layout, process, test (equal), writing – review and editing (equal).
LL: data curation (equal), investigation – device layout, process, test (equal), writing – review and editing (equal).
RY: data curation (equal), investigation – device layout, process, test (equal), writing – review and editing (equal).
YQ: data curation (equal), investigation – device layout, process, test (equal), writing – review and editing (equal).
DTC: data curation (equal), formal analysis, investigation – device layout, process, test (equal), writing – review and editing (equal).

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