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The Tunneling Field-Effect Transistor as Novel Device Concept for High-Frequency Hard-Switching Power Electronics

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Abstract. With ever-increasing power conversion densities in electric power converters, the volume of the converter must shrink for a certain power rating, which in turn demands the reduction in size of the energy-storing passive component. Constant power rating of those systems and the reduction of size of passive components leads to a higher switching frequency of the semiconductor power switches. At high switching frequencies, dynamic losses in the power semiconductor device dominate the overall power losses. Consequently, novel device concepts that address dynamic power losses may be superior to conventional power devices, even though they might have a higher static on-state loss. In this paper, the concept of the power tunneling field-effect transistor (Power-TFET) employing tunneling between a highly p-type doped source region and a n-type accumulation channel is proposed and compared to an equivalent LDMOS in terms of static and dynamic losses. Devices fabricated in a 2 µm 4H-SiC technology are measured and compared to evaluate the viability of the Power-TFET device concept. The fabricated Power-TFET shows high-voltage blocking capability and has a switchable tunneling junction with on- and off-state, despite showing high on-state resistance due to the tunneling through the wide bandgap of 4H-SiC. The alternative of tunneling through a switchable Schottky barrier is simulatively explored to solve the high on-state resistance of the pn-junction based Power-TFET.

Introduction

Many of the disciplines in semiconductor engineering have shown exponential development in their fields over the years. The most prominent example of such exponential growth is the integration density of integrated circuits and the scaling of the individual semiconductor devices in logic circuits, which was first described by Gordon Moore [1]. Analogous to Moore's law, there is also an exponential increase in the power conversion density over time in the field of power electronics [2]. The power conversion density describes the amount of electrical power transferred and converted in a set converter volume. To further increase the power conversion density, it is therefore mandatory to reduce the converter volume for a set power throughput. A reduction of the converter volume can mainly be achieved by two means. First, the energy storage components that need the most space in typical converter applications must shrink, which mandates higher frequency switching since the same power must be transferred through the smaller energy storage components [3] and second, smaller cooling solutions are required, which mandates lower power losses of the semiconductor devices at the same power throughput. In essence, semiconductor power devices need to become more efficient at higher switching frequencies for future applications. Every power device technology for a certain blocking voltage has a fundamental limit in terms of the efficiency that it can reach in a converter [4]. The efficiency is set by the static conduction losses during on-state and the dynamic losses that arise from switching. Consequently, the overall converter efficiency decreases with

increasing switching frequency [4]. In many power electronic applications that use metal oxide semiconductor field-effect transistors (MOSFET) or high electron mobility transistors (HEMT), the dynamic losses surpass the static losses already in the frequency range between 20 kHz and 100 kHz, which makes it impractical to surpass the 1 MHz mark without significant drawbacks in terms of dynamic power losses and therefore more complex and bulkier cooling [4].
A sensible solution for the shortcomings of the existing technologies is to search for device concepts that enable lower power consumption during hard switching processes. In this paper, the possibility of a tunneling field-effect transistor (TFET) for power applications (Power-TFET) is explored. The concept of the TFET has been developed over the past two decades [5] to find a steep-slope concept to replace the conventional MOSFET. The goal is to achieve higher efficiency of those integrated circuits by reducing the supply voltage necessary for reliable switching. Since the load at the output node of a complementary MOS (CMOS) logic gate is typically the input capacitance of the following CMOS logic gate, static losses are of smaller interest, and the dynamic losses are dominant. Bohr and Young have shown in their work that TFETs need less energy for switching and have a lower delay at the output node [6]. Considering this, the TFET may as well be a viable concept for a fast-switching power device.

The Tunneling Field-Effect Transistor as a Power Device Concept

A TFET, in its most basic form, is a pin-diode with a MOS gate adjacent to its intrinsic region. The MOS electrode controls the potential at the semiconductor interface such that carriers can tunnel from the source region into the now formed channel [7]. This works for n- and p-channel TFETs in the exact same way due to the ambipolar device behavior. A basic schematic of such a TFET is given in Fig. 1 a). For a power electronic device, such a TFET is not yet useful since only n-channel behavior is of interest due to the higher mobility of electrons. Additionally, a drift region must be added to contain the electric field at high blocking voltages. Therefore, the device structure shown in Fig. 1 b) is proposed. In comparison to the conventional TFET in Fig. 1 a), the gate is shortened to only cover the source-side junction of the central region to suppress the ambipolarity and prevent drain-side breakdown of the gate at high blocking voltages. The central intrinsic region is extended on the drain-side to accommodate higher fields and lightly n-type doped for better conduction in on-state. A similar device structure was already proposed in a patent by Vandenderghe and Verhulst in [8], although not for power semiconductor device applications but for CMOS applications, where ambipolarity is suppressed.

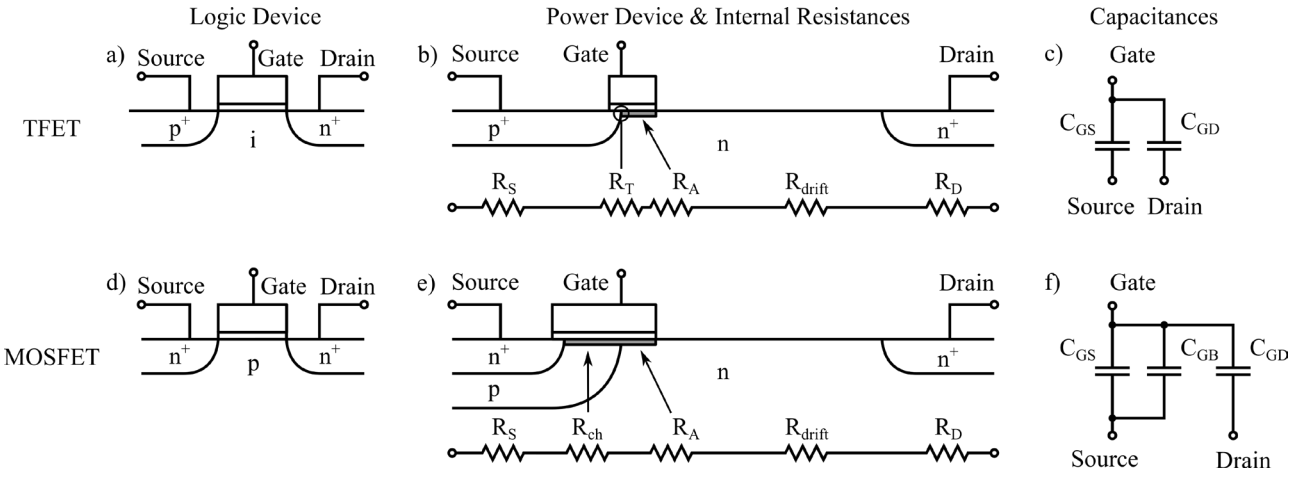

Fig. 1. Comparison of the a) TFET and d) MOSFET for logic applications with their power device counterparts in b) and e). Their respective internal resistances are shown, representing the static loss of each device. The channel is marked in grey in both cases. In c) and f) the input capacitances of Power-TFET and LDMOS are compared, representing the dynamic losses.

In Fig. 1 b), the static loss of the Power-TFET is compared with the static loss in on-state of an equivalent lateral power MOSFET shown in e). From the device structure it is apparent that the commonalities between the shown MOSFET and Power-TFET are mostly given by the resistances of the drift region R_{drift}, source region R_S, and drain region R_D. However, the total channel resistance differs greatly. The channel of the MOSFET can be separated in two sections: First, the inversion channel resistance R_{ch} within the p-type doped body and second, the resistance of the accumulation channel R_A at the overlap of the gate with the drift region. The channel of the Power-TFET can also be separated in two parts: First, a non-linear tunneling resistance at the junction R_T and second, the accumulation channel resistance R_A at the gate overlap with the drift region. Assuming the drift region overlap of the gate electrode is equal for the MOSFET and the Power-TFET than the accumulation channel resistance R_A are also equivalent. We can therefore directly compare the MOSFETs inversion channel resistance with the tunneling resistance in the Power-TFET to evaluate the relative static losses. The inversion channel resistance R_{ch} in a MOSFET at small drain-source voltage V_{DS} is given in [9, p. 327] as follows:

$$R_{ch} = \frac{L_{ch}}{w_{ch}\mu_n C_{ox}(V_G - V_{th})} \tag{1}$$

L_{ch} describes the channel length, w_{ch} the channel width, μ_n the inversion layer mobility of the electrons, C_{ox} the specific oxide capacitance and V_G-V_{th} is the difference between the applied gate voltage and the threshold voltage.

The tunneling resistance in a TFET is non-linear, which is apparent by the non-linearity of the tunneling current in p^+-n^+ junction. The inter-band tunneling current density J_T in a p^+-n^+ junction is given in [10] as:

$$J_T(V_T) = \frac{\sqrt{2m^*}q^3 \mathcal{E} V_T}{4\pi^2\hbar^2\sqrt{E_g}} \exp\left(-\frac{4\sqrt{2m^*}E_g^{\frac{3}{2}}}{3q\mathcal{E}\hbar}\right) = \frac{\sqrt{2m^*}q^3(E_g/q+V_T)V_T}{4\pi^2\hbar^2\lambda\sqrt{E_g}} \exp\left(-\frac{4\lambda\sqrt{2m^*}E_g^{\frac{3}{2}}}{3q(E_g/q+V_T)\hbar}\right) \tag{2}$$

In this equation, m^* is the effective mass, q the elementary charge, $\mathcal{E}$ the electric field within the junction, V_T is the externally applied voltage bias across the tunneling junction and E_g is the bandgap energy. A central assumption behind (2) is that the potential barrier is triangular and therefore the electric field is constant with the value $\mathcal{E} \approx (E_g/q + V_T) / \lambda$, where λ is the width of the tunneling barrier. Since the electric field $\mathcal{E}$ contained in (2) is also a function of V_T, it appears quadratically in the leading factor of J_T and it appears reciprocally in the exponent. While the channel resistance R_{ch} of a MOSFET is constant with respect to the applied drain-source voltage in its on-state with small forward voltage drop, in the Power-TFET the on-current is non-linear and therefore at low voltage the differential on-resistance is high and drops at higher drain-source voltage bias. In fact, small current flow will already result in a sizable voltage drop across a Power-TFET. Depending on the material parameters contained in (2), it is possible that a Power-TFET can match the static current carrying capability of an equivalent MOSFET and therefore its static losses, but only within a high current density regime at operation points with low differential on-resistance.

The Power-TFET has benefits with respect to its dynamic losses. Dynamic losses arise especially from the charging and discharging of the input capacitance of the respective power device [9, p. 432]. Fig. 1 c) and f) depict the capacitive parts of the gated region of c) a Power-TFET and f) a MOSFET, respectively. The total input capacitance for the Power-TFET can be written as follows:

$$C_{in,Power\text{-}TFET} = C_{GS} + C_{GD} \tag{3}$$

C_{GS} is the source-side overlap capacitance and C_{GD} is the drain side accumulation capacitance overlapping the drift-region. For the equivalent MOSFET given here, the total input capacitance is given as follows:

$$C_{in,MOSFET} = C_{GS} + C_{GB} + C_{GD} \tag{4}$$

C_{GB} is the body capacitance containing the inversion channel. Comparing the input capacitances from (3) and (4), we can see that the overlap capacitances of the source region and the drift region are equal for equivalent MOSFET and Power-TFET devices. The MOSFET has the additional channel capacitance, which is responsible for the establishment of the inversion channel. The reduced input capacitance of the Power-TFET does improve the dynamic power loss compared to those of the MOSFET, which makes it an interesting device concept for reduced dynamic loss.

The Lateral Homo-Junction 4H-SiC Power-TFET

Device Geometry and Fabrication. To evaluate the device concept of the Power-TFET, lateral devices were implemented alongside laterally diffused MOSFETs (LDMOS) for reference on the 2 µm high-temperature CMOS platform by Fraunhofer IISB [11]. Schematic cross-sections of the two fabricated devices are shown in Fig. 1 b) and e). As substrates n-type 4H-SiC wafers are used with a 12 µm thick epitaxial layer, which is n-type doped with a concentration of 10^{15} cm^{-3}. Further doping wells and contact regions were implanted. The n^+ and p^+ doped contact regions are doped with $5{\cdot}10^{19}$ cm^{-3} respectively and the p-well forming the body of the LDMOS is doped with a concentration of 10^{17} cm^{-3}. The gate MOS electrode consists of a 55 nm thick thermally grown SiO_2 and a n^+ doped polycrystalline silicon electrode. The channel length of the LDMOS is 2 µm and the drift zone of both devices have a length of 12 µm. The gate-source and gate-drain overlap are each 1 µm respectively.

Static Electrical Characteristics. In Fig. 2 the transfer characteristics are shown at a drain-source bias of V_{DS} = 1 V. The LDMOS device shows the typical exponential subthreshold behavior with a distinct off-state at V_{GS} = 0 V and a distinct on-state at V_{GS} = 20 V spanning eleven orders of magnitude in current between off- and on-state. The Power-TFET in contrast shows the same low leakage current in off-state, but does only span six orders of magnitude if the gate is biased up to V_{GS} = 40 V. Furthermore, the Power-TFET shows a shallow and rounded transfer characteristic. The onset of the tunneling current is also shifted towards higher voltages compared to the LDMOS. Fig. 3 shows the comparison of the measured output characteristics of the Power-TFET and the reference LDMOS. The characteristics are plotted on separate current axis due to the significant difference in on-state current, such that the qualitative shape of the characteristics can be compared. Compared to the linear behavior of the LDMOS at small V_{DS}, the Power-TFET exhibits the non-linear tunneling current with an immediate onset of the tunneling current above V_{DS} = 0 V. Both devices show a saturation behavior at high V_{DS}.

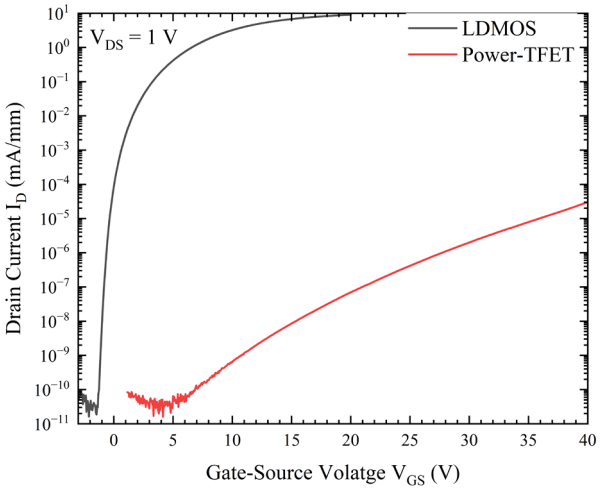

Fig. 2. Transfer characteristics of the 4H-SiC LDMOS and the 4H-SiC Power-TFET normalized on gate width.

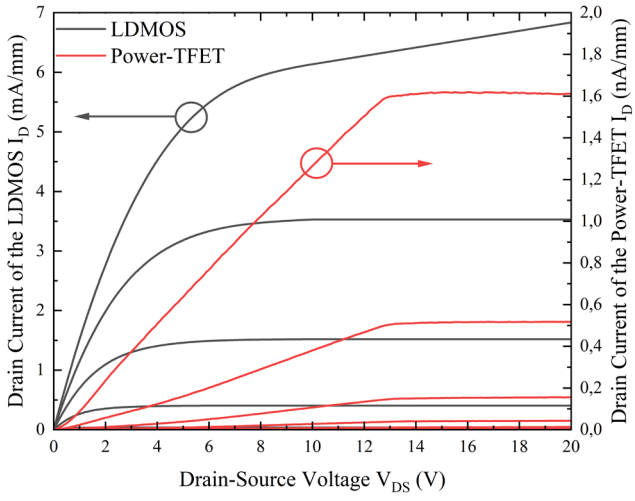

Fig. 3. Scaled output characteristics normalized on gate width of the 4H-SiC LDMOS and the 4H-SiC Power-TFET for comparison of the characteristics' shape.

The devices were also characterized with regard to their breakdown behavior, which is shown in Fig. 4. Since the devices discussed here are lateral devices that do not implement any doping structures to reduce surface electric field, the devices fail typically at the semiconductor-oxide interface and do not exploit the total breakdown capability of 4H-SiC. This also explains the variance in breakdown voltage shown in the inset in Fig. 4. Nevertheless, the devices show high-voltage capability with some Power-TFETs reaching a breakdown voltage of 600 V, beyond the capability of the LDMOS.

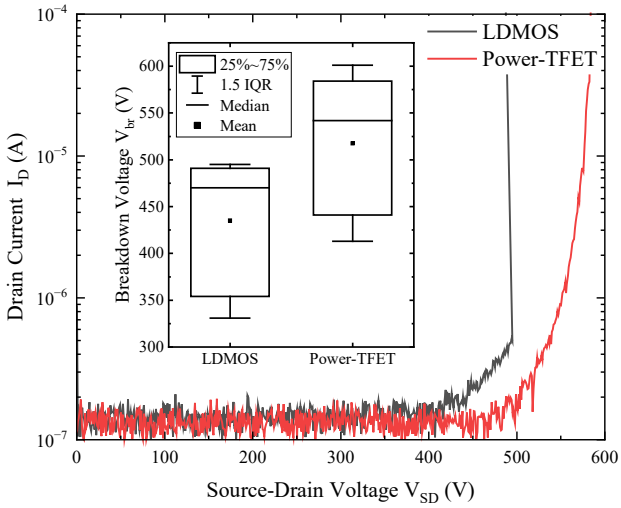

Fig. 4. Comparison of the breakdown behavior of the devices in off-state. The inset shows the distribution of breakdown voltages of LDMOS and Power-TFET.

Overall, the built devices show for the first time tunneling field-effect transistor behavior in 4H-SiC with a switched homo-junction with distinct off- and on-state and high blocking capability. Nevertheless, the on-current is too low for practical use and therefore the tunneling resistance and consequently the tunneling barrier must be optimized for the application.

Tunneling Barrier Design for Low Static Loss

Design Considerations. The output and transfer characteristics illustrate well that the tunneling resistance is eight orders of magnitude larger than the channel resistance of the equivalent LDMOS at V_{GS} = 20 V and V_{DS} = 1 V and limits the on-current to values not appropriate for the application as power device. The large tunneling resistance results almost entirely from the large bandgap energy of 4H-SiC, which the carriers must tunnel through. Equation (2) illustrates this since the bandgap energy is in the denominator of the pre-factor of the tunneling current density and in the numerator of the negative exponent of the exponential function, both leading to a lowering of the tunneling current density. Consequently, the barrier height is the parameter to optimize. In literature, TFETs for logic applications on other material systems are shown that employ heterojunctions using materials with smaller bandgap energy directly at the tunneling junction for increased current and steeper subthreshold behavior [12, 13]. In 4H-SiC heteroepitaxy is not a viable method [14] because the materials available still have large bandgaps limiting the tunneling current [15, 16]. The alternative is to use a Schottky-barrier for tunneling in the tunneling transistor [17–19]. Here the metal-semiconductor combination yields the barrier height and can be chosen quite freely and is in most cases easily manufacturable by evaporation or sputtering with optional annealing steps for alloying thereafter. Consequently, a low barrier height yields the highest tunneling current density in on-state and the lowest tunneling resistance. Low barrier height of a Schottky barrier does also introduce a lot of leakage in blocking mode through thermionic emission and Fowler-Nordheim tunneling, worsening the efficiency of the device in blocking mode and therefore increasing static loss in off-state. This leakage current has also been observed in power Schottky rectifier diodes and has been suppressed by additional structures such as in junction barrier Schottky (JBS) diodes, which

implement additional p-implanted structures underneath the Schottky contact depleting it in thermodynamic equilibrium and therefore suppressing the leakage from the Schottky barrier [20]. Implementing both, the JBS diode structure for the depletion of the Schottky barrier and a MOS gate contact adjacent to the Schottky barrier, making it switchable, keeps the low leakage in off-state while achieving a high on-current in the on-state.

Simulative Evaluation of the Switchable JBS Diode. To confirm the function of the concept a technology computer aided design (TCAD) simulation using Synopsys Sentaurus [21] was performed. The geometry of the simulated device is chosen analogous to the lateral homo-junction Power-TFET described above and 4H-SiC is chosen as semiconductor material. A schematic cross-section is shown in the inset of Fig. 5. The p^+ doped region underneath the Schottky contact is used to deplete the Schottky junction, such that the leakage is minimal. The gate is attached to the metal semiconductor junction with a distance of 1 µm from the p^+ doped region. The semiconductor is recessed at the boundary of the Schottky-junction for 100 nm, such that the electric field control of the gate on the semiconductor directly underneath the metal is optimal. For the simulation a multitude of models are used given in Tab. 1.

Table 1. Models used for the TCAD simulation of the Schottky Power-TFET and the reference LDMOS [21].

Recombination:	Shockley-Read-Hall
	Auger
	Non-local tunneling model with non-local mesh
Mobility:	Doping dependence (Massetti)
	Field dependence normal to carrier movement (Lombardi)
	High field saturation (Caughey Thomas)
Incomplete Ionization:	50% split of the shallow and deep nitrogen donor level in 4H-SiC
Material anisotropy:	Mobility
	Poisson
Interface Traps:	$5 \cdot 10^{12}$ cm^{-2} at the semiconductor-oxide interface

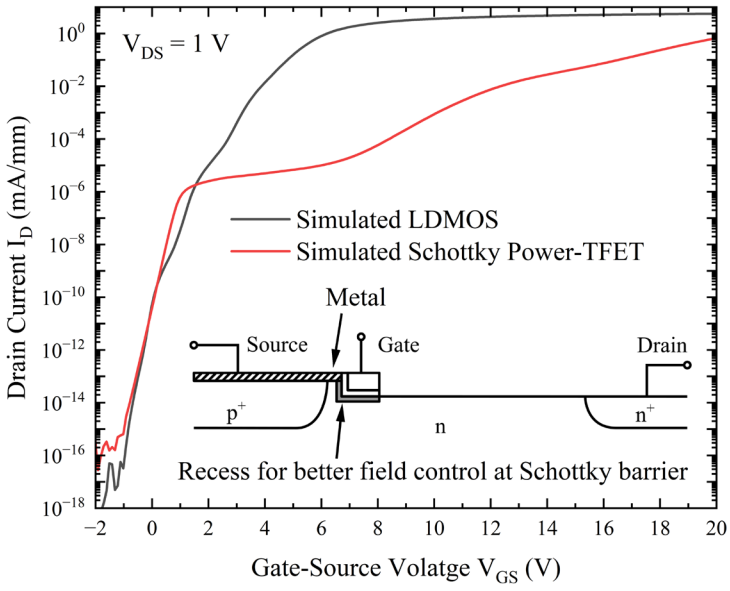

Fig. 5. Comparison of a simulated 4H-SiC LDMOS and a simulated 4H-SiC Schottky Power-TFET (cross-section shown in the inset).The channel established in the n-layer is shown in gray, which directly contacts the metal source contact. The contact potential at the Schottky junction is set to $\phi_{M\text{-}HL} = 0.6$ V.

For the Schottky barrier height between the n-layer and the metal source contact, a value of $\phi_{\text{M-HL}} = 0.6$ eV is chosen. The transfer characteristic of the device is shown in Fig. 5 and compared to a simulative representation of the abovementioned LDMOS simulated with the same models and parameters. The reference LDMOS in Fig. 2 shows overall a very similar behavior as the simulated LDMOS in Fig. 5. The values for the on-current and the onset of the subthreshold behavior fit well between simulation and measurement, hinting that the simulative results are reliable. The simulation shows the same leakage for both Schottky Power-TFET and LDMOS in off-state and at a gate bias of 20 V the Schottky Power-TFET achieves an on-current comparable to the on-current of the LDMOS. The transfer characteristic of the Schottky Power-TFET shows two distinct regions. First, a steep rise of current, which is the gate's influence on the depletion of the Schottky barrier by increasing the carrier concentration in the accumulation channel and thereby increasing the leakage at the Schottky barrier. Second, the Schottky barrier is getting thin and a significant tunneling current occurs due to the rising carrier concentration in the channel. This yields the rounded behavior of the second increase.

Conclusion

The Power-TFET promises lower dynamic loss by reduction of the input capacitance since it does not implement a gate-body capacitance compared to an equivalent MOSFET. This benefit is only useful, if the static loss of the Power-TFET is comparable to those of a MOSFET. The direct comparison of a fabricated lateral MOSFET and a Power-TFET has shown that the Power-TFET lacks eight orders of magnitude in terms of on-current due to the tunneling barrier being the bandgap of 4H-SiC. It is simulatively shown that swapping the homo-junction for a JBS diode structure, where the gate switches a Schottky barrier with low barrier height can achieve both low leakage in off-state and the required on-current.

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