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Study of Single-Event-Burnout for Refilled-PMOS SiC Trench MOSFET

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Abstract. This study proposes a refilled PMOS SiC trench MOSFET (RPTMOS) design with integrated parasitic PMOS clamping transistors to mitigate single-event burnout (SEB) susceptibility. The configuration of the core epi-refill process to realize the proposed RPTMOS is also demonstrated. Through systematic TCAD simulations, we analyze the transient lattice temperature, electric field distribution, and current density dynamics under heavy-ion irradiation (LET = 19.0 MeV·cm²/mg, Drain DC Bias V_D = 500 V). The optimized structure features a grounded parasitic PMOS clamp formed by the P-connect, P-bottom, and N-drift regions, which enables efficient hole extraction and suppresses electric field crowding at the gate oxide corner. Comparative simulations reveal that the proposed design reduces peak lattice temperatures and elevates the SEB withstand voltage by ~20%. Parametric studies further demonstrate that increasing the P-connect thickness (200 Å → 400 Å) significantly enhance radiation hardness, proves the pivotal contribution from the parasitic PMOS. The findings offering a viable pathway for radiation-hardened SiC power devices in aerospace and high-energy applications.

Introduction

SiC MOSFET are very attractive for irradiated power electronics applications[1]. One of the biggest threat to the SiC MOSFET operated under irradiation is the single-event-burnout (SEB) effect, which can cause permanent damage due to the incidence of high-energy particles. These particles generate electron and hole pairs along the incident path leading to local electrical field spike and serious thermal effect. Since the generated electrons could be drifted by the high drain bias, pumping out the holes in time become the critical reinforcement strategy to avoid SEB.

Many technologies have been developed to improve the anti-SEB capability. For instance, the N+N- junction within the deep P+ well of CoolSiC trench MOSFET to assist the hole extraction[2], adoption of semi-Superjunction[3], multi-buffer and multi-shield below p-well[4,5,6].

In this work, we proposed a refilled PMOS SiC trench MOSFET (RPTMOS), which protects the gate oxide[7] and help to pump out the irradiation-generated holes by the parasitic PMOS. The parasitic PMOSs are formed by a epi-refill process, which controls the flow rate of hydrogen chloride (HCl) gas during the trench re-fill process and grow a thin p-type region (p-connect) on the side walls of trench. TCAD characterization reveals that the lateral thickness of the p-connect region should be maintained below 400Å to achieve lower MOSFET on-resistance (Rds,on)[7]. We characterized the lattice temperature, electric field and current density etc. under heavy-ion strike with certain values of particle linear energy transfer (LET) and discovered that the parasitic PMOS plays a pivotal role during the SEB process.

Device Structure and Process

Fabrication of the device follows our prior work [7], with key steps shown in Fig.1. Fig.1 shows the main steps of realizing the RPTMOS.

As shown in Fig.1(a), from bottom to top, the epi-structure contains n+ substrate, n-buffer, n-epi (drift) layer, p-well layer, n+ source layer. The trench orientation in Fig.1(b), directed towards the reader, is aligned to the [11-20] crystal direction, with a deviation smaller than 0.2°.

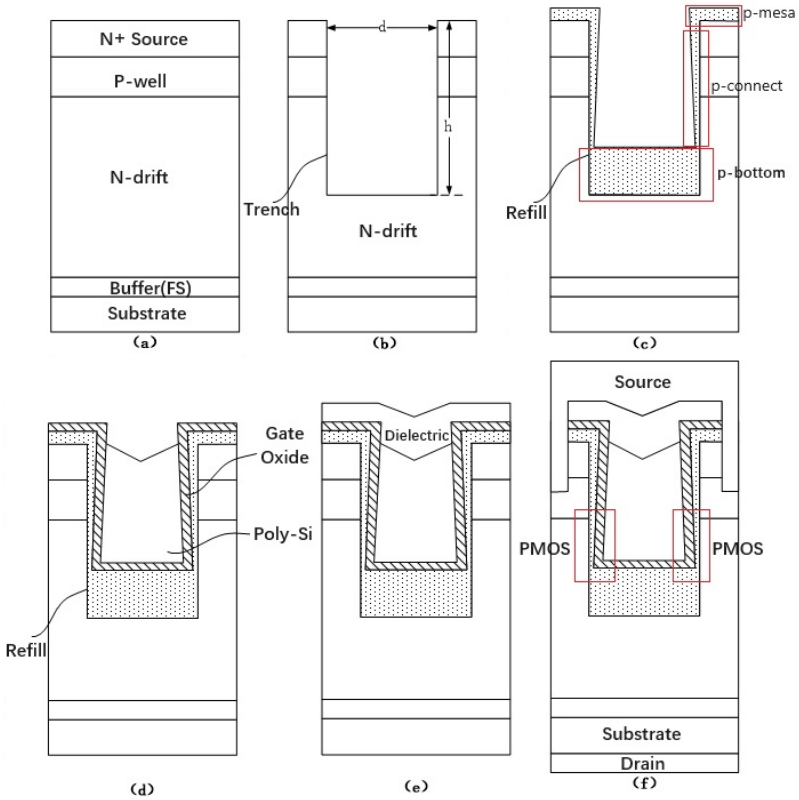

Fig. 1. The fabrication process of the RPTMOS.

The p-type epilayer is refilled in SiC trench, which can achieve a very thin layer (<0.1μm) above the sidewalls of n-type trench[8] as shown in Fig.1(c), The addition of hydrogen chloride is to have a certain etching effect on the trench sidewall [9,10,11]. The final structure of the device is as shown in Fig.1(f) [7,11], the parasitic PMOS is labeled within the red rectangle.

SEB TCAD Simulation RESULT

TCAD simulation was carried out to investigate the RPTMOS's performance under high-energy particle irradiation. For trench-gate devices, the region adjacent to the gate oxide represents the most vulnerable area in trench-gate MOSFET[4]. The conditions depicted in Fig.2 correspond to vertical heavy-ion irradiation at x = 5.0 μm of the trench-gate device, where x = 5.0 μm marks the boundary layer between the SiC P-connect region and the gate oxide. The standardized SEB irradiation parameters: B.DENSITY (electron-hole pair generation density) = 1×10^{20} cm^{-3} and radius = 0.05 μm. This yields a linear energy transfer (LET) value of 0.126 pC/μm, which equates to 19.0 MeV·cm^2/mg[2]. Our study adopts this LET value (19.0 MeV·cm^2/mg) for TCAD simulations of SEB. The SEB LET threshold for 1200V SiC MOSFETs is approximately 10 MeV·cm^2/mg[12], thereby justifying the selection of 19.0 MeV·cm^2/mg here as a conservative yet representative value for SEB.

About the RPTMOS, during reverse blocking operation, the parasitic PMOS inherently clamps the electrical potential of the p-bottom region. Under reverse blocking conditions, the P-bottom, N-drift, and P-well regions collectively form an equivalent PMOS clamping transistor. With the polysilicon gate grounded, the elevated potential in the N-drift region beneath the P-well activates the PMOS clamp, with the p-connect region as a hole provider. The parasitic PMOS act as an accumulation-mode PMOS[7].

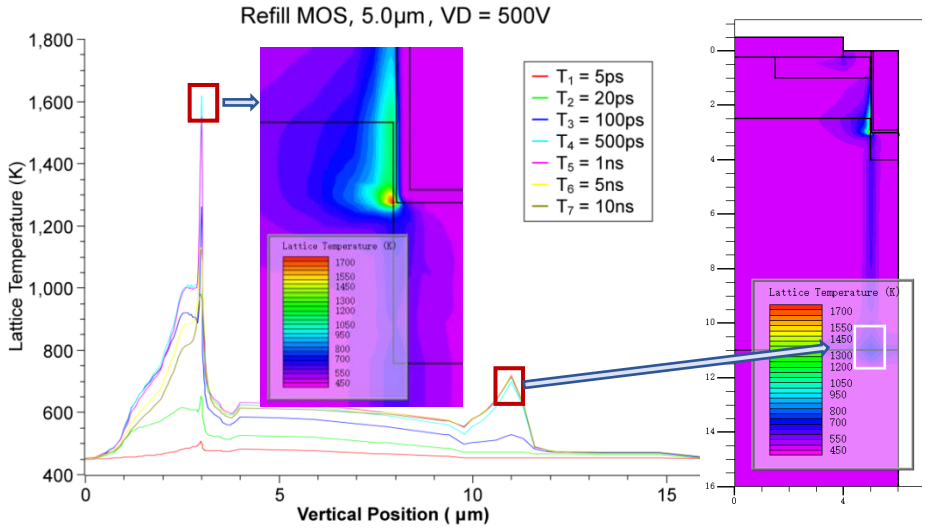

Fig. 2. The vertical distribution of the lattice temperature of the RPTMOS along x = 4.99 μm under heavy-ion irradiation at x = 5.0 μm at different transient time steps T_1 - T_7. The arrows point to the lattice temperature distribution within the RPTMOS.

The vertical axis of Lattice Temperature in Fig.2 illustrates the transient lattice temperature distribution along the vertical y-axis at x = 4.99 μm (corresponding to the central axis of the P-connect region that spans a lateral width of 200 Å) across distinct time points (T_1–T_7). Under drain bias of V_D = 500 V, the first temperature peak emerges at y = 3.0 μm. The embedded subplots (left: magnified lattice temperature distribution near the gate oxide corner at T_4 = 500 ps; right: global lattice temperature distribution of the RPTMOS) reveal that this peak lattice temperature corresponds to the interface between the P-connect region and the P-bottom region in Fig.1(c). Between T_4 = 500 ps and T_5 = 1 ns, the localized peak lattice temperature at this region exceeds 1500 K. Subsequently, in Fig.2, a secondary temperature peak emerges at y = 11.0 μm, occurring between T_4 = 500 ps and T_7 = 10 ns after heavy-ion irradiation. This peak corresponds to the temperature spike at the n^+/n^- junction between the N-drift region and the substrate. Many studies propose multilayer buffer structures to suppress this localized temperature rise[4,5,6].

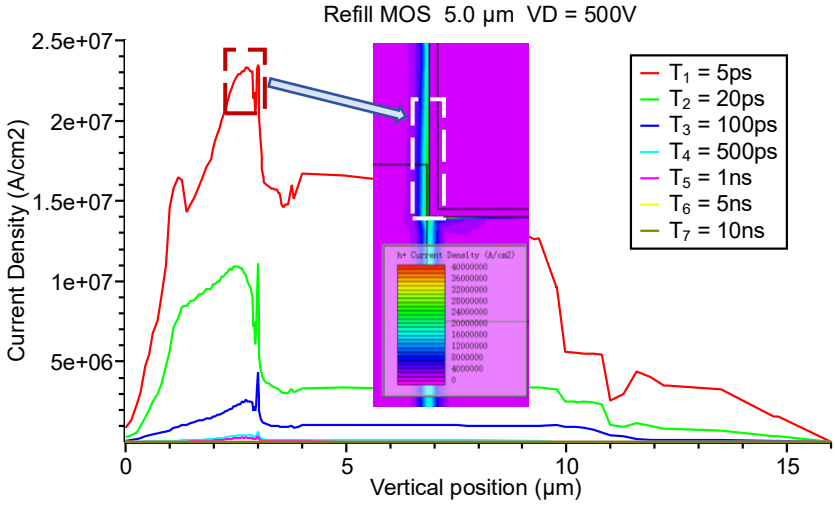

Fig. 3. The figure illustrates the current density distribution along x = 4.99 μm of the RPTMOS under vertical heavy-ion irradiation at x = 5.0 μm and drain voltage of V_D = 500 V at different transient time steps T_1 - T_7.

Fig.3 illustrates the current density distribution along the longitudinal tangent at x = 4.99 μm for the trench-gate device under vertical heavy-ion irradiation at x = 5.0 μm and a drain voltage of V_D = 500 V. At T_1 = 5 ps, the hole current density reaches its maximum value near y=2.0 μm to 3.0 μm(marked by the white dotted box), predominantly discharged through the parasitic equivalent

PMOS clamping transistor. The inset subplot depicts the spatial hole current density distribution, demonstrating that the hole current constitutes the dominant component (>2e+07A/cm^2) of the ion-induced current density at this stage.

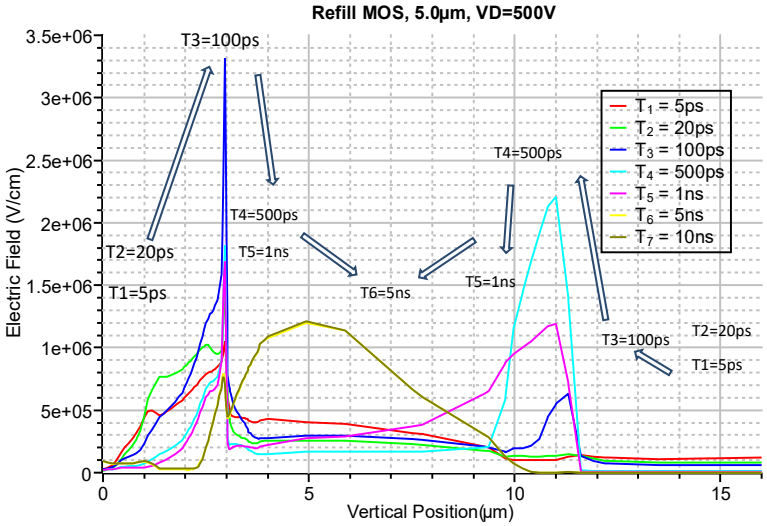

Fig. 4. The figure presents the electric field intensity distribution along x = 4.99 μm of the RPTMOS under vertical heavy-ion irradiation at x = 5.0 μm and drain voltage of V_D = 500 V at different transient time steps T_1 - T_7. The arrows indicates the evolution of local peak electric field intensity vs. each transient time steps T_1 - T_7.

Fig.4 presents the electric field intensity distribution along x = 4.99 μm for the trench-gate device under vertical heavy-ion irradiation at x = 5.0 μm and a drain voltage of V_D = 500 V. The arrows annotates the shift of the position of peak electric field intensity at different transient time steps T_1 - T_7 within the RPTMOS at following heavy-ion irradiation. At T_3 = 100 ps, the peak electric field (3.3 MV/cm) localizes at y = 3.0 μm(near the trench-gate bottom corner), accompanied by a mild electric field crowding (~0.6 MV/cm) near y = 11 μm(n^+/n^- junction).

The peak electric field at y = 3.0 μm arises from the requirement for charge neutrality within the semiconductor. Specifically, heavy-ion irradiation induces localized lattice temperature elevation and generates a high density of electron-hole pairs. In the absence of the equivalent PMOS clamping transistor, holes accumulate at the gate oxide corner due to the lack of an efficient extraction path. Concurrently, electrons are retained to satisfy charge neutrality, leading to increased plasma density. This disrupts the space-charge region's shielding effect, resulting in electric field peaking at y = 3.0 μm (the trench-gate bottom corner). Under these conditions, the combined effects of reduced critical breakdown field strength of the gate oxide at elevated temperatures and the high applied drain voltage render the gate oxide corner susceptible to dielectric breakdown due to severe electric field crowding.

In the RPTMOS proposed herein, the grounded equivalent PMOS clamping transistor integrated into the trench sidewall enables rapid extraction of excess holes. Furthermore, by reducing the electron concentration at the conduction band edge to maintain charge neutrality, part of the space-charge shielding of the p-doping region is preserved, mitigating field crowding and suppressing rapid junction temperature escalation.

Simulation RESULT Discussions

A comparative analysis of the transient distributions of lattice temperature, current density, and electric field along x = 4.99 μm under vertical 19.0 MeV·cm²/mg heavy-ion irradiation in Fig.2-4(vertical radiation incidence at x = 5.0 μm, V_D = 500 V) reveals the following:

At T_1–T_3, the y = 3.0 μm vicinity first exhibits a current density peak of 2.3×10^7 A/cm² at T_1 = 5 ps. This peak spans a broad y-axis range (y = 1.0–3.0 μm), coinciding with the equivalent PMOS clamping transistor and P-well regions. By T_2 = 20 ps, the current density peak declines to

1.1×10^7 A/cm². At T_3 = 100 ps, the current density peak further diminishes to ~4×10^6 A/cm², representing an approximate order-of-magnitude reduction compared to T_1. Concurrent observation of the lattice temperature profile shows that the peak temperature rises from ~500 K at T_1 to ~650 K at T_2 and further to 1260 K at T_3. This decline in current density between T_1 and T_3 can be attributed to the increasing localized temperature near y = 3.0 μm, which elevates the resistance of the equivalent PMOS clamping transistor, thereby suppressing hole extraction efficiency. The T_3 time point coincides with the transient electric field intensity curve reaching its extreme at y = 3.0 μm. This result arises from the high transient hole density coupled with inefficient extraction of the PMOS, which weakens the space-charge region's protective effect on the gate oxide corner. Beyond T_3, the peak temperature near y = 3.0 μm gradually decreases, primarily due to external thermal dissipation (simulated with a thermal conductivity coefficient α = 1 W/cm·K). As the heavy-ion irradiation is a single-event process with a Gaussian temporal charge generation profile (width T_c = 2 ps), the massive hole extraction process concludes after T_3. Consequently, the space-charge shielding effect is gradually restored, leading to reduced electric field peaking at y = 3.0 μm and a further temperature decline to ~970 K by T_7 = 10 ns.

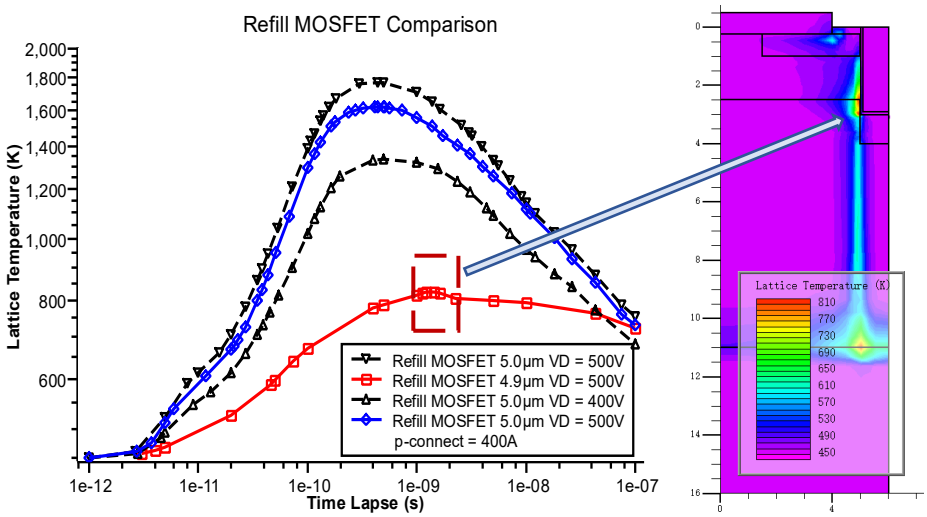

Fig. 5. Comparison of the temporal evolution(horizontal axis) of the SiC peak temperature(vertical axis) of the RPTMOS(labeled as refill MOSFET) throughout the irradiation process under different heavy-ion incidence conditions and structural parameters.

Furthermore, we compare the temporal evolution of the SiC peak temperature throughout the heavy-ion irradiation process in Fig.5. The black inverted-triangle curve in Fig.5 corresponds to the aforementioned scenario (vertical 19.0 MeV·cm²/mg ion strike at x = 5.0 μm, incident at the gate oxide/SiC interface, V_D = 500 V), where the device peak temperature reaches 1770 K. As analyzed earlier, the limited lateral width (200 Å along the x-axis) of the equivalent PMOS clamping transistor introduces current-limiting effects under elevated lattice temperatures, reducing hole extraction efficiency and weakening field shielding. Therefore, the blue diamond-shaped curve in Fig.5 corresponds to a P-connect x-axis thickness increased from 200 Å to 400 Å under V_D = 500 V, yielding a peak temperature of 1616 K—significantly lower than the 200 Å case 1770K. This demonstrates that increasing the P-connect thickness enhances the device's radiation hardness, on the other hand, the thicker P-connect thickness suppresses the Rds,on, which is a trade-off. The black upright-triangle curve represents identical ion strike parameters compared to the black inverted-triangle curve with V_D reduced to 400 V, resulting in a lower peak temperature 1336 K.

In Fig.5, the red square-shaped curve represents a scenario where the ion strike is offset by 100 nm from the gate oxide/semiconductor interface x = 5.0 μm to x = 4.9 μm, leads the peak temperature decreases to 824.6 K. This results validates that the gate oxide/semiconductor interface is the most SEB-sensitive region of SiC Trench MOSFET[2]. Under this condition, the RPTMOS(labeled as refill MOSFET in Fig.5) attains its peak temperature around T_5 = 1ns. The right-side inset subplot in Fig.5 depicts the lattice temperature distribution of the RPTMOS at T_5 = 1 ns.

Apart from the peak temperature at the n^+/n^- junction between the substrate and N-drift region, two additional hot-spots localize at the source and drain terminals of the parasitic PMOS clamping transistor is observed(pointed by arrow). It can be inferred that even for an ion strike's incident position offset to x = 4.9 μm, the parasitic PMOS clamping transistor retains significant charge extraction capability for ion-generated electron-hole pairs compared to the main p-n junction formed by p-well and n-drift region in RPTMOS.

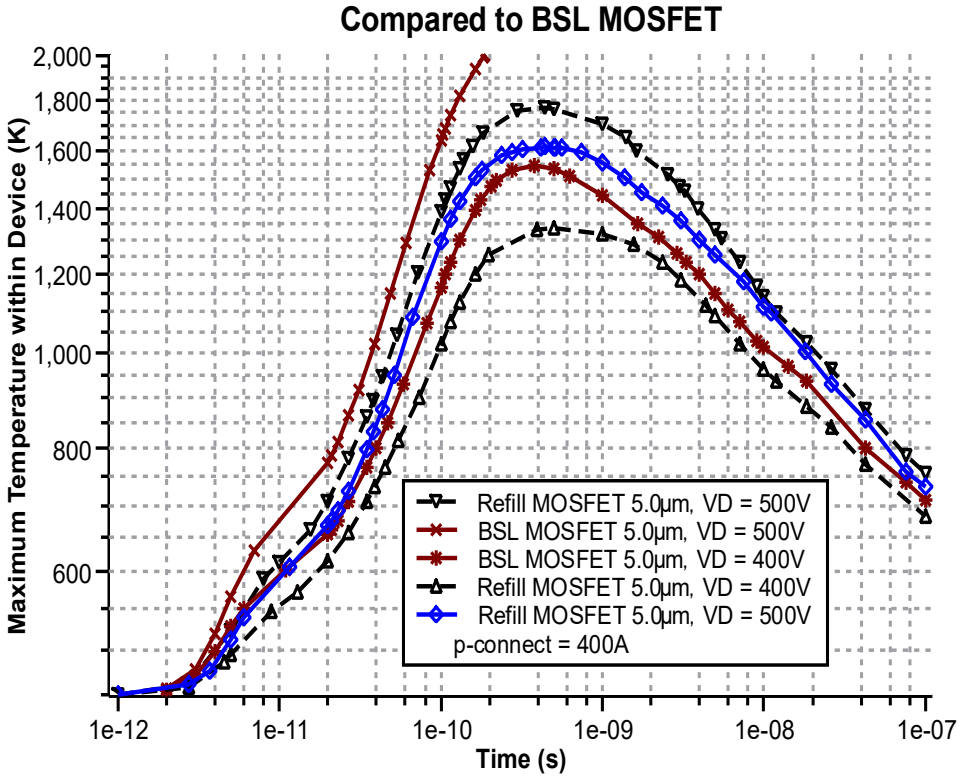

Fig. 6. Comparison of the temporal evolution(horizontal axis) of the SiC peak temperature(vertical axis) throughout the heavy-ion irradiation process between the RPTMOS(labeled as refill MOSFET) with baseline (BSL) SiC trench MOSFET(lacking the equivalent PMOS clamping transistor). The proposed RPTMOS design with P-connect thickness along the x-axis increased from 200 Å to 400 Å.

Finally, we compare the temporal evolution of the SiC peak temperature throughout the heavy-ion irradiation process between the proposed RPTMOS(labeled as refill MOSFET in Fig.6) design with a baseline (BSL), lacking the equivalent PMOS clamping transistor, SiC trench MOSFET(labeled as BSL MOSFET in Fig.6) in Fig.6. Both devices share identical critical dimensions and doping profiles. In Fig.6, the brown cross-shaped curve represents the BSL MOSFET under vertical 19.0 MeV·cm²/mg irradiation (x = 5.0 μm, V_D = 500 V), exhibiting a peak temperature exceeding 2000 K, higher than the RPTMOS. Furthermore, the brown asterisk-shaped curve corresponds to the BSL MOSFET under V_D = 400 V, yielding a peak temperature of 1548 K, still higher than the RPTMOS under identical conditions. For the RPTMOS, the SEB withstand voltage is improved by approximately 20%.

New SIC MOSFET Structure and Experimental Results

Fig.7 propose a novel SiC trench MOSFET structure[13]. Fig.7(b) provides a top-down perspective of the proposed SiC trench MOSFET structure corresponds to the B-B' horizontal cross-section of Fig.7(a) and 7(c). Regions with identical colors or patterns in Fig.7(a), 7(b), and 7(c) represent the same material compositions within the device.

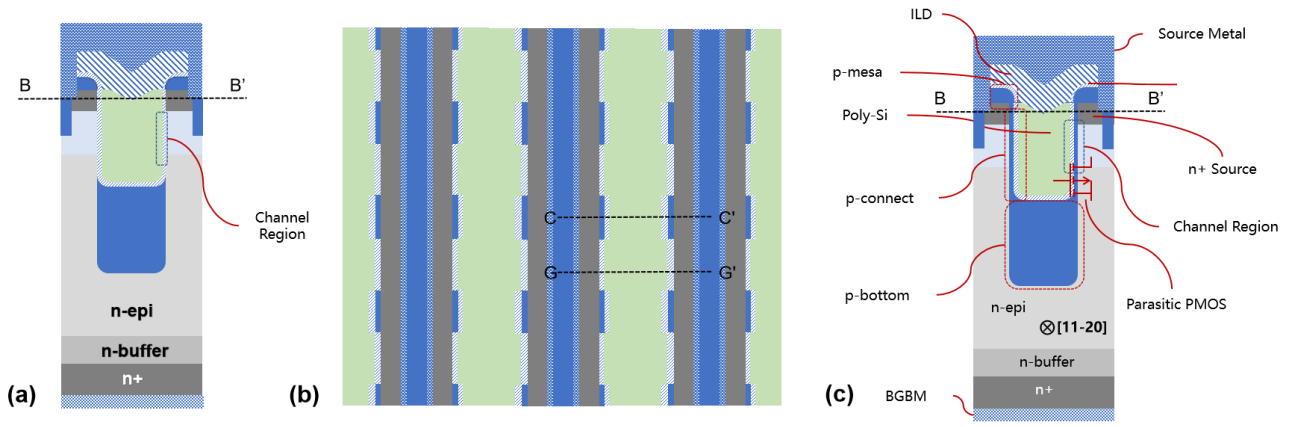

Fig. 7. This figure ilustrates a novel SiC trench MOSFET structure.

Compared to the previously described RPTMOS[7], an additional process step is introduced in the fabrication process shown in Fig.1(c): periodic selective regions along the trench direction are defined. As shown near the G-G' location in Fig.7(b)(top-down perspective of the new SiC MOSFET), an isotropic SiC etching process is applied to remove the thin p-connect region in this area, thereby forming a low on-resistance zone in the new SiC MOSFET.

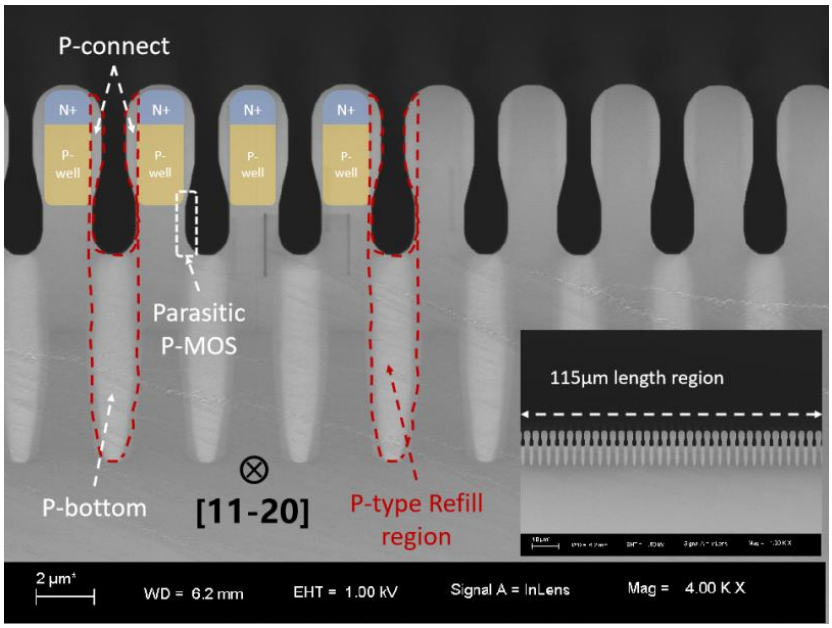

Fig. 8. SEM figure of the core epi-refill process from Fig.1(b) to Fig.1(c).

Moreover, we have successfully demonstrated the core epi-refill process from the structure in Fig. 1(b) to that in Fig. 1(c) using an 8-inch SiC wafer in our in-house 8-inch pilot line, as illustrated in Fig. 8. It is shown that a thin p-channel for the accumulation-mode p-MOS can be effectively fabricated through p-type epi-refill. By adjusting the HCl flow rate (optimum condition HCl:SiH_4 ~ 20), we achieved the required process conditions to realize the configuration demanded by RPTMOS device. The trench aspect ratio was set at 13.0 μm : 1.6 μm, with the trench direction (into the paper) aligned along the [11-20] crystal orientation, maintaining a misalignment of less than 0.2°. The configuration of the n+ source contact and the p-well in the proposed RPTMOS is also depicted in Fig. 8. Additionally, the subfigure in Fig. 8 confirms that the epi-refill process enables a relatively uniform distribution across the wafer.

Summary

This work demonstrates that integrating a parasitic PMOS clamping transistor into RPTMOS effectively mitigates SEB vulnerability by enhancing hole extraction and reducing field crowding. The parasitic PMOS clamp rapidly discharges ion-generated holes, preserving space-charge shielding and limiting peak electric fields at the gate oxide corner. Peak lattice temperatures near critical junctions (e.g., P-connect/P-bottom interface) are reduced by >230 K in the RPTMOS under 500 V drain DC bias, achieves a 20% higher SEB voltage than baseline MOSFET, highlighting its superiority in radiation-hardened applications. Furthermore, increasing the P-connect thickness (400 Å) lowers peak temperatures by around 10 %, validating design flexibility and the pivotal contribution from the parasitic PMOS. Furthermore, we propose a novel SiC trench MOSFET structure with periodical epi-refilled p-connect structure, to better leverage the design advantages of RPTMOS. In addition, we successfully demonstrated the configuration of the core epi-refill process to realize the proposed RPTMOS.

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