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Benchmark Study of State-of-the-Art Commercial 1200V SiC MOSFETs for Automotive Applications

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Abstract. A comparative study of state-of-the-art commercial 1200V trench-gate, planar-gate, and trench-assisted planar Silicon Carbide (SiC) MOSFETs is presented. The experimental study mainly focuses on disclosing the static and robustness characteristics of distinct SiC technologies targeting automotive applications under room and high temperatures. The benchmark study of static characteristics covers specific on-resistance ($R_{ON,SP}$), gate leakage (I_{GSS}), drain leakage (I_{DSS}), breakdown voltage (BV_{DSS}), and drain-induced barrier lowering (DIBL) effects. The avalanche robustness is investigated by the unclamping inductive switching (UIS) setup under 25 °C and 175 °C while the single-pulse and repetitive short-circuit capability is evaluated under hard switching fault (HSF) under 25 °C.

Introduction

Silicon carbide (SiC) power MOSFETs are promising switches for high-voltage, high-power, high-frequency, and high-temperature applications to replace legacy Silicon counterparts in existing applications, owing to wide bandgap, high breakdown electric field, and excellent thermal conductivity [1]. The adoption of 1200V SiC MOSFETs into electric vehicles (EV) is increasingly popular because the superior efficiency, high power density, high-temperature operating capability, and faster switching speed contribute to longer driving range, shorter charging time, and more compact system design.

For automotive applications, the most important parameters of SiC power devices are lower on-resistance to minimize the conduction losses, faster switching speeds to decrease the switching losses, high breakdown voltage to handle the high-voltage architecture, and wide operating temperature range to withstand harsh engine compartment conditions, contributing to the improved efficiency. In addition, the SiC power MOSFETs used for automotive applications can experience high voltage spikes and potential short circuits during motor control and power conversion, and their ability to withstand these events directly impacts the reliability and safety of the system, especially in demanding situations like rapid acceleration or sudden braking where large current surges can occur. The SiC MOSFETs with poor avalanche or short-circuit robustness could fail permanently, leading to system malfunction or even damage to other components.

Multiple manufacturers have released their latest generation of 1200V silicon carbide (SiC) MOSFETs, which are qualified to AEC-Q101 standards for demanding automotive applications. These components are specifically designed to meet the requirements of high-power systems such as on-board chargers (OBCs), traction inverters, and e-compressor inverters [2]. These commercial 1200V SiC MOSFETs adopt planar-gate, trench-gate, and trench-assisted planar technologies with their unique benefits and weaknesses as discussed in [3] and [4]. There are very limited studies making comprehensive benchmark between the state-of-the-art 1200V SiC MOSFETs oriented towards automotive applications. However, the comparative study of various 1200V SiC technologies

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are valuable for the researchers and engineers in the field when understanding the device performance and choosing the most suitable SiC power devices for their applications.

In this work, the static and robust characteristics of commercial 1200V trench-gate, planar-gate, and trench-assisted planar SiC MOSFETs from five mainstream manufacturers are characterized with side-by-side comparison.

Results and Discussion

Table 1 summarizes the key information for the devices under test (DUTs). We selected the latest generation trench-gate SiC MOSFETs from two manufacturers: Manufacturer A (asymmetric trench technology) and Manufacturer B (double trench technology). We also included the latest generation trench-assisted planar SiC MOSFETs from Navitas, and the latest generation planar SiC MOSFETs from two other distinct manufacturers, D and E. The blocking voltage rating is 1200V for all DUTs.

The current rating is extracted from the datasheets and used for on-resistance ($R_{DS,ON}$) test. To make fair comparison, the active areas of DUTs are extracted by optical measurement after decapsulation. Trench-gate silicon carbide (SiC) MOSFETs exhibit a high static threshold voltage ($V_{GS,TH}$) of 4.2–4.3V at room temperature, while planar-gate SiC MOSFETs have a lower V_{TH} of 2.6–2.7V. This difference is due to the different crystal faces used: trench-gate devices are built on the a-face, which has a lower interface trap density, leading to higher channel mobility and a larger $V_{GS,TH}$ [5]. Owing to the benefits of high $V_{GS,TH}$, the trench-gate SiC MOSFETs can be driven using 0V gate turn-off voltage ($V_{GS,OFF}$) while planar-gate SiC MOSFETs recommend a negative $V_{GS,OFF}$ to avoid false turn-on. The trench-gate technologies show a higher temperature coefficient.

Table 1 also shows that trench-assisted planar technology offers several advantages over traditional planar technology, including lower $R_{ON,SP}$, Q_{GD} , $Q_{GD} \times R_{ON,SP}$. While trench-gate technology offers a lower $R_{ON,SP}$, the trench-assisted planar technology delivers a superior FOM (Figure of Merit) considering both BV_{DSS} and $R_{ON,SP}$ ($B_{VDSS}^2/ R_{ON,SP}$). Its performance surpasses that of planar-gate technology and is slightly inferior to trench-gate technology. The Q_{GD} and Q_{GD} x $R_{ON,SP}$

Table 1. Key information of devices under test from different manufacturers.

Manufacturer	**A**	**B**	**Navitas**	**D**	**E**
Technology	Asymmetric Trench	Double Trench	Trench-assisted Planar	Planar	Planar
Generation	Gen 2	Gen 4	Gen 4	Gen 3	Gen 4
Voltage Rating (V)	1200	1200	1200	1200	1200
$V_{GS,th}$ (V) *	4.3	4.2	2.6	2.7	2.6
BV_{DSS} (V) at V_{GS} = 0V *	1486	1550	1696	1532	1609
Current Rating (A)	56.7	42	70	74	84.3
$R_{DS,ON}$ (mΩ) at 25°C	12.2	18	12.5	14	13
$R_{ON,SP}$ (mΩ·cm²) at 25°C	1.9	2.4	2.6	3.3	3
$R_{DS,ON}$ (mΩ) at 175°C	28.9	43.1	25	29	23
Temperature coefficient	2.15	2.40	2.07	2.11	1.94
$BV_{DSS}^2/ R_{ON,SP}$	1.16E+06	1.00E+06	1.11E+06	7.11E+05	8.63E+05
Q_{GD} (nC)	34	52	82	98	102
Q_{GD} x $R_{ON,SP}$ (nC·mΩ·cm²)	64.6	124.8	213.2	323.4	306
$V_{GS,ON}$ / $V_{GS,OFF}$ (V)	+18/0	+18/0	+18/-5	+18/-3	+15/-4

Notes: 1. Gate technology, generation, voltage rating, current rating, $R_{DS,ON}$, Q_{GD} and $V_{GS,ON}$ /$V_{GS,OFF}$ are from the application notes or datasheets of the manufacturers. 2. All other parameters with * label are based on the average values of 5 samples tested at room temperature.

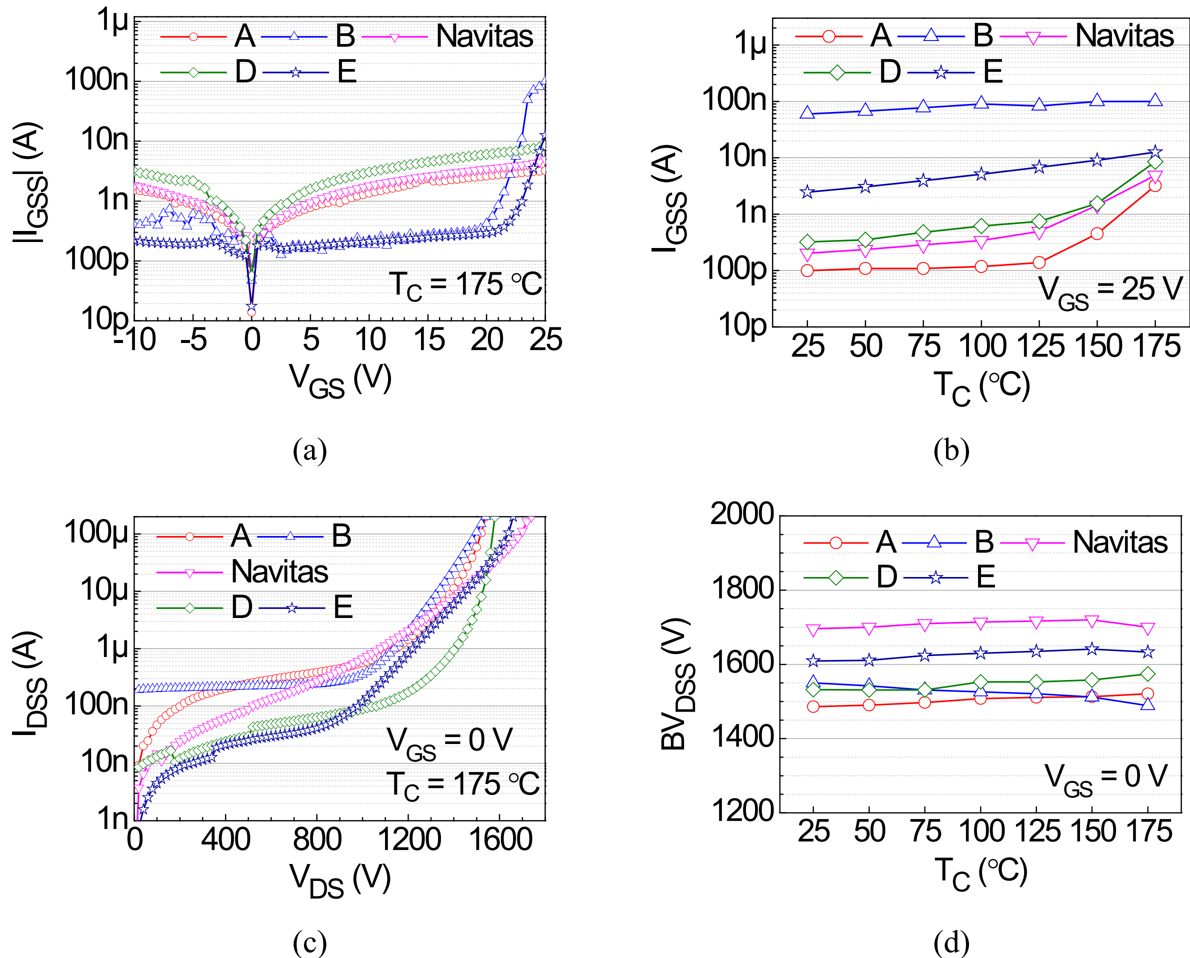


Fig. 1. (a) I_{GSS}–V_{GS} curves under V_{DS} = 0V, T_C = 175 °C, (b) I_{GSS} at V_{GS} = 25 V with T_C from 25 °C to 175 °C. (c) I_{DSS}–V_{DS} curves under V_{GS} = 0V, T_C = 175 °C, (b) breakdown voltage, BV_{DSS}, is defined at I_{DSS} = 100 μA and extracted from I_{DSS}-V_{DS} curves at T_C from 25 °C to 175 °C.

of planar-gate technology is obviously inferior to trench-gate technology, while that of trench-assisted planar-gate technology is better than pure planar-gate devices.

Gate leakage (I_{GSS}) and drain leakage (I_{DSS}) are critical parameters for device reliability. As depicted in Fig. 1, the device from Manufacturer B demonstrated a significantly higher I_{GSS} at elevated temperatures compared to the other manufacturers. The device from Manufacturer E presented a high I_{GSS} at V_{GS} = 25 V and T_C = 175 °C, which is attributed to utilizing a thinner gate oxide [6] and corresponds to a lower $V_{GS,ON}$ of 15 V in Table I. Furthermore, Manufacturer B also exhibited higher I_{DSS} at low drain-source voltages, and a noticeable reduction in breakdown voltage (BV_{DSS}) with increasing temperature. In contrast, the device from Navitas showed a robust BV_{DSS} greater than 1700 V, indicating excellent immunity to high-voltage spikes.

The drain-induced barrier lowering (DIBL) effect, which influences the threshold voltage ($V_{GS,TH}$), was also analyzed. The DIBL coefficient (ΔV_{TH_DIBL}) was defined as the change in $V_{GS,TH}$ as the drain-source voltage (V_{DS}) increased from 3 V to 1200 V. As illustrated in Fig. 2, Manufacturer A's trench-gate device, despite having the highest initial $V_{GS,TH}$, exhibited the largest reduction in $V_{GS,TH}$ across the tested voltage range. This figure also demonstrates that the other manufacturers show better control over threshold voltage stability at different voltages and temperatures.

The avalanche capability of the device under test (DUT) was characterized by using an unclamping inductive switching (UIS) setup in [7]. As shown in Fig. 3, a 1.0 mH inductor was utilized, and the inductor current was increased incrementally by approximately 1 A per step until either destructive or parametric failure was observed. The maximum current achieved just before failure was documented as the single-pulse avalanche current, designated as $I_{ds,pk}$.

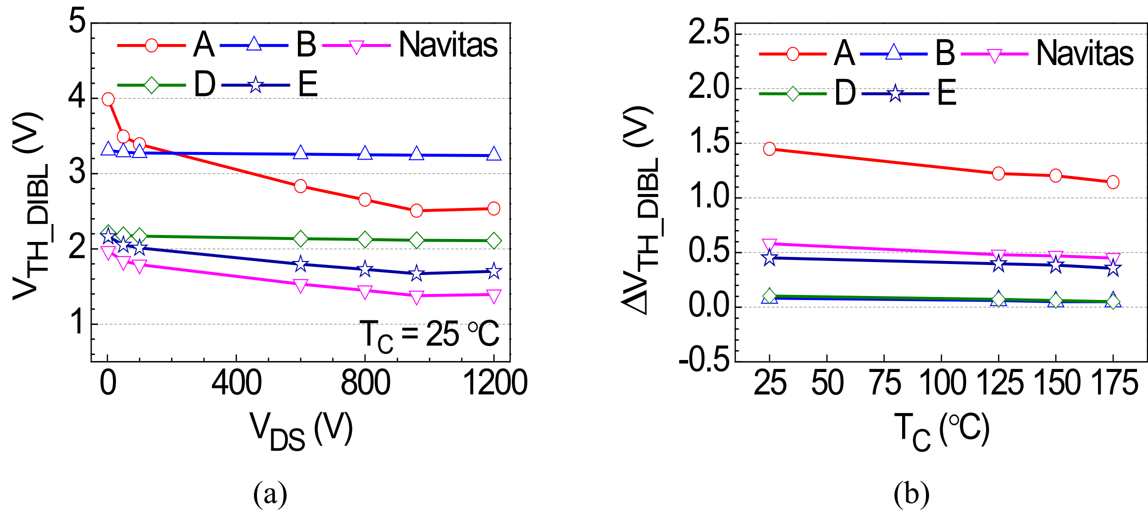


Fig. 2. (a) Threshold voltage measured under different V_{DS}, V_{TH_DIBL}, at I_{DS} = 2.5 mA at T_C = 25 °C. (b) ΔV_{TH_DIBL} at I_{DS} = 2.5 mA with V_{DS} from 3 V to 1200 V under T_C = 25 °C, 125 °C, 150 °C, 175 °C.

Fig. 4 presents the normalized avalanche energy density (E_{AS}/Active Area) and the normalized avalanche current density ($I_{ds,pk}$/Active Area) for all DUTs at a junction temperature of 175 °C. The data indicates that the planar-gate and trench-assisted planar devices exhibited a superior energy handling capability per unit area compared to the trench-based devices, suggesting a more effective structural design for dissipating avalanche energy. This trend of greater robustness in planar devices is further supported by the data in Fig. 5, which illustrates the percentage change in these normalized parameters from 25 °C to 175 °C. The planar-gate and trench-assisted planar devices demonstrated a smaller reduction in avalanche energy and current density at elevated temperatures compared to the trench-gate devices. Notably, Manufacturer B, a double-trench MOSFET, showed the poorest avalanche performance among all tested technologies, suggesting a potential weakness in shielding at the bottom or corner of the gate trench.

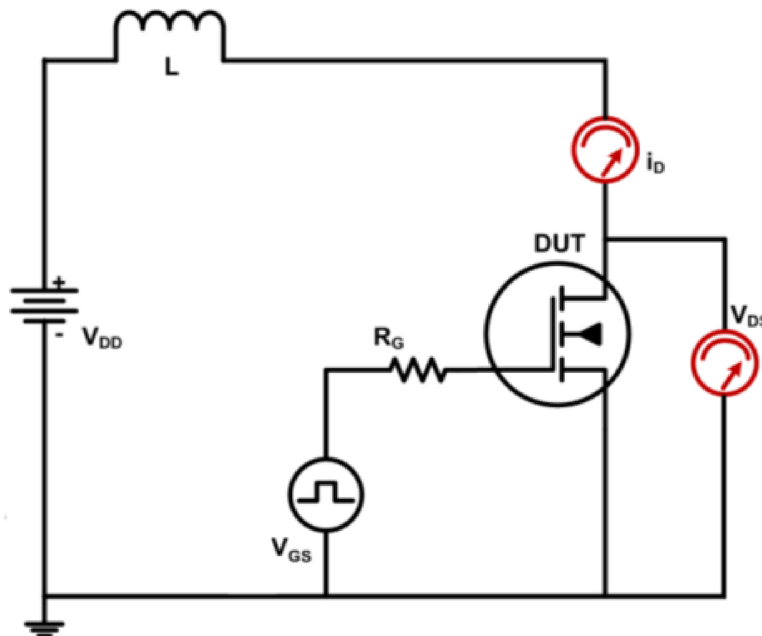


Fig. 3. UIS test circuit schematic [5].

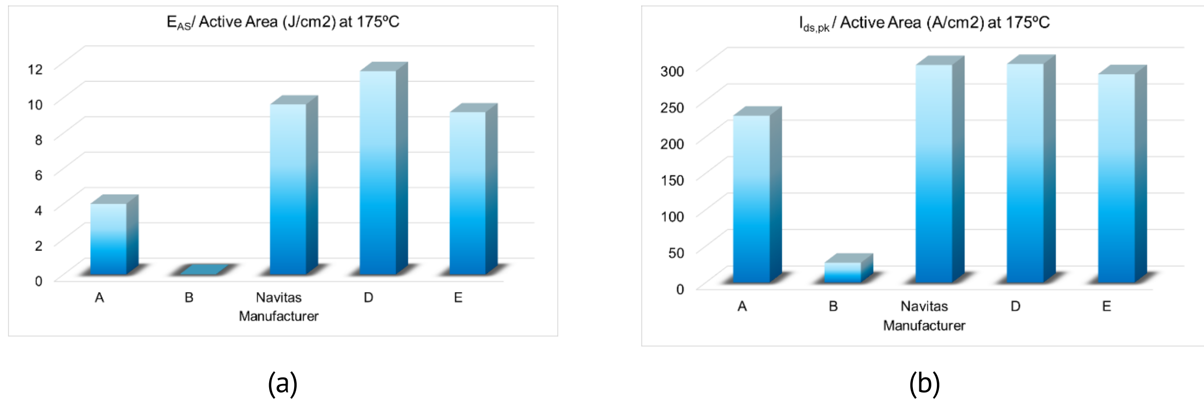


Fig. 4. (a) normalized avalanche energy density (E_{AS} / Active Area); (b) normalized avalanche current density ($I_{ds,pk}$ / Active Area).

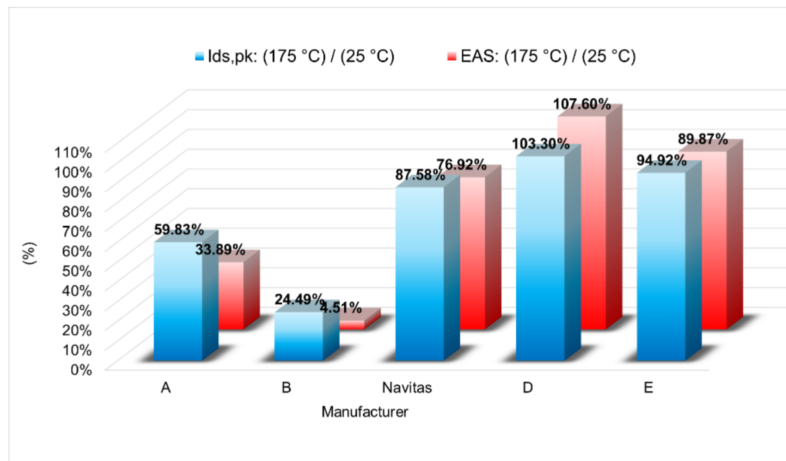


Fig. 5. Percentage change in normalized avalanche energy density and normalized avalanche current density from 25°C to 175°C.

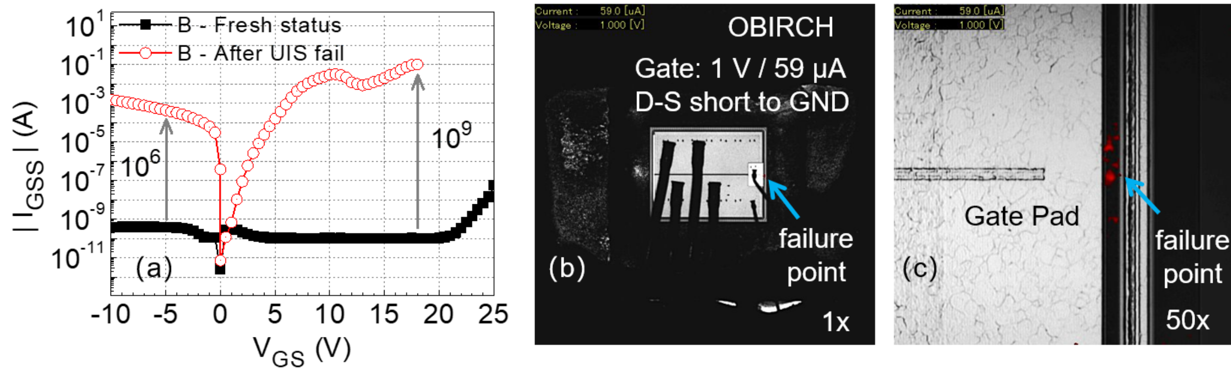


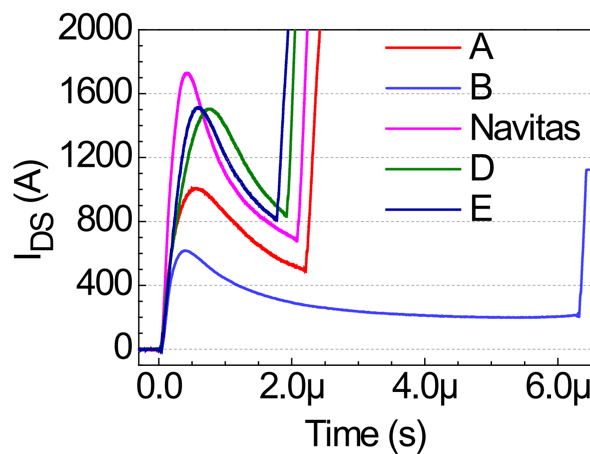
Fig. 6. (a) Gate leakage characteristics of 1200V SiC MOSFET from Manufacturer B tested at fresh status and after UIS fail at 25 °C with D-S short. (b) OBIRCH analysis of the decapsulated sample by applying 1V / 59µA at gate with drain/source short to ground. (c) Zoom-in view of failure point beside gate pad.

The parametric failure evidence of the device from Manufacturer B is explored from gate leakage characteristics as shown in Fig. 6(a). After UIS fail, I_{GSS} at V_{GS} = -5V and +18V is 10^6 and 10^9 times higher than the values in the fresh status, respectively. The sample is further decapsulated without detecting destructive failure points. The optical beam induced resistance change (OBIRCH) analysis is conducted on the decapsulated die to find out the soft failure points located beside the gate pad, as shown in Fig 6 (b) and (c).

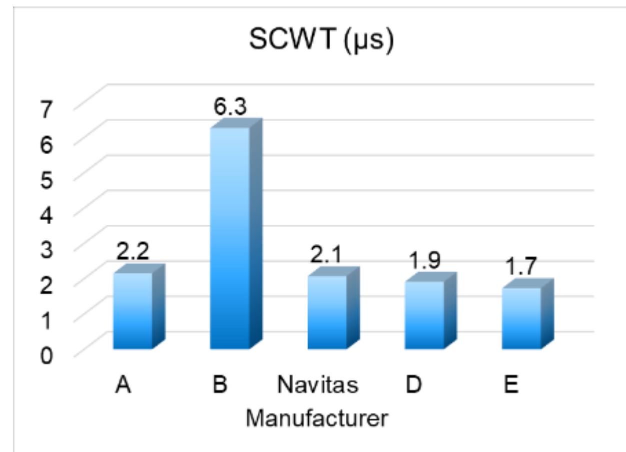
Single-pulse and repetitive short-circuit tests were conducted to evaluate the devices' fault tolerance. The single-pulse short-circuit test was used to quantify three critical parameters: the short-circuit withstanding time (SCWT), the peak short-circuit current density ($I_{ds,pk}$), and the short-circuit

energy density (E_{SC}). As illustrated in Fig. 7, the device from Manufacturer B demonstrated the lowest I_{DS}, highest SCWT, lowest normalized $I_{ds,pk}$ and highest normalized E_{SC}. However, the other devices exhibited a much tighter range of SCWT, from 1.7 to 2.2 µs which are in acceptable range for the automotive applications.

A comparison of the UIS and SCWT results (Fig. 4 to 7) reveals a notable trade-off in Manufacturer B's design. The device's poor performance in the UIS test suggests susceptibility to gate oxide failure caused by electric field concentration at the trench corners. However, this structure appears to excel at thermal management and current limiting, resulting in a superior SCWT. This dichotomy highlights a fundamental design compromise in power semiconductors: optimizing for one type of fault tolerance often comes at the expense of another. Manufacturer B's design appears to have prioritized short-circuit robustness over avalanche capability.



(a)



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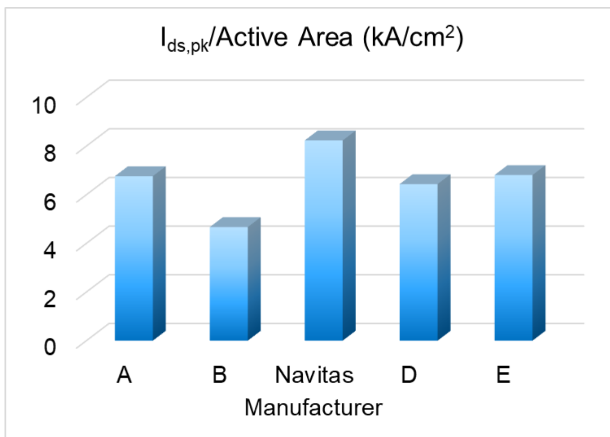
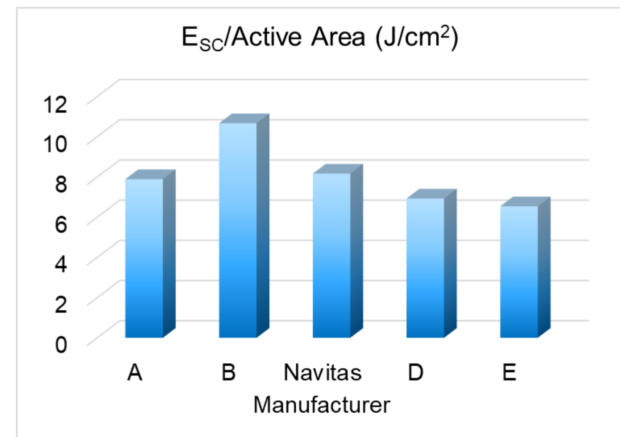


(c)



(d)

Fig. 7. (a) I_{DS} waveforms during the single-pulse short-circuit test under V_{DS} = 800V using $V_{GS,ON}/V_{GS,OFF}$ and $R_{G\text{-}total}$ shown in Table I. Comparison between five different manufacturers in terms of (b) short-circuit withstanding time (SCWT), (c) peak short-circuit current density ($I_{ds,pk}$ / active area) and short-circuit energy density (E_{SC} / active area).

Furthermore, the repetitive short-circuit capability is investigated using a fixed V_{IN} = 800V and a periodic gate driving scheme as shown in Fig. 8. The 1.4µs gate driving pulse and 700 short-circuit shots are used by referring to literature [8]. The 20-second intervals are used to cool down DUTs and avoid self-heating effects during periodic short circuit tests. The intelligent LabVIEW control system can automatically capture I_{DS}, V_{DS}, V_{GS} waveforms during every short-circuit shot. In addition, the I_{GSS} and BV_{DSS} are monitored at 25 °C after every 100 short-circuit events to detect parametric failures.

The results, shown in Fig. 9, indicated that most devices, except for Manufacturer D, showed robust performance with no significant degradation in gate leakage or breakdown voltage. The device from Manufacturer D showed a marked increase in gate leakage and lost its blocking capability after the repetitive stress test, highlighting a potential reliability concern.

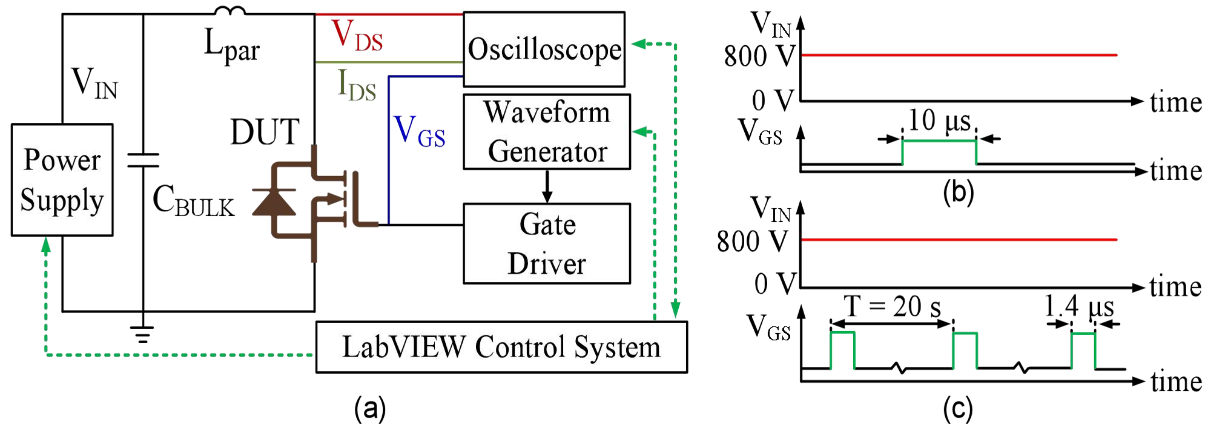


Fig. 8. (a) Schematic of hard switching short-circuit testing setup with LabVIEW control system. Control schematic for (b) single-pulse and (c) repetitive short-circuit test.

Fig. 9. (a) $I_{ds,pk}$ / Active Area and (b) E_{SC} / Active Area, (c) I_{GSS} under V_{GS} = 25 V, V_{DS} = 0 V at 25 °C, (d) percentage shift of BV_{DSS} at 25 °C after 1 to 700 repetitive short-circuit cycles under V_{DS} = 800 V, gate driving pulse width of 1.4 μs.

Summary

This benchmark study comprehensively compares the static and robustness characteristics of five state-of-the-art commercial 1200V SiC MOSFETs. The findings reveal a variety of performance trade-offs among different SiC technologies. Although trench-gate devices offer lower on-resistance at room temperature, planar-gate and trench-assisted planar devices demonstrate superior performance at higher temperatures and greater thermal robustness under avalanche conditions. Short-circuit tests also revealed significant differences in fault tolerance. This underscores the importance of thorough characterization beyond standard datasheet parameters, especially for high-reliability automotive applications. The study confirms that while SiC technology is mature, significant variation still exists in the reliability and performance of commercially available devices.

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