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Scalable Fabrication and Electrical Characterization of Lateral Pin-Diodes on 4H-SiC A-Plane Wafers for Functionalization of Silicon Vacancies

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Abstract. Precise control of optical transitions of color centers like silicon vacancies (V_{Si}) in 4H-SiC is essential for their functionalization. An applied electric field ($\vec{E} \parallel \vec{c}$) of a pin-diode can be used to tune the optical properties of V_{Si} centers via the Stark effect, while the associated space charge region under bias suppresses spectral diffusion. Unlike commonly used 4H-SiC c-plane wafers, a-plane wafers allow a scalable fabrication of lateral pin-diodes and resonant laser excitation of the V_{Si} perpendicular to the wafer surface ($\vec{c} \perp \vec{a}$). In this work non-circular lateral pin-diodes oriented perpendicular to the wafer flat were produced in a scalable, CMOS-compatible process. Electrical characterization revealed that 97% of the devices on an a-plane wafer with n-type epitaxial layer were functional, exhibiting breakdown voltages exceeding 200 V and reverse currents below 100 pA/µm, enabling low current noise during optical measurements. The diodes remained operational at cryogenic temperatures after frozen-out charge carriers were re-ionized by the applied electric field. Electron irradiation followed by thermal annealing at 600 °C was used to generate V2 silicon vacancies in the intrinsic region without significantly altering the electrical characteristics. Optically detected magnetic resonance (ODMR) measurements on selected single emitters confirmed the presence of V2 centers by detecting a contrast at 70 MHz, while cryogenic photoluminescence (PL) spectra revealed a zero-phonon line (ZPL) peak at 916 nm.

Introduction

Color centers such as silicon vacancies (V_{Si}) in 4H-SiC crystals are promising candidates for quantum sensing, communication and computing applications [1–5]. Electric fields of pin-diodes ($\vec{E} \parallel \vec{c}$) have been shown to reduce spectral diffusion and tune the resonant excitation and emission of V_{Si} [5, 6]. This is interesting for the measurement of local physical properties like the electric field inside of a semiconductor device [5], thus allowing for device optimization. Moreover, for possible quantum computing applications the photons emitted by different V_{Si} must be indistinguishable [1]. To compensate for variances in the local environment, and thus the resonant excitation and emission wavelength [7], the electric field can be used to shift the optical transitions [5, 6] to either allow or prohibit optical interaction between multiple V_{Si}.

Unlike commonly used 4H-SiC c-plane wafers, a-plane wafers allow a scalable fabrication of lateral pin-diodes ($\vec{E} \parallel \vec{c}$) in a CMOS compatible process with convenient access to resonant excitation

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perpendicular to the V_{Si} dipole moment, which aligns with the c-axis [7]. This allows laser excitation of the V_{Si} perpendicular to the wafer surface ($\vec{c} \perp \vec{a}$) and in-plane excitation using a waveguide aligned to the m-axis ($\vec{m} \perp \vec{a}$), supporting high scalability and co-integration of advanced electronics and photonics, which is a key step towards quantum photonic integrated circuits (QPICs) [1].

This work demonstrates scalable production of lateral pin-diodes with a CMOS-compatible process on 4H-SiC a-plane wafers. These pin-diodes are electrically and optically characterized at room temperatures and at cryogenic temperatures to investigate their usability in respect to the quantum sensing and computing applications.

Methodology

Device Design.

For the design of the pin-diodes in the intended application, boundary conditions differ from those in standard power electronics, as discussed in the introduction. Key factors include the electric field orientation, high blocking capability with low leakage currents [5], and parameters influencing the optical properties of the color centers. The following design considerations refer to the lateral pin-diodes fabricated on a-plane wafers. The devices on c-plane wafers, sharing identical designs, serve as reference devices purely with respect to electrical characterization.

To achieve the required electric field orientation along the c-axis, unidirectional lateral pin-diodes were fabricated, oriented perpendicular to the wafer flat. Slightly rotated variants were included to compensate for possible crystal orientation deviations from wafer manufacturing. To minimize spectral diffusion, local electrical inhomogeneities and crystal damage, color centers were incorporated into a lowly n-type doped epitaxial layer. Consequently, ion implantations in this region for adjusting series resistance or breakdown field strength were omitted.

Leakage currents, particularly along the passivation interface, are reduced by using a high-quality oxide. Combined with the feature resolution and alignment constraints of the CMOS process, these considerations yield the devices schematically shown in Fig. 1.

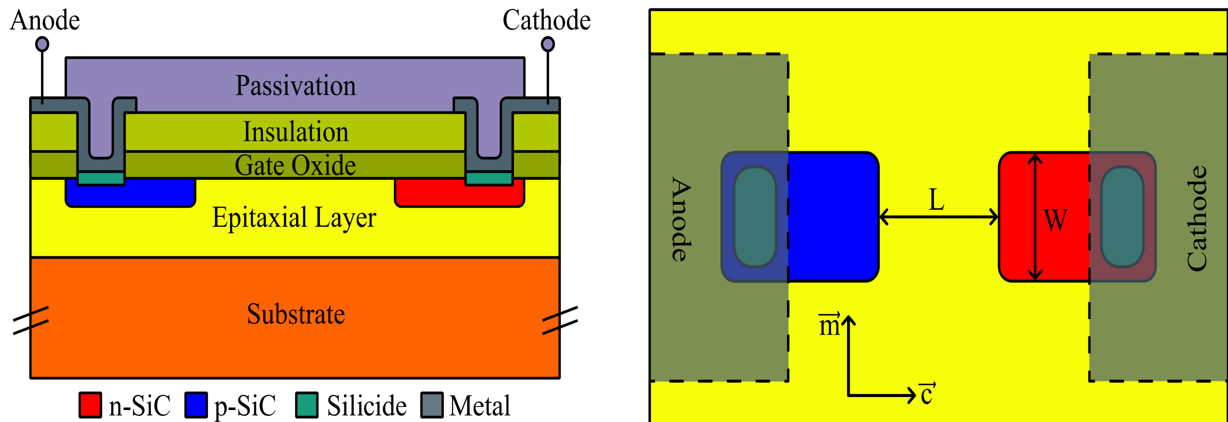

Fig. 1. Schematical cross section (left) and top view (right) of the manufactured lateral pin-diodes on a-plane and c-plane wafers. In the top view the overlying metal layers are shown semi-transparent, and the insulation layers are omitted for better visibility of the underlying structures.

Additionally, diode dimensions as shown in Fig. 1 (right) were varied to study scalability limits and breakdown behavior. Lengths (L) ranged from 1 µm to 20 µm, and widths (W) from 3 µm to 50 µm. The nomenclature “W10L20” denotes a diode with a width of 10 µm and a length of 20 µm.

Sample Fabrication.

The devices were fabricated using a CMOS-compatible process [8] on 35 mm on-axis 4H-SiC a-plane substrates. For reference, identical devices were also produced on 150 mm c-plane wafers with a 4° off-cut. On both substrate types, 10 µm-thick n-type epitaxial layers were grown [9]. An overview of the substrates and their parameters is given in Table 1.

Table 1. Overview of the manufactured samples and their key parameters.

Sample Name	Wafer Orientation	Epitaxial Layer Doping (cm^{-3})
a-plane n-type	$11\bar{2}0$	$8.9 \cdot 10^{15}$
a-plane i-type	$11\bar{2}0$	$2.4 \cdot 10^{13}$
c-plane n-type	0001	$1.2 \cdot 10^{15}$
c-plane i-type	0001	$3.4 \cdot 10^{12}$

To suppress channeling, a 30 nm scattering oxide was deposited prior to ion implantation. Aluminum and nitrogen ion implantations were employed to form the highly doped p-type and n-type regions. Dopant activation was carried out by annealing at 1700 °C in an argon atmosphere using a carbon capping layer to mitigate carbon vacancy formation. The gate oxide was grown by dry thermal oxidation at 880 mbar and 1300 °C, followed by annealing in nitric oxide (NO). Due to different oxidation rates for a-plane and c-plane [9, 10], oxidation times were 6 min 30 s for a-plane and 33 min for c-plane substrates. The NO annealing time for a-plane devices was reduced to 30 min compared to 60 min for c-plane.

After deposition of an additional insulating layer, contact areas were defined by dry etching of the contact holes, followed by self-aligned deposition of a 70 nm thick nickel–2.6 wt% aluminum (NiAl) layer. This layer was patterned by lift-off, and ohmic contacts were formed by rapid thermal processing at 980 °C for 2 min. Residual NiAl was removed using Caro's acid. A stack of 40 nm Ti / 400 nm Pt / 40 nm Ti was deposited for metallization. Finally, a SiO_2 / Si_3N_4 / SiO_2 layer stack was deposited and patterned by dry etching to passivate the devices against environmental exposure.

After full processing V_{Si} were generated by electron irradiation with an energy of roughly 2 MeV and a dose of $3 \cdot 10^{12}$ cm^{-2} with subsequent annealing at 600 °C in vacuum for 30 min.

Electrical Measurements.

Statistical room temperature I-V characterization was carried out by a semi-automatic probing station using a Keithley SCS-4200 SMU. The pin-diodes were measured in multiple measurements to have a high resolution in forward mode and a large measurement range in blocking mode of the device. In forward mode, the devices were measured from 10 V to −2 V in 50 mV steps. To investigate the current in blocking mode voltages up to −200 V with 0.5 V steps were applied. Finally, for characterization of the breakdown behavior up to −420 V were applied. For room temperature measurements, multiple chips with different design variations totaling to at least 300 pin-diodes on each wafer were investigated. Selected chips were also characterized after the electron irradiation and after the annealing step at 600 °C.

Furthermore, to investigate the electrical behavior at 4 K, selected devices were wire-bonded using 50 µm aluminum wire and characterized at various temperatures in an AttoDry800 closed-cycle cryostat. Due to limitations of the measurement setup blocking voltages of only up to −100 V can be applied.

Optical Measurements.

Photoluminescence (PL) characterization was performed using a commercially available confocal PL setup developed by SQUTEC. Excitation was provided by a 730 nm laser operated at a power of 0.1 mW. The laser was focused onto the sample using a 100x Zeiss objective with a numerical aperture of 0.9 and a working distance of 1 mm. To suppress back-reflected excitation light, the emitted PL signal was spectrally filtered using a dichroic mirror with a nominal cutoff at 875 nm, in combination with an 800 nm long-pass filter. The filtered light was coupled into an optical fiber and directed to a superconducting nanowire single-photon detector (SNSPD), read out using a Swabian Instruments Time Tagger 20.

PL xy-scans were conducted with a pixel scan rate of 30 Hz and a pixel spacing of roughly 100 nm. For cryogenic spectral measurements, the sample was cooled to 4 K using an AttoDry800 closed-cycle cryostat. Spectra were recorded using an Ocean Optics QEPro-XR300 spectrometer. ODMR measurements at room temperature were carried out at a similar home-built setup.

Statistical Electrical Characterization at Room Temperature

Production Yield.

After process completion, the wafer first was examined by optical microscope. An overview of a 35 mm a-plane wafer is shown in Fig. 2 (left), demonstrating a scalable process. The yield of the pin-diodes was determined using three criteria which had to be met simultaneously:

1.) Forward mode: current at 0.25 V lower than $1 \cdot 10^{-10}$ A
2.) Forward mode: current at 3 V higher than $1 \cdot 10^{-8}$ A
3.) Blocking mode: current at −50 V lower than $1 \cdot 10^{-10}$ A

For both samples with n-type epitaxial layer the yield reaches as high as 97% (a-plane) or 99% (c-plane). For sample a-plane i-type, a reduced yield of only 23% is observed. This is due to a misalignment of the p-type ohmic contact, which leads to elevated currents in blocking mode on most of the chips, thus failing the third criteria for a working device. Moreover, the yield is reduced to 87% on sample c-plane i-type due to irregularities of the doping of the epitaxial layer in the outer regions.

Besides these effects, nearly all devices are functional and devices with the same design show comparable electrical behavior except some processing-related small variations as exemplarily shown for the diode W20L20 on sample a-plane n-type in Fig. 2 (middle).

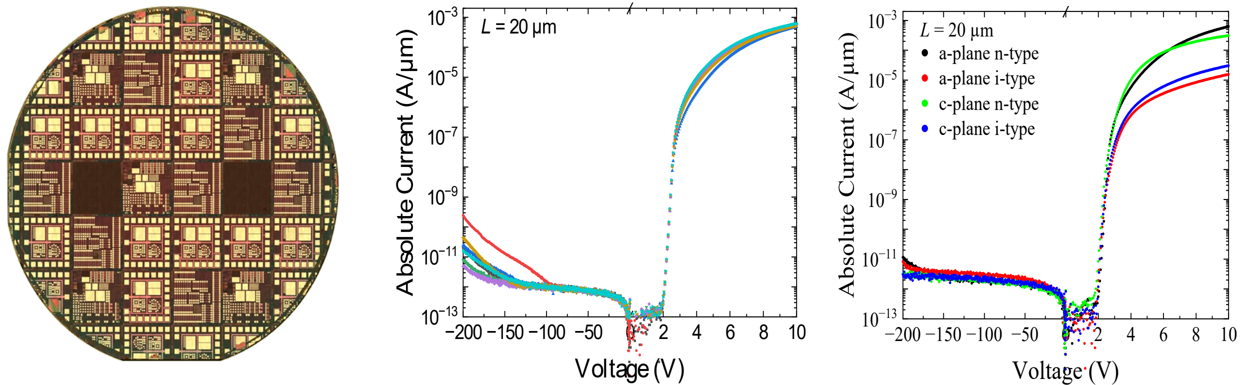

Fig. 2. Left: microscope image of a fully processed a-plane wafer showing a wide variety of integrated devices. Middle: I-V characteristics of all measured identically designed W10L20 pin-diodes on sample a-plane n-type. Right: comparison of I-V characteristics of representative pin-diodes from different samples. Note the different scaling of the x-axis for forward and reverse characteristic. Currents normalized on device width.

Evaluation of Key Parameters.

A comparison of the I-V characteristics of the W10L20 pin-diodes fabricated on different substrates is shown in Fig. 2 (right). In forward bias, the turn-on behavior was comparable for all devices, with only slight variations in the slope near turn-on. At higher forward voltages, however, the devices exhibited pronounced differences in current magnitude. In reverse bias, the behavior was largely similar, with the measured current limited by the accuracy of the measurement setup.

From these measurements, the characteristic parameters of the diodes were extracted and are summarized in Table 2. As expected, statistically significant differences were found in the ideality factor, and particularly the series resistance. Notably, the series resistance differed substantially between the n-type and i-type samples. The main distinguishing factor between the diodes is the doping concentration of the epitaxial layer, which will be further examined through analysis of the design variations. Note that rotating the devices relative to the flat of the wafer had negligible influence on the electrical properties.

Table 2. Evaluated series resistance and ideality factor from the I-V measurements of all measured W10L20 pin-diodes at room temperature for all substrate types.

Sample Name	Series Resistance (Ω)	Ideality Factor
a-plane n-type	521 ± 42	1.81 ± 0.02
a-plane i-type[1)]	27511	2.24
c-plane n-type	1785 ± 45	2.22 ± 0.06
c-plane i-type	15056 ± 2385	1.95 ± 0.10

1) Due to low yield no meaningful standard deviation can be calculated.

Influence of Device Design on Breakdown Voltage.

As Sentaurus technology computer-aided design simulations (not shown) revealed, breakdown in the investigated devices occurs near the surface, specifically at the corner of the p-type implanted region. Due to the small curvature radius at this location, strong electric-field crowding arises. As discussed in the device design section, no countermeasures were implemented to reduce this effect, as the design was optimized for quantum applications. Breakdown voltages were analyzed as a function of epitaxial layer doping and the length of the intrinsic region, as shown in Fig. 3 (left).

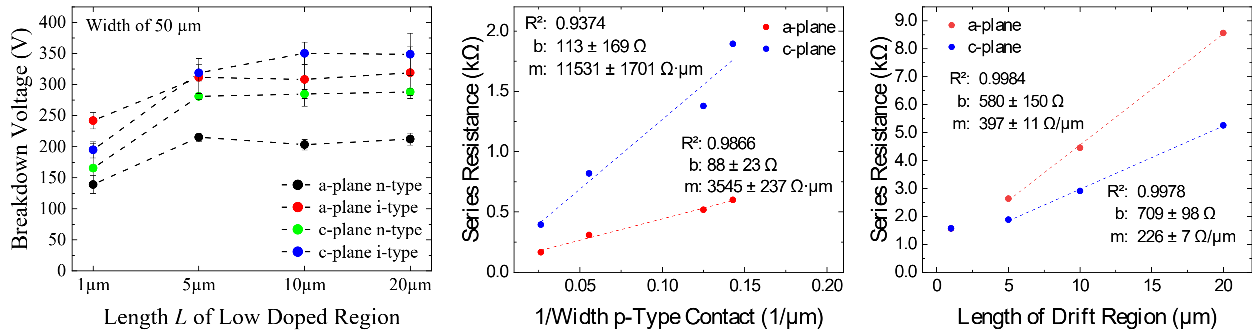

Fig. 3. Left: evaluated breakdown voltages in dependence of the length L of the low doped region. Middle: dependence of the series resistance on the inverse width of the p-type ohmic contact of the n-type L1 samples. Right: dependence of the series resistance on the length of the drift region for the i-type W50 samples. The dashed lines are linear fits (y = m · x + b) to the data points. Their corresponding parameters and coefficient of determination (R^2) are given.

Device breakdown occurs when the local electric field at the p^+/i-interface reaches the material's critical breakdown field. For the present 2D lateral geometry, the breakdown voltage (V_{BD}) can be approximated as the integral over the course of the electric field E along the device axis [11]:

$$V_{BD} = \int_0^L E \cdot dl \qquad (1)$$

This implies that the expansion of the electric field into the highly doped areas is negligibly small compared to *L*. From Poisson's equation:

$$\nabla E = \frac{q \cdot N_D}{\varepsilon_0 \cdot \varepsilon_r} \qquad (2)$$

in the low-doped i-region, the electric-field gradient is directly proportional to the doping concentration N_D. Here, q is the elemental charge, ε_0 the vacuum permittivity and ε_r the specific permittivity of 4H-SiC.
Two trends are observed:

1. Dependence on intrinsic region length

Increasing L of the pin-diode increases the area below the course of the electric field and thus V_{BD}, until a saturation point is reached where the electric field has decayed to near zero before the depletion region reaches the n^+ contact. This corresponds to a non-punch-through condition in pin-diodes, where breakdown is governed entirely by the high-field p^+/i-junction.

2. **Dependence on doping**

Higher doping increases the field gradient, causing the field to decay more rapidly along the depletion path, thereby reducing V_{BD}.

Series Resistance in Forward Bias.

The total series resistance R_S can be expressed as:

$$R_S = R_{metal} + R_{n-ohm} + R_{n^+} + R_{drift} + R_{p^+} + R_{p-ohm} \tag{3}$$

Test structures (transfer length method structures and resistance meanders) confirmed that R_{metal}, R_{n^+}, and $R_{n\text{-}ohm}$ are negligibly small. The dominant terms differ between n-type and i-type devices. For n-type, R_S scales with the width of the ohmic contact, as can be seen in Fig. 3 (middle). The influence of the p-doped-region width is comparatively low and results in a significantly poorer fit (not shown). Still, the deviations from the shown fit can be phenomenologically attributed to the contribution of the p-type implanted region, which was also qualitatively verified but is not shown here.

As shown in Fig. 3 (right), for i-type, R_S is primarily determined by the intrinsic region length. L1 diodes were excluded from fitting due to excessive uncertainty caused by lithographic misalignment. In forward bias, the low-doped region is flooded with carriers, and the excess carrier concentration $\Delta n(x)$ decays exponentially with distance according to:

$$\Delta n(x) \propto e^{\left(\frac{-x}{\sqrt{(D_n \cdot \tau_n)}}\right)} \tag{4}$$

where D_n is the diffusion constant and τ_n is the carrier lifetime [11]. Analog considerations can be made for holes. The short lifetime expected from the lateral geometry and increased interface recombination reduces the diffusion length, leaving a non-flooded region in longer i-type regions where conduction is limited by the background doping N_D. Consequently, the fit for the c-plane sample (lower doping) shows a higher slope compared to the a-plane sample (higher doping).

Electrical Behavior at Cryogenic Temperatures

Modulation of the Onset-Voltage.

At cryogenic temperatures, the aluminum acceptors and the nitrogen donors of 4H-SiC are largely not ionized due to their ionization energies of approximately 200 meV and 60 meV [12], respectively. Under small forward bias, the free carrier concentration is too small to support significant injection, and the diode current remains strongly suppressed, as can be seen in Fig. 4 (blue curves). When the electric field in the depletion region reaches a critical value, however, an abrupt increase in current is observed.

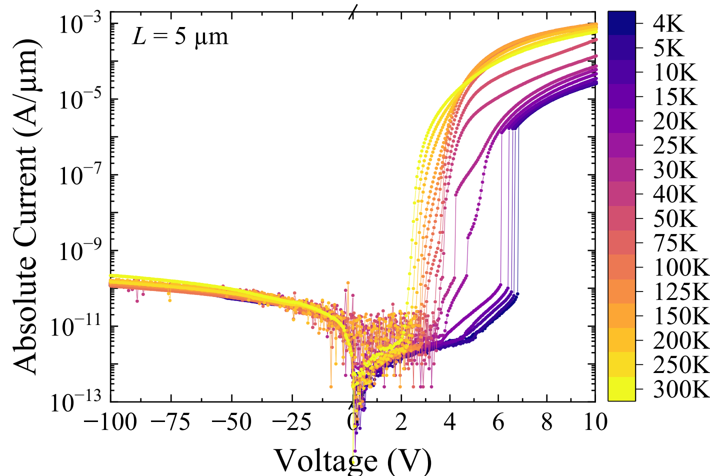

Fig. 4. I-V characteristics of an a-plane lateral pin-diode for different measurement temperatures. Note the different x-axis scaling for forward and reverse bias.

This threshold behavior originates from field-assisted ionization of the frozen-out acceptors [13]. The applied electric field reduces the Coulombic binding potential via the Poole–Frenkel effect [11], lowering the effective ionization energy. In parallel, the few free carriers present are accelerated by the electric field, forming a non-equilibrium hot-carrier distribution with an effective temperature well above the lattice temperature. These hot carriers can transfer part of their kinetic energy to bound carriers in inelastic collisions, thereby ionizing them. Once released, these carriers are also accelerated by the field, enabling them to activate further bound carriers. This positive feedback leads to an avalanche-like multiplication of free carriers once the field exceeds the critical threshold [13].

At elevated temperatures the onset voltage is shown to decrease. This is due to two reasons. On one hand, a larger fraction of dopants is already ionized at higher temperatures. On the other hand, with increasing temperature, thermal activation increasingly contributes to dopant ionization, thus lowering the barrier that must be overcome.

Conductivity in Forward Mode.

As discussed in the previous chapter, the series resistance is strongly influenced by the resistance of the neutral drift region. The conductivity σ of this region where mainly electrons are present can be expressed as:

$$\sigma = q \cdot n \cdot \mu \quad (for\ electrons) \tag{5}$$

where q is the elementary charge, n is the free carrier concentration, and μ is their mobility [11]. The temperature dependence of R_S follows directly from the competing effects of carrier activation and carrier scattering:

- **Low temperatures:** The free carrier concentration n is reduced due to incomplete dopant ionization, resulting in lower σ and thus higher R_S.
- **Intermediate temperatures:** All dopants are ionized, maximizing n, while phonon scattering is still low. Mobility μ is therefore high, leading to a minimum in R_S.
- **High temperatures:** While n remains constant (all dopants ionized), μ decreases due to increased lattice (phonon) scattering. At high T, the mobility approximately follows [11]:

$$\mu \propto T^{\frac{-3}{2}}$$

Consequently, σ decreases, R_S increases, and the on-current decreases again.

Implementation of Silicon Vacancies and Optical Characterization

Influence of Irradiation and Annealing on Device Performance.

In Fig. 5 (left) exemplary I-V characteristics of a selected pin-diode after processing (reference), after electron irradiation and after the 600 °C anneal in vacuum are shown. As can be seen, the device performance degrades slightly by showing increased reverse currents at high blocking voltages. Moreover, after annealing the device shows extended recombination in low forward biasing due to introduced electrically active defects in the space charge region. Furthermore, the series resistance is slightly reduced after annealing probably due to alterations in the ohmic contacts. These effects apply to many examined devices and are differently pronounced. This degradation should not strongly influence the usability of the devices for the intended quantum applications.

Optical Photoluminescence Characterization.

The PL scans recorded after annealing show strong influence of the processing steps on background PL noise. The different device regions (compare Fig. 1 – right) are clearly visible in Fig. 5 (middle). Nevertheless, in the intrinsic region of the pin-diode bright spots are observed, which are shown to be single emitters (not shown). ODMR measurements on selected single emitters at room temperature reveal an ODMR contrast at roughly 70 MHz (Fig. 5 right-top). PL spectra recorded at 4 K show a zero-phonon line (ZPL) at 916 nm (Fig. 5 right-bottom).

These are characteristic for V2 silicon vacancies [5], thus confirming the successful generation of the desired color centers in this region. These color centers are located in the region of the pin-diode, where the electric field can be varied with the applied voltage to tune the optical properties.

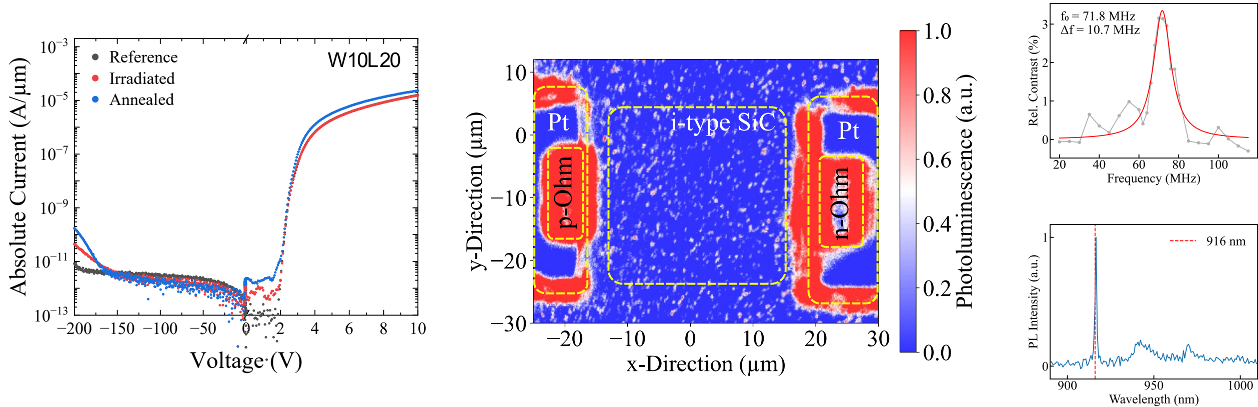

Fig. 5. Left: I-V characteristics of an a-plane lateral pin-diode from sample a-plane i-type after processing, electron irradiation and 600 °C annealing in vacuum. Note the different x-axis scaling for forward and reverse bias. Middle: PL scan of the a-plane n-type pin-diode with generated color centers. The different areas of the pin-diode are marked for visibility. Right: exemplary room temperature ODMR scan and 4 K emission spectrum of selected single V2 center.

Summary

Lateral pin-diodes on 4H-SiC a-plane wafers were successfully fabricated in a CMOS-compatible, scalable process with a device yield of 97%. The structures on the differently doped epitaxial a-plane layers demonstrated breakdown voltages above 200 V (a-plane n-type) and 350 V (a-plane i-type) and low reverse leakage currents (< 100 pA/µm). The devices maintain functionality at cryogenic temperatures after re-ionization of the frozen-out dopants by the electric field. Post-fabrication electron irradiation and annealing generated single V2 silicon vacancies in the intrinsic region without significantly degrading device performance. ODMR and cryogenic PL measurements on selected single emitters confirmed the presence of V2 centers, exhibiting a ODMR contrast at 70 MHz and a ZPL at 916 nm.

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