Key Engineering Materials
ISSN: 1662-9795, Vol. 1056, pp 33-40
doi:10.4028/p-34PxQw

Submitted: 2025-09-13
Revised: 2025-12-04
Accepted: 2026-02-23
Online: 2026-05-20

A Simulation Study of Electronic Device Designs for the Control of SiC Color Centers as Spin Qubits

F. J. Magerl[1,a,*], C. Pixius[2,b], J. Förthner[1,2,c], P. Berwian[2,d], E. Bär[2,e], and J. Schulze[1,2,f]

[1]Friedrich-Alexander-Universität Erlangen-Nürnberg, Chair of Electron Devices, Cauerstraße 6, 91058 Erlangen, Germany

[2]Fraunhofer Institute for Integrated Systems and Device Technology IISB, Schottkystraße 10, 91058 Erlangen, Germany

[a]fabian.magerl@fau.de, [b]christophe.pixius@iisb.fraunhofer.de, [c]julietta.foerthner@iisb.fraunhofer.de, [d]patrick.berwian@iisb.fraunhofer.de. [e]eberhard.baer@iisb.fraunhofer.de, [f]joerg.schulze@fau.de

Keywords: 4H-SiC, Color Centers, Quantum Applications, Qubits, TCAD Simulations

Abstract. Point defects in 4H silicon carbide (4H-SiC), such as the silicon vacancy, also known as color centers, offer considerable potential for quantum applications in the fields of quantum sensing as well as computing and communication. The latter two necessitate indistinguishable photons for entanglement swapping and consequently demand precise control over the electronic transition energies, i.e. emission and absorption wavelengths of color centers. One way to achieve this is through monolithic integration of electronic devices in combination with integrated photonics in 4H-SiC. This is considered a potential pathway for scalable quantum photonic integrated circuits. In this paper, we investigate the suitability of a signal-ground-modulator and a vertical pin diode in combination with a waveguide to (i) achieve local field strengths of 5 to $20\,\mathrm{MV/m}$ in the crystal's c-direction, (ii) stabilize the charge state of the silicon vacancy by controlling the local Fermi level, (iii) meet the requirements for photonic single-mode operation, and (iv) minimize the absorption of the evanescent wave due to metal contacts. The findings of the electronic and optical simulations conducted with Synopsys Sentaurus and Ansys Lumerical suggest that the signal-ground-modulator, commonly used in integrated photonics, rarely attains the requisite field strength. In contrast, the vertical pin diode has the potential to meet these requirements even at reduced bias voltages. Furthermore, the intrinsic layer of the diode offers a wide region in which to host the color center in its optically active, negatively charged state.

Introduction

Due to its long spin-coherence time, the silicon vacancy V_{Si} in 4H Silicon Carbide (SiC) is among the most promising color centers for the realization of spin-qubits with potential applications in quantum computing, quantum communication and quantum sensing [1]. Adding to its appeal is the fact that SiC is a mature technology platform for power electronic devices and applications in photonics. This opens the prospect of designing integrated SiC-based quantum chips that combine both photonic and electronic structures on the same chip.

For quantum computing and quantum communication, it is crucial to reliably entangle color centers at different locations, which can be achieved over macroscopic distances by making use of photon-mediated entanglement swapping [2]. To obtain a high success rate of entanglement, photons emitted from different color centers need to be indistinguishable. However, local variations in the electric field lead to a natural variability in the color centers' energy states, resulting in small shifts of the emitted photon frequencies. To offset the natural variability, precise control over the electronic transition energies is needed. This can be achieved by Stark shift tuning, embedding the color center into an electronic device to modify the electric field in its vicinity [3, 4, 5]. In current research demonstrators, the photons emitted by the color center are focused into an external optical fiber using solid immersion lenses [2, 6]. For future applications, integrating both photonic and electronic structures on the

same chip would be desirable to allow for more scalable technological applications [7]. While there have been successful realizations of the control over electronic transition energies by embedding color centers into electronic devices [8], as well as the successful fabrication of SiC-based photonic structures [9, 10], embedding color centers into both electronic and photonic structures simultaneously has not been investigated yet to our knowledge.

We aim to explore the combined requirements of a V_{Si} center embedded into both an electronic control structure and a single-mode (SM) waveguide made on a Silicon Carbide on Insulator (SiCOI) material. Recent studies on the fabrication of color centers demonstrate high positioning accuracy and implantation depths exceeding 150 nm, enabling precise placement within integrated waveguides and electronic devices [11]. To this end, we simulate two representative categories of electronic device designs compatible with the integration of a SM waveguide. We extract the internal electric field strength and the Fermi level position for the different device designs. The electrical field strength inside the device is essential to shift and to narrow the optical emission lines of individual color centers to make photons emitted by color centers at separate locations (potentially on different chips) indistinguishable. The Fermi level position is essential for the stabilization of the charge state of the color center in thermal equilibrium. Since only the negatively charged silicon vacancy V_{Si}^{-} is optically active, the equilibrium Fermi level must ensure that this charge state is energetically favorable [12]. Due to its wider availability and bigger substrate size, we restrict our analysis to c-plane 4H-SiC. Consequently, the focus is exclusively on device structures that generate vertical electric fields aligned with the dipole axis of the color center, putting a strong constraint on the possible geometries of the electronic structures under investigation. Although investigations have been made on 4H-SiC substrates with alternative crystal orientation, such as a-plane, processing on these substrates differs and is still under investigation [13].

Methods

The electronic device simulations were performed using the latest version of Synopsys Sentaurus (X-2025.06) [14]. Calibration of the simulation models was performed using measurements of forward characteristics of 4H-SiC pin diodes comparable to the simulated ones. We should point out, however, that the electric field and the Fermi level under reverse bias, are insensitive to changes in transport and recombination model parameters, as well as temperature. We are therefore confident that our results are applicable to a wide range of temperatures and device types.

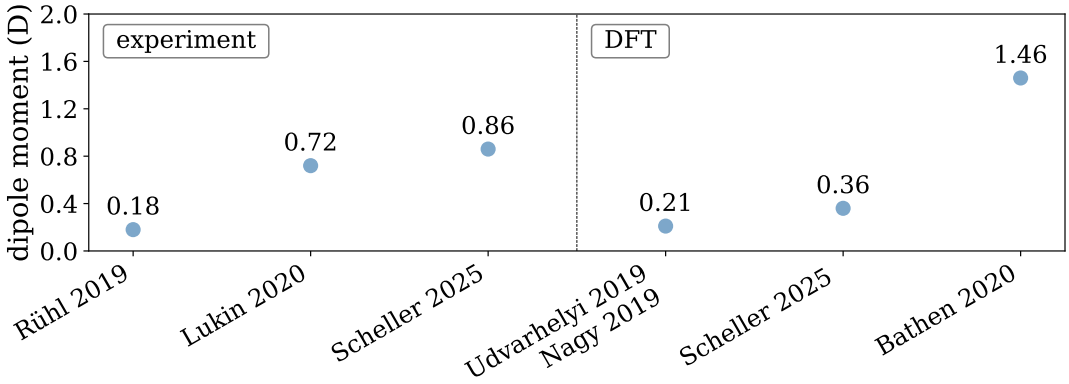
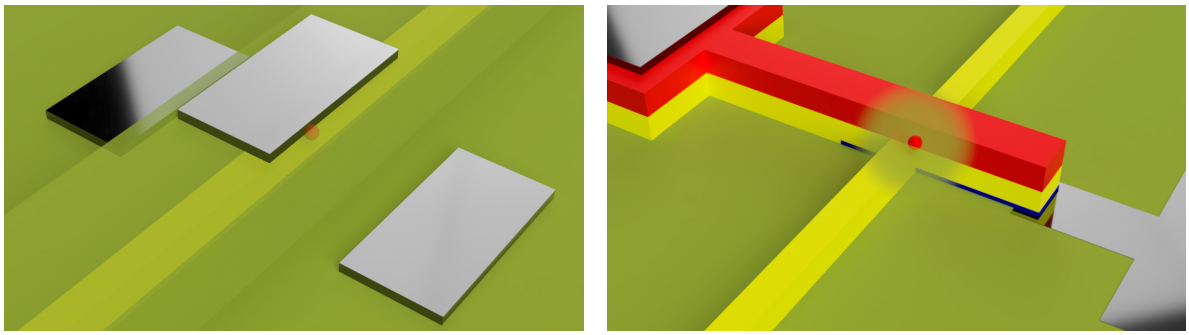


Fig. 1: Experimental and calculated values for the dipole moment of the silicon vacancy in 4H-SiC from different literature sources [3, 8, 9, 15, 16, 17].

A central requirement for a suitable electronic control structure for V_{Si}^{-} centers is the ability to offset the natural spectral distribution. In [18] Nagy *et al.* showed that silicon vacancies at hexagonal lattice sites have a spectral distribution of ± 10 GHz. Offsetting this potential 20 GHz shift between



(a) (b)

Fig. 2: (a) Schematic view of the simulated signal-ground-modulator with one signal electrode above and two ground electrodes next to the waveguide. (b) Schematic view of the vertical pin diode with a waveguide crossing the intrinsic region at the position of the color center. In both panels different regions are color-coded as follows: Intrinsic (low n-type) 4H-SiC (yellow), the V_{Si} (red sphere), dielectric (green), n-type 4H-SiC (red), p-type 4H-SiC (blue) and metal contacts (grey).

two color centers can be achieved by tuning the emission line via the linear Stark-effect [3]:

$$\Delta f = -d \cdot E_{\|c}\,, \tag{1}$$

where Δf is the frequency shift of the optical transition, d is the dipole moment, and $E_{\|c}$ the electric field along the c-axis of the crystal. Published values for the dipole moment of the silicon vacancy from measurements and ab initio simulations [3, 8, 9, 15, 16, 17] are shown in Fig. 1. For a detailed discussion of the underlying experiments and calculations, we refer the reader to the respective papers. We use the two extreme values from the experimental data to calculate a range for the minimal strength of the electric field that needs to be achieved for the required detuning, resulting in $E_{\|c,min}$ between $5\,\mathrm{MV/m}$ and $20\,\mathrm{MV/m}$. In addition to Stark tuning, the electronic structure should stabilize the charge state of the silicon vacancy since only vacancies with a single negative charge are optically active. In thermal equilibrium, the charge state is controlled by the local Fermi-level, which is required to be located between the $(0|-)$ and $(-|2-)$ transition energies, around $1.29\,\mathrm{eV}$ and $0.67\,\mathrm{eV}$ below the conduction band, respectively [12, 19]. Silicon vacancies can be either located at hexagonal $V_{Si}^{-}(h)$ or cubic $V_{Si}^{-}(k)$ lattice sites, where they give rise to the V1/V1' and the V2 emission lines, respectively. However, the electric dipole moment and the transition energies of $V_{Si}^{-}(h)$ and $V_{Si}^{-}(k)$ are largely similar [9, 12], such that we will not distinguish between both lattice sites in the following.

We focus on two structures for the generation of the electric field and the Fermi level control; (i) a signal-ground-modulator (SGM) structure, commonly used for optical modulators, and (ii) a vertical pin diode with an integrated waveguide. Both structures are shown schematically in Fig. 2. The SGM is considered as a representative for a wider group of structures that generate an electric field via a metal electrode sitting on a cladding dielectric.

Due to the high symmetry of the SGM, performing the corresponding TCAD simulations in 2D is sufficient. The vertical pin diode, on the other hand, is simulated in full 3D, since the lack of symmetry at the intersection between the electronic structure and the waveguide, shown in Fig. 2(b), does not allow for a 2D simplification.

Simulation Results

We first determine suitable dimensions for the waveguide by performing finite-difference eigenmode (FDE) simulations using Ansys Lumerical Mode (2021 R1.2) [20]. A 4H-SiCOI rectangular strip waveguide was simulated to find the optimal waveguide geometry for single -mode operation at $861\,\mathrm{nm}$ (zero phonon line of V1). The waveguide was designed to support only the fundamental TE

mode with the dominant electric field parallel to the c-axis while suppressing higher order modes. The substrate was SiO_2 with air cladding above the waveguide resulting in an optimal waveguide height of $650\,\mathrm{nm}$ and width of $220\,\mathrm{nm}$. We additionally analyzed the expected propagation loss of the fundamental mode in the SM waveguide due to the presence of a $4\,\mu\mathrm{m}$ wide and $500\,\mathrm{nm}$ thick metal layer in its vicinity. This resembles typical metal interconnects in state of the art 4H-SiC CMOS technology [21]. Based on this information, we recommend a distance of at least $1.7\,\mu\mathrm{m}$ between the edges of the metal contact and the waveguide to ensure minimal absorption losses below $1 \cdot 10^{-10}\,\mathrm{dB/cm}$. Note that this requirement eliminates the use of Schottky diodes for our purposes and requires unusually thick dielectrics when considering metal-insulator-semiconductor (MIS) structures.

The signal-ground-modulator. At first glance, simple MIS capacitors with a single gate electrode might seem like promising candidates for creating large electric fields around implanted color centers. However, due to the presence of large numbers of charge carriers in the inversion or accumulation layer for MIS devices, the electric field is effectively shielded from the interior of such devices [22]. This rules out MIS structures with a single gate electrode for the purpose of manipulating color centers that are implanted several tens or hundreds of nanometers into the SiC bulk. In the SGM, the presence of a signal and a ground electrode leads to a more homogeneous electric field, making it a potentially viable candidate for the wavelength tuning of color centers. Our 2D simulation model for the SGM is a rectangular SiC waveguide with homogeneous n-type doping of $1 \cdot 10^{15}\,\mathrm{cm}^{-3}$ sandwiched between thick dielectric layers.

The simulated local electric field is presented in Fig. 3(a). Inside the waveguide, the electric field is oriented vertically, parallel to the dipole moment of the color center. Most of the field strength is concentrated across the upper dielectric cladding, with distinct peaks appearing at the cladding edges. Fig. 3(b) illustrates the local field strength obtained in the different constituent materials along the 1D-cutline shown in the left panel of Fig. 3(a). Even at an applied voltage of $100\,\mathrm{V}$ at the signal electrode, the electric field in the waveguide barely reaches the lower threshold of 5 MV/m, as derived in the previous section. This limitation arises from Fermi-level pinning at the SiC/SiO_2 interface, shown schematically in the real-space band diagram of Fig. 3(c). As the applied bias across the SiO_2–SiC–SiO_2 stack is increased, both the conduction and valence band edges shift toward the intrinsic Fermi level. This process attracts charge carriers to the interface, which in turn shield the SiC core from the external electric field. Once the Fermi level reaches the edge of the bandgap on both sides, any further increase in applied bias is immediately compensated by additional charge carrier generation from the semiconductor, thus leading to a saturation in the electric field strength which depends on the thickness of the waveguide.

Fig. 3(c) additionally illustrates that, at $100\,\mathrm{V}$ signal bias, only a narrow region of approximately $250\,\mathrm{nm}$, between $120\,\mathrm{nm}$ and $370\,\mathrm{nm}$ from the interface, supports the negatively charged state V_{Si}^- and consequently, the optically active state. On the one hand, this imposes stringent requirements on the fabrication and control of the V_{Si}^- implantation depth. On the other hand, the region with the correct equilibrium charge state varies depending on the applied signal bias, thus further limiting the allowed values of the signal bias. Fig. 3(d) illustrates the saturation of the maximum electric field strength in the waveguide for different waveguide thicknesses. For decreasing thickness, the maximum electric field strength increases significantly at high applied biases, which can be understood from the band diagram in Fig. 3(c) and the relation between electric field E and valence band energy E_v

$$E = \frac{1}{e} \nabla E_v \,. \tag{2}$$

Assuming a constant gradient of the valence band energy, the electric field strength saturates when the Fermi energy reaches the band edges on the two opposed interfaces, yielding $E_{\mathrm{max}} \approx E_{\mathrm{g}}/(eH)$, where H is the waveguide height and e is the electron charge. This simplified estimate, shown as the black curve in Fig. 3(d) correctly predicts the value where the field strength starts to saturate. Consequently, the waveguide height needs to be carefully adapted to the maximum required electric field to tune

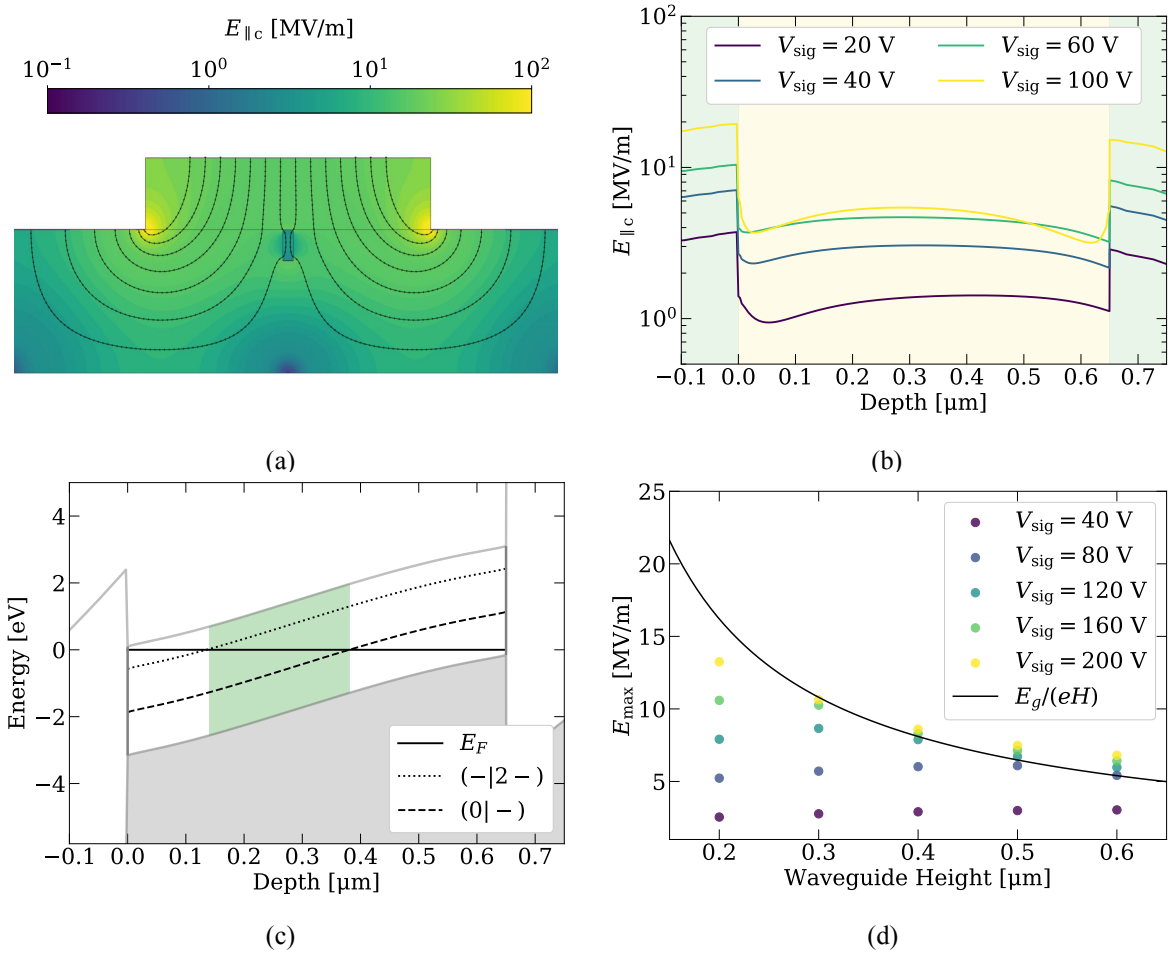


Fig. 3: (a) 2D electric field strength and field lines. (b) Electric field component parallel to the c-axis at different signal biases along the 1D-cutline shown in panel (a), 4H-SiC shown in light yellow, dielectric cladding in light green. (c) Real-space band diagram inside the 4H-SiC waveguide at 100 V signal bias. The blue and yellow curves mark the transition levels of the silicon vacancy between neutral and negative, as well as negative and doubly negative charge state, respectively. The green shaded region, where the Fermi level lies between both transition states, marks the locations where the color center is in the correct charge state in equilibrium. (d) Maximum field strength in the waveguide as a function of waveguide thickness for different signal bias values. The black curve shows the estimation for the maximally attainable field strength from simple geometric arguments.

two V_{Si} to the same wavelength. One should keep in mind, however, that a thinner waveguide also means a narrower region that supports optically active color centers, putting further constraints on the required manufacturing process. Thus we conclude that, although capacitor-like structures such as the SGM at first seem like promising devices for the tuning of color centers, our results show that they are not ideal for color center tuning. Due to the accumulation of charge carriers at the SiC/SiO_2 interface, the attainable strength of the local electric field in the waveguide is severely limited.

The vertical pin diode. A structure that has already been used successfully for the charge stabilization and emission line tuning of color centers is the vertical pin diode. In [19], Widmann *et al.* reported successful integration and charge stabilization of V_{Si} centers in a bulk vertical pin diode. However, some adaptations are needed for such a configuration to become compatible with integrated photonic platforms. We propose the device structure schematically shown in Fig. 2(b), which (i) keeps the metal contacts to the cathode and anode of the pin diode at the required distance from the waveguide to reduce optical losses and (ii) has a thin intrinsic region, adapted to the requirements of an SM waveguide. Our 3D simulation focuses on the central device region, where the waveguide crosses the electronic

structure. The cathode is a homogeneously doped n-type layer with a concentration of $1 \cdot 10^{19}\,\mathrm{cm}^{-3}$ while the anode is a shallow p-type profile with a maximum concentration of $5 \cdot 10^{19}\,\mathrm{cm}^{-3}$ implanted into an n-type epitaxy with low doping ($1 \cdot 10^{15}\,\mathrm{cm}^{-3}$).

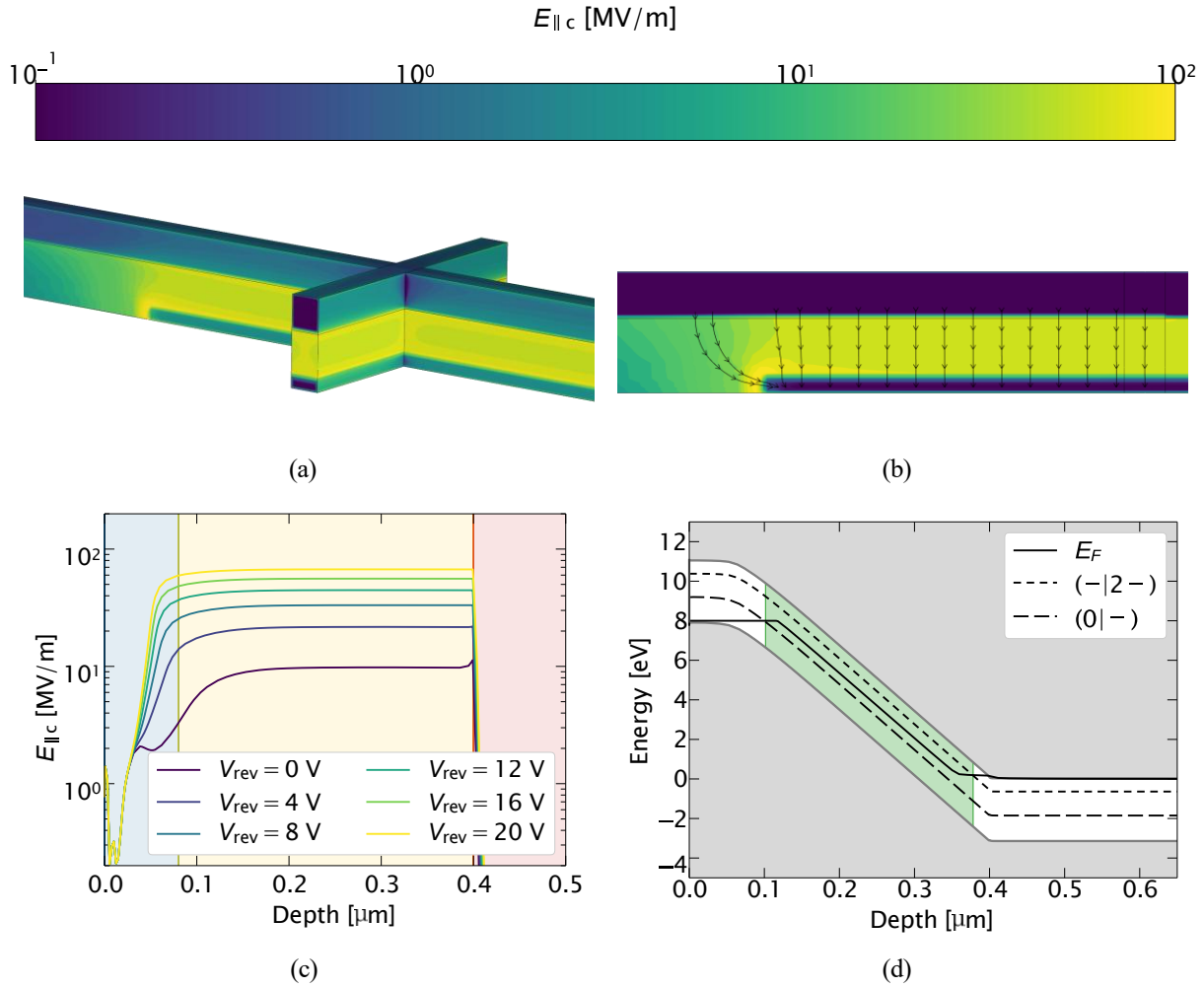


Fig. 4: (a) 3D representation of the electric field strength around the intersection of the pin diode and waveguide at a reverse bias of 20 V. (b) 2D cut along the middle of the 3D structure in panel (a), showing the local field strength and the direction of the field lines. (c) Vertical cut of the field strength inside the pin diode at different reverse bias voltages. The colored regions indicate the doping according to the same color-coding as in Fig. 2(b). (d) Real-space band diagram along the same vertical cut as in panel (c) at a reverse bias of 8 V. The green shaded region indicates the depth range where the color center is present in the optically active charge state.

Fig. 4(a) presents a 3D map of the electric field strength at the intersection of the waveguide and vertical pin diode structure at an applied voltage of 20 V. The shorter arm in the figure corresponds to the waveguide, while the extended arms to the left and right connect to the contact pads, as shown schematically in Fig. 2(b). As illustrated in Figs. 4(a) and 4(b), the application of a bias voltage of 20 V already yields electric field strengths that approach 100 MV/m, oriented vertically across the waveguide region. The vertical pin diode reaches the required field strength at substantially lower applied voltages than the previous configuration. This significantly simplifies implementation in experimental setups and facilitates the design of quantum photonic integrated circuits (QPIC). Also note that, even with field-crowding effects at the edge of the implanted region in Fig. 4(b), the maximum electric field in the device is still well below the breakdown field of 4H-SiC. The intrinsic region of the pin diode supports a strong internal electric field even at zero applied bias, a consequence of the highly doped p- and n-regions. For a heavily doped $p+/n+$ junction, the maximum electric field within the

intrinsic region can be approximated by $E_{\mathrm{max}} \approx (V_{\mathrm{ext}} + V_{\mathrm{bi}})/W_{\mathrm{i}}$, where V_{ext} is the externally applied bias voltage, V_{bi} is the built-in potential, and W_{i} is the intrinsic layer thickness [22]. Furthermore, this electric field remains nearly constant across a spatial extent of approximately $300\,\mathrm{nm}$. In contrast to the SGM, the maximum Stark-shift tuning of the color center is therefore not limited by the structure, but by the breakdown electric field strength of 4H-SiC itself. Compared to the SGM, the intrinsic region of the pin diode additionally offers a broader range for stabilizing $\mathrm{V_{Si}}$ in its negatively charged state. This behavior is illustrated in the real-space band diagram of Fig. 4(d) at $8\,\mathrm{V}$ bias. Specifically, this region extends about $120\,\mathrm{nm}$ from the p-region, allowing a large degree of flexibility regarding the implantation depth of the color center.

Conclusion

We employed TCAD simulations to investigate the performance of two distinct electronic structures for stabilizing the charge state and tuning the emission lines of color centers in 4H-SiC. Fundamental requirements, such as the distance between the integrated waveguide and metal contacts or the direction and penetration depth of the electric field rule out many basic device designs, such as Schottky diodes, lateral pin diodes and simple MIS structures. We therefore focused on the signal-ground-modulator and the vertical pin diode, both of which fulfill the minimum requirements. Our simulations revealed several advantages of the vertical pin diode over the signal-ground-modulator. These include a high electrical field strength parallel to the direction of the color center's dipole even at relatively low bias voltages. In addition, the space charge region in the intrinsic layer of the pin diode provides a large area to maintain the color center in the optically active charge state.

Although vertical pin diodes and a photonic single-mode waveguides are well-established structures in SiC, process related challenges to the integration of both components remain. While more work is needed for the technological realization of the proposed device structures, success would pave the way for scalable SiC quantum photonic integrated circuits.

Acknowledgement

We thank C. Schwemmer (Fraunhofer IISB) for helpful discussions on spin-photon entanglement. We acknowledge that this work is funded by the Deutsche Forschungsgemeinschaft (DFG, German Research Foundation) – 532769051, included in the QuantERA call 2023, and Lighthouse Project TeQSiC (State of Bavaria).

Author Contributions

F. J. M. together with C. P. performed optical and electrical simulations. J. F. helped developing the concept and supervised the project. All authors discussed and contributed to the manuscript.

References

[1] S. Castelletto and A. Boretti, *Silicon carbide color centers for quantum applications,* J. Phys. Photonics, vol. 2, no. 2, p. 22001, 2020, doi: 10.1088/2515-7647/ab77a2.

[2] H. Bernien *et al.*, *Heralded entanglement between solid-state qubits separated by 3 meters,* Nature, vol. 497, no. 7447, pp. 86–90, 2013, doi: 10.1038/nature12016.

[3] M. Rühl *et al.*, *Stark Tuning of the Silicon Vacancy in Silicon Carbide,* Nano letters, vol. 20, no. 1, pp. 658–663, 2020, doi: 10.1021/acs.nanolett.9b04419.

[4] C. F. de las Casas *et al.*, *Stark tuning and electrical charge state control of single divacancies in silicon carbide,* Applied Physics Letters, vol. 111, no. 26, 2017, doi: 10.1063/1.5004174.

[5] C. P. Anderson *et al.*, *Electrical and optical control of single spins integrated in scalable semiconductor devices,* Science (New York, N.Y.), vol. 366, no. 6470, pp. 1225–1230, 2019, doi: 10.1126/science.aax9406.

[6] R.-Z. Fang *et al.*, *Experimental Generation of Spin-Photon Entanglement in Silicon Carbide,* Phys. Rev. Lett., vol. 132, no. 16, 2024, doi: 10.1103/PhysRevLett.132.160801.

[7] G. Moody *et al.*, *2022 Roadmap on integrated quantum photonics,* J. Phys. Photonics, vol. 4, no. 1, p. 12501, 2022, doi: 10.1088/2515-7647/ac1ef4.

[8] D. Scheller *et al.*, *Quantum-enhanced electric field mapping within semiconductor devices,* Phys. Rev. Applied, vol. 24, no. 1, 2025, doi: 10.1103/pv13-vgcw.

[9] D. M. Lukin *et al.*, *Spectrally reconfigurable quantum emitters enabled by optimized fast modulation,* npj Quantum Inf, vol. 6, no. 1, 2020, doi: 10.1038/s41534-020-00310-0.

[10] C. Babin *et al.*, *Fabrication and nanophotonic waveguide integration of silicon carbide colour centres with preserved spin-optical coherence,* Nature materials, vol. 21, no. 1, pp. 67–73, 2022, doi: 10.1038/s41563-021-01148-3.

[11] Y. Xue *et al.*, *Selective generation of V2 silicon vacancy centers in 4H-silicon carbide,* Nano Letters, vol. 24, no. 7, p. 2369-2375, 2024, doi: 10.1021/acs.nanolett.3c03905.

[12] M. E. Bathen *et al.*, *Electrical charge state identification and control for the silicon vacancy in 4H-SiC,* npj Quantum Inf, vol. 5, no. 1, 2019, doi: 10.1038/s41534-019-0227-y.

[13] J. H. Schwarberg *et al.*, *Investigation of CMOS Single Process Steps on 4H-SiC a-Plane Wafers for Quantum Applications*, 2024, 47th MIPRO ICT and Electronics Convention (MIPRO). IEEE, 2024, doi: 10.1109/MIPRO60963.2024.10569589.

[14] Sentaurus™ *Process User Guide*, Version X-2025.06, Synopsys Inc., 2025.

[15] M. E. Bathen *et al.*, *First-principles calculations of Stark shifts of electronic transitions for defects in semiconductors: the Si vacancy in 4H-SiC,* Journal of physics. Condensed matter : an Institute of Physics journal, vol. 33, no. 7, p. 75502, 2020, doi: 10.1088/1361-648X/abc804.

[16] R. Nagy *et al. High-fidelity spin and optical control of single silicon-vacancy centres in silicon carbide*, Nat Commun 10, 1954 (2019), doi: 10.1038/s41467-019-09873-9.

[17] P. Udvarhelyi *et al.*, *Spectrally Stable Defect Qubits with no Inversion Symmetry for Robust Spin-To-Photon Interface,* Phys. Rev. Appl., vol. 11, no. 7, p. 044022, doi: 10.1103/PhysRevApplied.11.044022.

[18] R. Nagy *et al.*, *Narrow inhomogeneous distribution of spin-active emitters in silicon carbide,* Applied Physics Letters, vol. 118, no. 14, p. 46, 2021, doi: 10.1063/5.0046563.

[19] M. Widmann *et al.*, *Electrical charge state manipulation of single silicon vacancies in a silicon carbide quantum optoelectronic device,* Nano letters, vol. 19, no. 10, pp. 7173–7180, 2019, doi: 10.1021/acs.nanolett.9b02774.

[20] *Lumerical Inc.*

[21] A. May *et al.*, *A 4H-SiC CMOS technology enabling smart sensor integration and circuit operation above 500 C*, 2024 Smart Systems Integration Conference and Exhibition (SSI). IEEE, 2024, doi: 10.1109/SSI63222.2024.10740550.

[22] S. M. Sze and K. K. Ng, *Physics of Semiconductor Devices*: Wiley, 2006, doi: 10.1002/0470068329.