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Channel Length Effects on Threshold Voltage Instability in Gamma Irradiated 4H-SiC PMOSFETs

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Abstract. Silicon carbide (SiC) complementary metal-oxide-semiconductor (CMOS) technology and its circuit applications have been rapidly advancing, making the stability and reliability of planar p-channel metal-oxide-semiconductor field-effect transistors (PMOSFETs) increasingly important. In this study, a channel-length-dependent threshold voltage instability was observed under both gate bias stress and gamma-ray irradiation. The results indicate that the majority of positive charge trapping originates from hole injection induced by external bias. Secondary ion mass spectrometry (SIMS) analysis confirmed the retention of aluminum species in the gate dielectric after thermal oxidation. Based on these experimental findings, a dopant diffusion model was proposed, suggesting that dopant contamination in the gate oxide is the primary cause of the channel-length-dependent instability.

Introduction

4H-type silicon carbide (4H-SiC) is regarded as one of the most promising semiconductor materials for power electronic applications, owing to its wide bandgap, high thermal conductivity, and high electron mobility [1]. Various types of SiC devices, such as junction barrier Schottky (JBS) diodes [2] and vertical double-diffused MOSFETs (VDMOSFETs) [3, 4], are now widely used in automotive, renewable energy, and transportation applications [5]. Beyond these advantages, SiC has also attracted considerable attention from the aerospace industry for the past two decades due to its high threshold displacement energy [6]. This property enables SiC-based detectors to exhibit strong resistance to radiation damage while maintaining stable charge collection efficiency [7].

To further expand its applications, many studies have investigated the radiation effects on MOS structures, particularly VDMOSFETs. One of the most critical concerns is the generation of electron–hole pairs in silicon dioxide under gamma-ray irradiation. Because holes have relatively low mobility, they tend to be trapped in the oxide [8]. If a significant number of charges are trapped, this can degrade both conduction and blocking characteristics, as demonstrated in previous studies [9, 10].

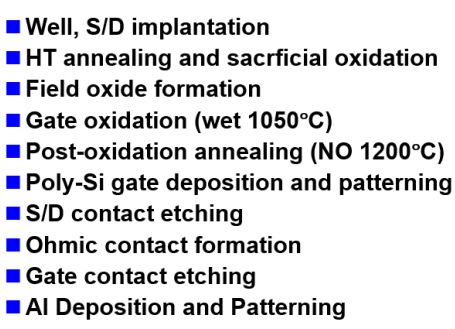
Moving beyond power MOSFETs, it is also essential to understand the effects of radiation on CMOS devices. With continuous progress in SiC CMOS technology, which is now capable of supporting simple circuit implementations [11, 12], evaluating its radiation tolerance has become increasingly important. Consequently, the electrical performance and stability of both NMOS and PMOS devices under radiation environments are critical research topics. Research on the electrical performance and stability of 4H-SiC PMOSFETs remains relatively limited. Therefore, in this work, we focus on the electrical characteristics of PMOSFETs and propose a novel explanation for the observed phenomenon.

Experiments

The simplified process steps and the cross-sectional structure of the PMOSFETs are illustrated in Fig. 1. The fabrication process began with a 4H-SiC wafer consisting of a 5.5-µm-thick epitaxial layer with a nitrogen concentration of 1×10^{16} cm^{-3}. The N-well and N^+ regions were formed by phosphorus implantation, while aluminum implantation was employed for the p-type regions. To reduce the threshold voltage of the PMOSFETs, a counter-doping implantation was applied to the channel. Ion implantation was performed at 500°C, followed by high-temperature activation at 1700°C for 30 minutes. The 40-nm-thick thermal gate oxide was grown in a wet ambient at 1050°C, followed by pure NO post-oxidation-annealing (POA) at 1200°C. Nickel was used as the contact metal, and ohmic contact was formed through appropriate annealing. More details of the fabrication process can be found in our previous work [12].

The experimental setup is shown in Fig. 2. The fabricated chips were packaged on a printed circuit board and mounted on an acrylic stand. A cobalt-60 gamma-ray source was used to irradiate the samples at a dose rate of 0.515 kGy(Si)/hr. During irradiation, the PMOSFETs were subjected to a gate bias of –20 V, while all other terminals were grounded. The devices were divided into two groups: one group was exposed to a total gamma-ray dose of 1 kGy under gate bias, while the other was only subjected to gate bias stress for 2 hours (the same duration as the irradiation). This experimental design was intended to distinguish the effects of gamma-ray irradiation from bias stress

The threshold voltage (V_{th}) was defined as the gate to source voltage (V_{GS}) at which the normalized drain current, $I_D \times (L/W)$—where L and W represent the channel length and width, respectively-reached 10 nA at a drain to source voltage (V_{DS}) of -0.1 V. However, the extracted V_{th} is affected by the interface state density, making it difficult to accurately estimate the trapped charge density in the gate oxide using V_{th} alone. To address this, an additional self-defined parameter, V_i, was introduced, defined as the gate voltage at which the normalized drain current reaches 1 pA. This parameter helps to minimize the ambiguity caused by subthreshold swing (S.S.). The S.S. was extracted from the normalized current in the range of 10 to 100 pA.



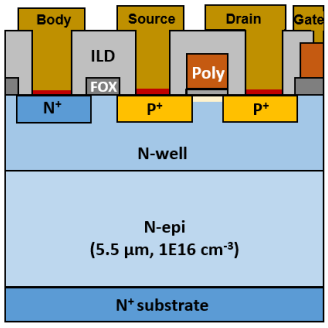


Fig. 1. Simplified process flow and cross-sectional structure of the PMOSFETs.

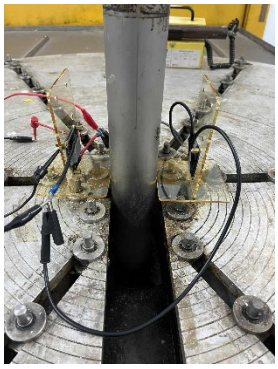


Fig. 2. Experimental equipment and samples setup.

Results and Discussion

Fig. 3 presents the transfer characteristics of PMOSFETs with different channel lengths before and after gamma-ray irradiation. As expected, both devices exhibit a clear leftward shift in the I–V curves. However, an unexpected result is that the short-channel device (L = 0.8 µm) shows a much larger shift compared to the long-channel device (L = 50 µm). The precise changes in the extracted parameters are summarized in Table I. A difference of approximately 1.2 V in ΔV_{th} between the short- and long-channel devices was calculated, with only minor contributions from ΔS.S. The change of trapped charge per area (ΔQ_{ox}) can still be reliably estimated from ΔV_i using the relation

$$\Delta Q_{ox} = \Delta V_i / C_{ox}. \quad (1)$$

where C_{ox} is the specific capacitance of gate oxide. Based on this calculation, the gate dielectric of the short-channel device is found to trap approximately 1.5 times more positive charges than that of the long-channel device.

Table 1. Change of electrical properties after irradiation and gate stress. All parameters were extracted at V_D of -0.1 V.

Device	After Irradadiation		After Gate Stress	
	L= 0.8 μm	*L*= 50 μm	*L*= 0.8 μm	*L*= 50 μm
ΔV_i (V)	-1.56	-0.63	-1.46	-0.61
ΔS.S. (mV/dec)	39	-2	-73	-78
ΔV_{th} (V)	-1.79	-0.59	-0.78	-0.39

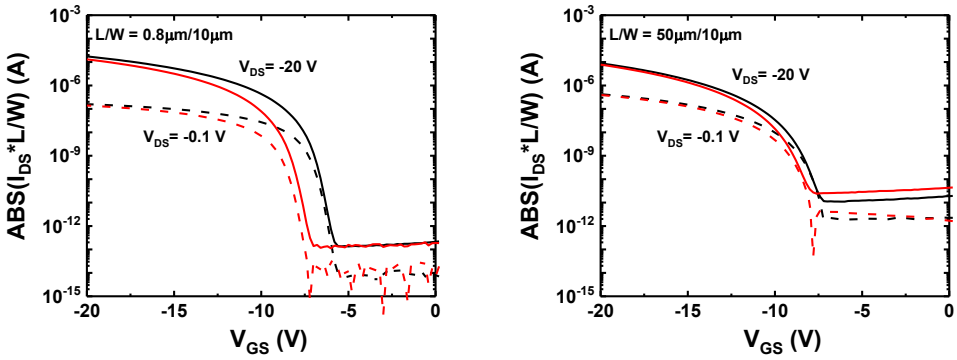


Fig. 3. Transfer characteristics of PMOSFETs before and after gamma irradiation under a gate bias of -20 V for 2 hours. (a) *L*= 0.8 μm (b) *L*= 50 μm.

For the samples subjected to 2 hours of gate bias stress, the results are shown in Fig. 4, where a gate-length-dependent ΔV_{th} is also observed. For devices with the same channel length, the irradiated samples exhibit a larger threshold voltage shift. This phenomenon is related to the improvement in S.S. caused by gate bias stress, although the exact mechanism remains unclear. The uncertainty in S.S. highlights the necessity of introducing the parameter V_i. Interestingly, the ΔV_i values of PMOSFETs with the same channel length are found to be very similar in different groups. This indicates that gamma-ray irradiation contributes primarily to the maintenance or degradation of the S.S., whereas negative bias is more effective in trapping positive charges than gamma-ray–induced charge generation. The efficiency of trapping holes can be explained by considering that holes generated under irradiation tend to drift toward the poly-Si side under the electric field, thereby reducing their impact on the I–V curve shift. In contrast, carriers induced by gate bias can directly inject into the oxide near the SiC/oxide interface. A schematic illustration of this explanation is provided in Fig. 5.

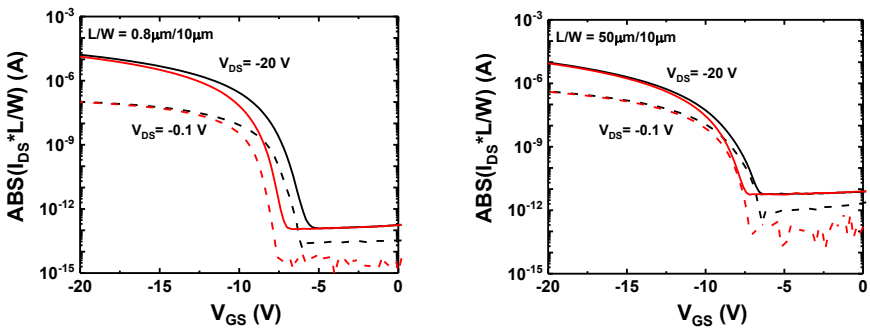


Fig. 4. Transfer characteristics of PMOSFETs before and after gate stress at -20 V for 2 hours. (a) *L*= 0.8 μm (b) *L*= 50 μm.

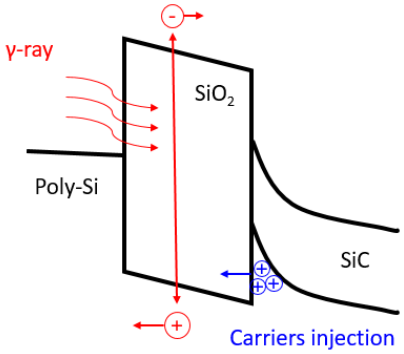


Fig. 5. The schematic of band diagram illustrating carriers movement in PMOSFETs under negative gate bias during gamma-ray exposure.

To account for the observed gate-length-dependent ΔV_{th} and ΔV_i, a lateral dopant diffusion model was proposed. To establish this model, it is first necessary to confirm that aluminum species remain in the SiO_2 after oxidation and POA. A SIMS analysis was performed on an aluminum-implanted wafer after the thermal oxidation step, and the result is shown in Fig. 6(a). The Si intensity profile was used to identify the SiO_2/SiC interface, and a dopant concentration exceeding 1×10^{19} cm^{-3} was detected in the oxide. Since SiC processes typically involve high temperatures, often reaching 1300°C or higher, the retained dopants are able to laterally diffuse from the source and drain edges toward the gate center [13], as shown in Fig. 6(b). Under the same processing conditions, a larger fraction of the gate oxide in short-channel devices becomes contaminated by these dopant species. These atoms may act as trap centers [14, 15], resulting in a higher effective trapped charge density in short-channel devices and, consequently, larger shifts in the I–V characteristics.

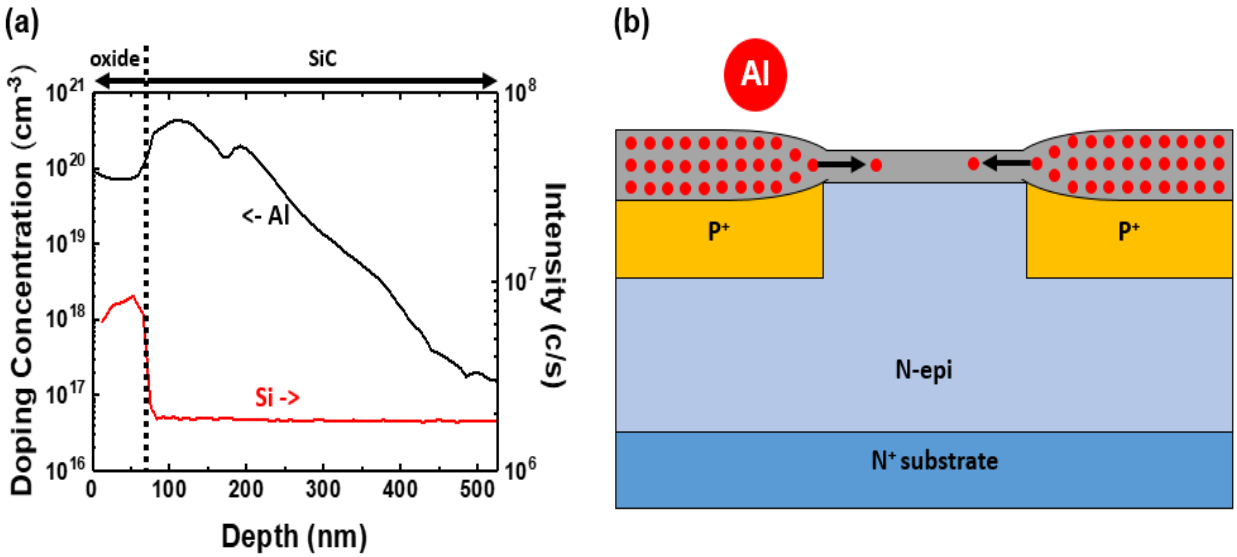


Fig. 6. (a) SIMS depth profile of Al atoms in the gate oxide and SiC. The dashed lines represent the oxide/SiC interface. (b) The schematic of lateral dopants diffusion model.

To further confirm that the trapped charges indeed affect the electrical characteristics, Sentaurus TCAD simulations were performed to analyze the electrostatic conditions of the PMOSFET gate oxide with and without positive charge incorporation under all electrodes grounded. Fig. 7(a) and 7(b) show the simulated potential distribution of a short-channel PMOSFET (L = 0.8 μm). In Fig. 7(a), the gate oxide is assumed to be free of trapped charges, whereas in Fig. 7(b), a Gaussian distribution of positive charges with a peak concentration of 1×10^{18} cm^{-3} is introduced at the edges of the P^+ regions adjacent to the channel. In the charge-free case Fig. 7(a), the equipotential lines in both the gate oxide and the channel region remain flat and uniform, indicating stable electrostatic conditions. By contrast, in the charged case Fig. 7(b), the equipotential lines become distorted, particularly near the channel

edges, revealing a significant perturbation to the electrostatic potential profile. Fig. 8 shows the valence-band energy along the channel, taken very close to the oxide/SiC interface (Line A in Fig. 7(b)). The case with oxide charges exhibits a lower valence-band energy in the channel region, which corresponds to a higher barrier for hole transport from source to drain. As a result, a higher gate voltage is required to induce sufficient carriers. This distortion strongly suggests that trapped charges in the oxide can degrade MOSFET operation, especially in short-channel devices where the entire channel is more sensitive to local field variations. For comparison, in a long-channel device (L = 50 μm), the distortion caused by trapped charges is confined primarily to the channel edges, while the central channel region gradually recovers to a more uniform potential distribution, similar to the charge-free case. This highlights the channel-length dependence of charge-induced potential distortion in SiC PMOSFETs.

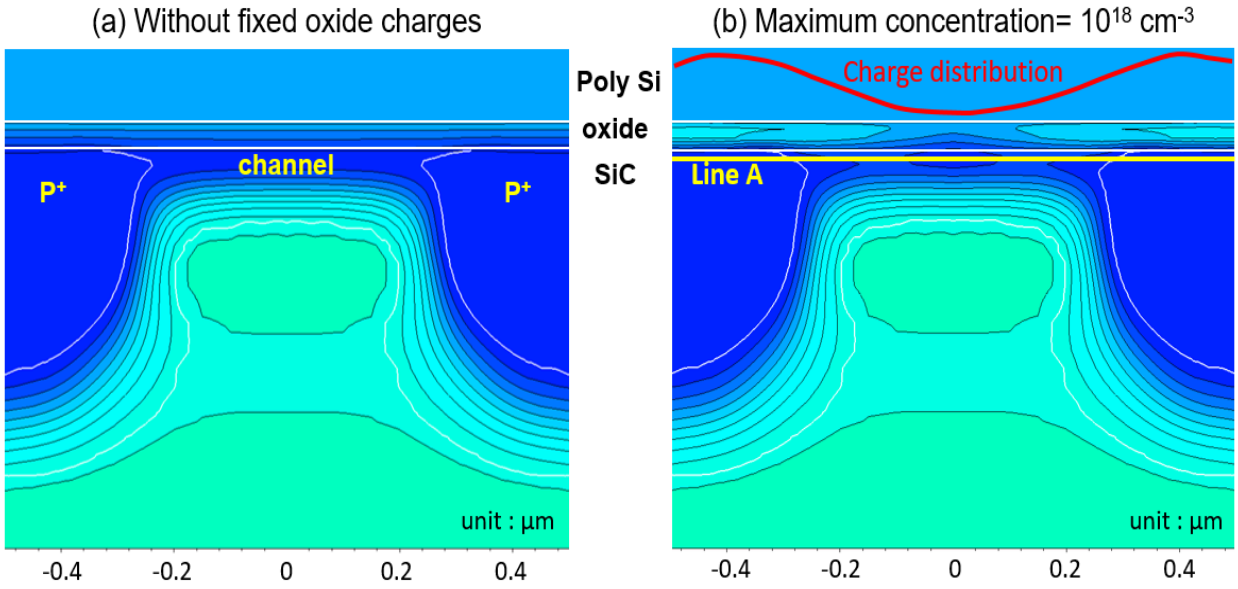


Fig. 7. Equipontential lines distribution in short-channel PMOSFET (a) without and (b) with fixed oxide charges.

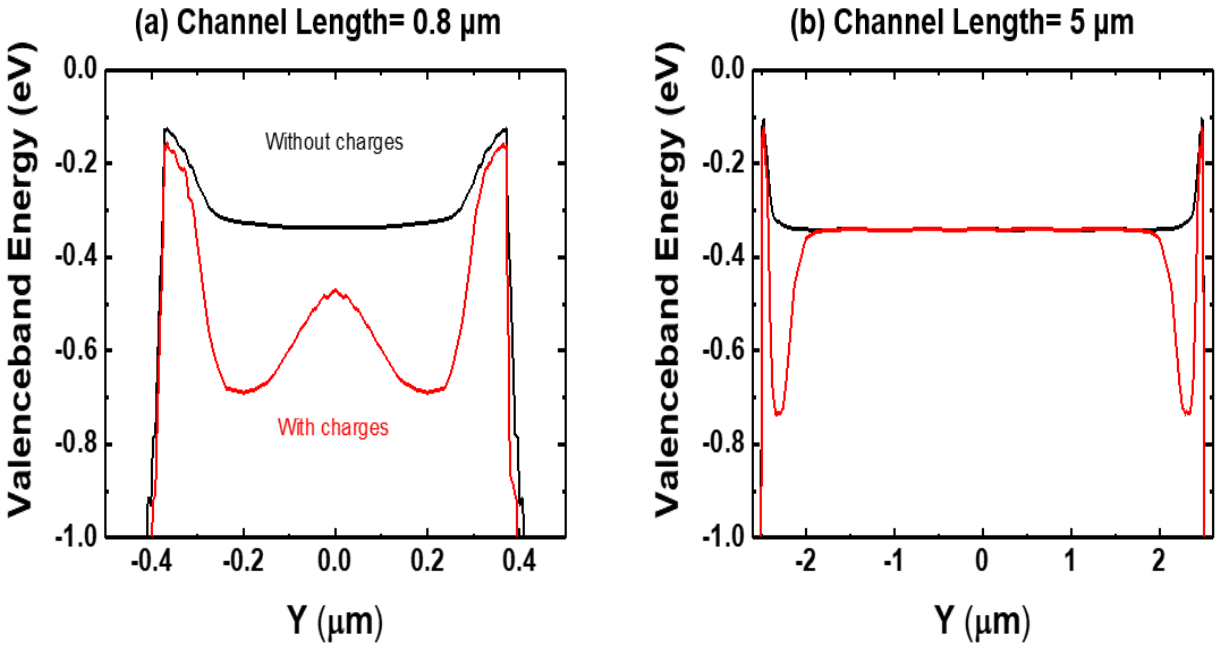


Fig. 8. Valence-band energy at line A in Fig. 7(b). (a) L= 0.8 μm (b) L= 5.0 μm.

Summary

In summary, a channel-length-dependent threshold voltage instability was observed under both gate bias stress and gamma-ray irradiation. The experimental results indicate that the majority of positive charge trapping originates from hole injection induced by external bias, and gamma-ray irradiation contributes the change in S.S. SIMS analysis further confirmed the retention of aluminum species in the gate dielectric after thermal oxidation. Based on these findings, a lateral dopant diffusion model was proposed, suggesting that aluminum contamination in the gate oxide is the primary cause of the channel-length-dependent instability. Finally, TCAD simulations were employed to analyze the electrostatic potential distribution in PMOSFETs, clearly revealing how trapped charges affect their electrical performance.

Acknowledgement

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