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Towards a Fully Integrated 4H-SiC A-Plane Quantum-Chip – Transistors and Light Emitters

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Abstract. Silicon vacancies (V_{Si}) are relevant for quantum technologies, including sensing, computing, and communication. For the realization of quantum photonic integrated circuits (QPICs) and, therefore, co-integration of optical and electrical devices with resonant excitation through the wafer surface, a-plane 4H-SiC wafers are required. Transferring established complementary metal-oxide-semiconductor (CMOS)-compatible processes from c-plane to a-plane wafers is, therefore, a crucial step. In this work, key fabrication steps, namely ion implantation, thermal oxidation, and ohmic contact formation, were investigated for a-plane 4H-SiC substrates. To demonstrate successful process transfer, p-channel MOS field-effect transistors were fabricated and electrically characterized, showing comparable I_{on}/I_{off} ratios and mobilities to their c-plane counterparts, but with a threshold voltage shift from −7.1 V to −12 V on the a-plane. Additionally, tunneling diodes were realized as broadband light emitters, with a significant portion of the emission spectrum falling within the range of off-resonant excitation of V_{Si} centers. The devices maintained light emission functionality down to cryogenic temperatures.

Introduction

Silicon vacancies (V_{Si}) in 4H-SiC emerged as a promising candidate for quantum sensing, communication and computing applications [1–5]. Electric fields enable tuning of their optical properties by depleting the local environment from free charge carriers thus reducing noise and by shifting resonance frequencies using the Stark effect [2, 6]. Since the dipole moment of V_{Si} is aligned with the c-axis of the crystal, optical resonant excitation must be carried out perpendicular to this axis [7]. Conventional c-plane wafers only allow resonant excitation through a cleaved edge of the wafer [2], thus impairing the electrical properties of the devices. In contrast, lateral pin-diodes ($\vec{E} \parallel \vec{c}$) on 4H-SiC a-plane wafers ($\vec{a} \perp \vec{c}$) enable convenient resonant excitation through the wafer surface.

Since these pin-diodes can be manufactured in a complementary metal-oxide-semiconductor (CMOS)-compatible process on the 4H-SiC platform [8, 9], co-integration of advanced integrated electronics and photonics is enabled which is a key step towards quantum photonic integrated circuits (QPICs) [1]. These allow for on-chip excitation and read-out of optical signals, thus lowering cost and complexity of the measurement setups needed.

In this work, we demonstrate the compatibility of the CMOS process on c-plane and a-plane wafers exemplarily using a p-channel MOS (pMOS) field-effect transistors, thus allowing transfer of state-of-the-art devices and circuits to a-plane wafers. Furthermore, a tunneling diode, which can be manufactured in the same CMOS process, is proposed as a possible on-chip integrated light source for initialization and off-resonant excitation of V_{Si}.

Methodology and Sample Fabrication

The tunneling diodes and pMOS transistors were fabricated using a CMOS-compatible process [8] on two 35 mm on-axis 4H-SiC a-plane substrates. For reference, identical devices were also produced on four 150 mm c-plane wafers with a 4° off-cut. On both substrate types, 10 µm-thick n-type epitaxial layers were grown [9]. The nitrogen doping corresponds to the pMOS channel doping given in Table 3. To suppress ion channeling, a 30 nm scattering oxide was deposited prior to implantation. Aluminum and nitrogen ion implantation was employed to form the highly doped p-type and n-type regions, with implantation parameters as listed in Table 1. Dopant activation was carried out by annealing at 1700°C in an argon atmosphere for 1 h using a carbon capping layer to mitigate carbon vacancy formation.

Table 1. Ion implantation parameters for generation of n-type and p-type profiles.

	n-type (nitrogen)		p-type (aluminum)	
Parameter	Energy (keV)	Dose (1/cm²)	Energy (keV)	Dose (1/cm²)
Shot 1	90	$4.0 \cdot 10^{14}$	90	$2.8 \cdot 10^{14}$
Shot 2	50	$2.3 \cdot 10^{14}$	60	$1.8 \cdot 10^{14}$
Shot 3	25	$2.0 \cdot 10^{14}$	30	$1.4 \cdot 10^{14}$

The gate oxide was grown by dry thermal oxidation followed by an annealing in nitric oxide (NO) both at 880 mbar and 1300 °C. Due to different oxidation rates for a-plane and c-plane [9, 10], oxidation times were 6 min 30 s for a-plane and 33 min for c-plane substrates. The NO annealing time for a-plane devices was reduced from 60 min to 30 min.

The gate electrode was formed by low pressure chemical vapor deposition of n-doped polycrystalline silicon and patterned using a combination of dry and wet etching. After deposition of an insulating layer, contact areas were defined by dry etching of the contact holes, followed by self-aligned deposition of a 70 nm nickel–2.6wt% aluminum (NiAl) layer. This layer was patterned by lift-off, and ohmic contacts were formed by rapid thermal processing at 980 °C for 2 min. Residual NiAl was removed using Caro's acid. Following gate via etching, a metal stack of 40 nm Ti / 400 nm Pt / 40 nm Ti was deposited for metallization. Finally, a SiO_2 / Si_3N_4 / SiO_2 layer stack was deposited and patterned by dry etching to passivate the devices against environmental exposure.

Evaluation of Test Structures for Assessing Process Success

Ion Implantation.

For both c-plane and a-plane samples, ion implantation was performed using identical shots. Secondary ion mass spectrometry (SIMS) measurements are shown in Fig. 1 (left).

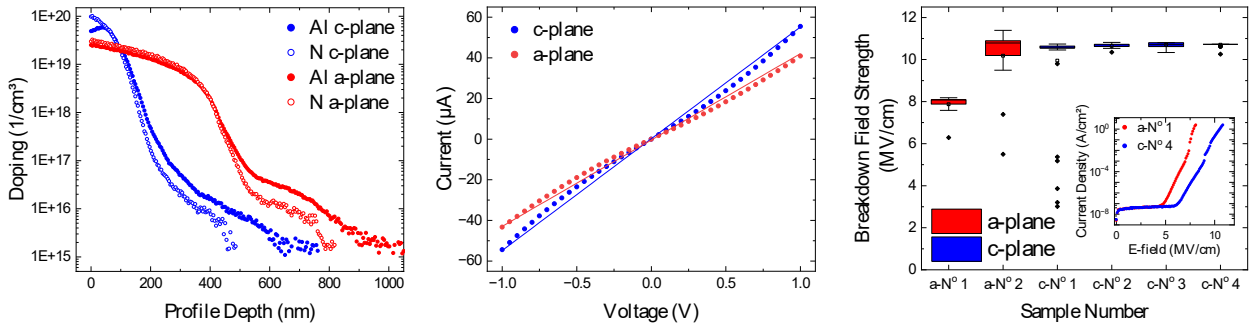

Fig. 1. Left: SIMS measurements of the implanted n+- and p+-profiles on a-plane and c-plane samples. Middle: raw data of an I-V measurement of the p-type ohmic contacts. The straight lines are for better visibility of the measured data and underline the non-ideal ohmic behavior of the p-type ohmic contacts. Right: breakdown field strength of the thermally grown oxides of all samples grouped by substrate type. Sample sizes are 15 for a-plane and 51 for c-plane. Inset: exemplary leakage current density against applied electric field for samples a-N° 1 and c-N° 4.

The profiles reveal a deeper dopant penetration in the a-plane samples. This effect is attributed to extended channeling, which occurs despite the presence of a scattering oxide. The most plausible explanation for this is additional channeling along the m-axis, which is tilted by 30° relative to the a-axis and provides an additional channel path. Monte Carlo simulations conducted in Sentaurus technical computed aided design (TCAD) tool suggest that this behavior cannot be completely prevented no matter the implantation angle and scattering oxide thickness [9].

The influence of these implantation profiles on the sheet resistance of the p-type regions was evaluated based on transfer length method (TLM) measurements. A slight sheet resistance variation between a-plane (53.2 ±4.6 kΩ/□) and c-plane (40.7 ±0.8 kΩ/□) samples was observed. This impact may result from the higher background doping of the n-type epitaxial layer [9]. Since the TLM evaluation is based on purely ohmic behavior of the contacts, non-idealities also my lead to deviations. Furthermore, minor deviations in the implanted dose cannot be excluded, as two different implantation systems had to be used due to the differences in wafer size.

For a complete process transfer, further testing with deeper implantation profiles – such as those used for p-well and n-well formation – is required. Nevertheless, the achieved high surface concentrations of the present process should allow for ohmic contact formation.

Ohmic Contact Formation.

For characterization of the ohmic contacts, multiple TLM structures on a-plane and c-plane samples were characterized after processing was completed. The specific contact resistance of the n-type ohmic contact could not be determined exactly, because no p-well was used in this study. Consequently, the discussion focuses on the p-type ohmic contact, which is generally reported to be more challenging to form [11] and showed roughly 4 orders of magnitude higher specific contact resistance compared to n-type ohmic contacts. The contribution of the n-type contact resistance is, therefore, assumed to be negligible for the subsequent analysis.

Raw data from the I-V measurements of a p-type contact is presented in Fig. 1 (middle) for both investigated substrates. The I-V characteristics indicate that a perfectly ohmic behavior was not achieved in either case, still symmetric conductivity for positive and negative voltages is observed. Nonetheless, the evaluated specific contact resistances for a-plane (103 ± 6.5 mΩcm²) and c-plane (109 ± 10.4 mΩcm²) show no significant dependence on the substrate orientation. Thus, the process transfer to the a-plane substrate was successful. However, further optimization potential like utilization of different contact materials for each contact [8] remains.

Thermal Oxidation.

Due to different oxidation rates especially in the reaction limited regime [9, 10] different processing times for a-plane and c-plane were chosen as stated in the methodology section. The resulting layer thicknesses were optically measured to be 50.1 nm (a-plane) and 53.1 nm (c-plane). Since not only physical layer thickness but mainly electrical properties are relevant, I-V and C-V measurements were carried out on multiple 200 µm by 200 µm large vertical MOS capacitors on the epitaxial layer of each sample. From the C-V measurements at 100 kHz, the key parameters shown in Table 2 are evaluated.

Table 2. Evaluated key parameters of the C-V measurements for the different substrates.

Parameter	a-plane	c-plane
Eval. Oxide Thickness (nm)	51.1 ± 0.4	55.1 ± 0.3
Oxide Capacitance (pF)	27.0 ± 0.2	25.1 ± 0.1
Interface State Density ($1/cm^2eV$)[1)]	$9.5 \cdot 10^{11} \pm 0.6 \cdot 10^{11}$	$8.8 \cdot 10^{11} \pm 2.1 \cdot 10^{11}$

1) Evaluated at |E – EC| = 0.2 eV using Terman method [12] for C-V measurements at 100 kHz.

The evaluated oxide thickness matches the optically measured one within a deviation of below 2 nm. Since the thickness is evaluated using the oxide capacitance and the dielectric constant, the growth of an oxide with appropriate dielectric constant is confirmed. Deviations might be due to slight size variations of the MOS capacitor from the wet chemical etching of the electrode. The

interface state density evaluated using the Terman method [12] shows higher concentration for the investigated a-plane samples. This might be explained by the shorter NO annealing time for these samples to avoid extensive layer growth while annealing. In the future, distinct processes for annealing of a-plane samples should be investigated to further reduce the interface state density.

From the I-V characterization, the breakdown behavior of the oxides is evaluated, as shown in Fig. 1 (right). The breakdown field of the oxides is comparable for most processed wafers and in line with the literature values for thermal silicon oxides (e.g. [13, 14]). The lower breakdown field of a-plane sample a-N° 1, thus, is not related to the crystal orientation but likely stems from issues with subsequent wet chemical structuring of the polycrystalline silicon used as gate electrode for the MOS capacitors. As shown in the inset the leakage current density remains negligibly (< 0.1 µA/cm²) small for electric fields up to 5 MV/cm corresponding to roughly 25 V for the given oxide thickness.

Based on the results, the transfer of thermal oxidation process was successful but leaves room for improvement. In particular the post oxidation annealing process might further reduce the interface state density for a-plane samples. Nevertheless, the manufactured oxides with low leakage current and high dielectric breakdown are suitable as gate oxides for pMOS transistors.

Electrical Properties of the Manufactured pMOS Transistors

Device Design.

For demonstration of CMOS-compatibility of the process, standard pMOS field effect transistors were manufactured. The source and drain areas are highly doped p-type regions and the channel is formed by the n-type doping of the epitaxial layer, as shown in Fig. 2 (left). Using the ohmic contacts and metal layers, the source was shorted with the body potential, as can be seen in Fig. 2 (right). The width of the channel (W) is 12 µm and the length (L) varies from 1 µm to 3 µm. The gate overlaps slightly with the source and drain areas to compensate for misalignment during lithography, thus preventing channel pinch off. The structure is encapsulated using a multi-layer insulation and passivation.

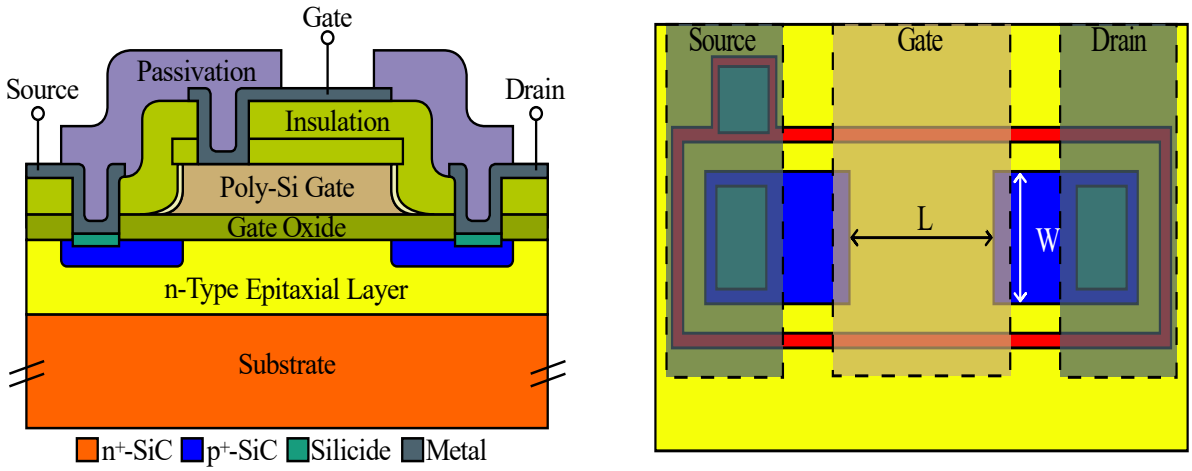

Fig. 2. Schematic cross section (left) and top view (right) of the manufactured pMOS transistors on c-plane and a-plane wafers. In the top view overlying metal layers are shown semi-transparent, and insulation layers are omitted for better visibility of the underlying structures.

Electrical Measurements.

For statistical characterization, output and transfer characteristics of the fabricated devices were measured with a semi-automatic probing station using a Keithley SCS-4200 SMU. Transfer characteristics were recorded from 0 V to −20 V in −0.1 V steps at a drain voltage of −1 V. Output characteristics were measured from 0 V to −10 V in −0.1 V steps at gate voltage from 0 V to −15 V in −1 V steps.

Electrical Properties.

Exemplary representative I-V characteristics for an a-plane and a c-plane device with a channel length of 2 µm are shown in Fig. 3. The devices on both substrates are functional and clearly show an on and an off state. As can be seen in the transfer characteristics (left) the devices on a-plane substrates have a significantly lower threshold voltage (V_{Th}) of −12 V compared to −7.1 V for c-plane samples. This is at least partwise explainable by the higher doping of the epitaxial layer of the a-plane samples (see Table 3 – top row) as well as their increased interface state density as discussed in the previous section.

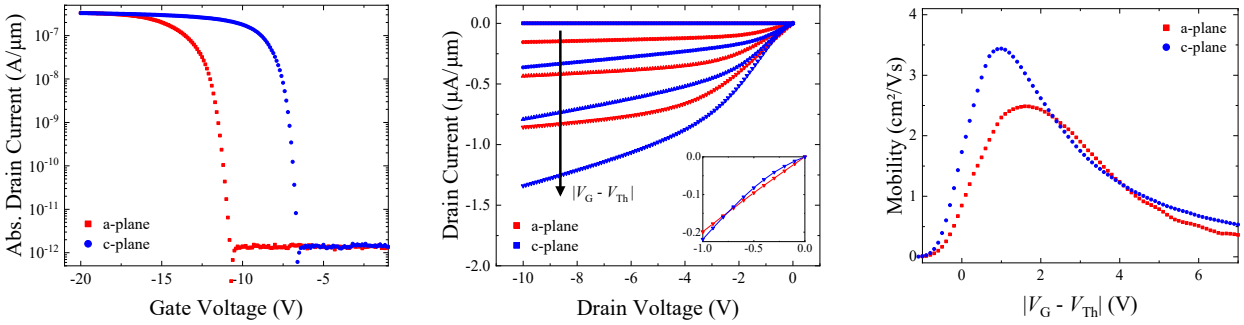

Fig. 3. Transfer characteristics (left) and output characteristics (middle) of representative pMOS transistors with a channel width of 12 µm and a length of 2 µm. Inset: zoomed view of the linear region of the output characteristic. Right: representative characteristics of the mobility as function of the V_{Th} corrected gate voltage.

In the output characteristics (Fig. 3 middle) an extended influence of short-channel effects (drain induced barrier lowering – V_{Th} decreases and current increases with rising drain voltage [15]) on the c-plane samples can be seen. This is due to the lower doping of the epitaxial layer leading to stronger influence of the applied drain voltage compared to the a-plane devices. This effect gets stronger for shorter channel length (not shown). The inset in the output characteristics shows the not ideal ohmic behavior of the metal contacts on the p-type areas in the linear region of the pMOS.

Calculating the mobility dependance of the applied gate voltage (compensated for the V_{Th} differences) gives the characteristics shown in Fig. 3 (right). As can be seen, the characteristic for a-plane is similar to c-plane. The slightly lower maximum mobility on a-plane samples compared to c-plane samples is likely due to the higher interface state density as discussed for the V_{Th} variation. Due to these results and as stated before a post oxidation annealing which is distinctly tailored for a-plane interfaces should be investigated.

The evaluated characteristics for all measured a-plane and c-plane pMOS transistors with a channel length of 2 µm with their standard deviation are summarized in Table 3. As can be seen the transfer of the CMOS process to a-plane wafers was successful, thus enabling manufacturing of more complex devices and circuits on a-plane wafers. Process optimization especially for the SiC / SiO_2 interface is needed to move the threshold voltage closer to 0 V and increase the carrier mobility.

Table 3. Evaluated key parameters and standard deviation of all pMOS transistors with channel width of 12 µm and length of 2 µm.

Parameter	a-plane	c-plane
Channel Doping (10^{15}/cm^3) [3]	8.9 ± 0.1	1.2 ± 0.1
I_{On} / I_{Off}	$2.42 \cdot 10^6 \pm 0.04 \cdot 10^6$	$2.48 \cdot 10^6 \pm 0.69 \cdot 10^6$
Threshold Voltage (V)[1)]	-12.0 ± 0.1	-7.10 ± 0.6
Maximum Mobility (cm²/Vs)	2.32 ± 0.14	2.84 ± 0.43
R_{On} @ $\lvert V_G - V_{Th}\rvert$ = 3 V (kΩ)	388 ± 7	321 ± 68

1) Evaluated using Second-Derivative method [16] with slight smoothing according to [17]

Electrical and Optical Properties of the Manufactured Tunneling Diodes

Device Design.

The light emitters are designed as circular devices. To achieve high tunneling currents with a broad radiative recombination spectrum the n^+- and p^+-implanted areas are designed as overlapping circles (Ø 56 µm to 58 µm) represented in violet in Fig. 4. Since donors as well as acceptors are present in this region trap assisted tunneling with radiative recombination can take place. Both areas are contacted using ohmic contacts and the metal layer stack. To route the inner contact region to the contact pad the outer p-type implanted area and ohmic contacts are interrupted.

Electrical and Optical Measurements.

For electrical characterization at room temperature I-V measurements were carried out in a range from 5 V to −30 V in 0.1 V steps with a semi-automatic probing station using a Keithley SCS-4200. For cryogenic measurements the device was cooled using

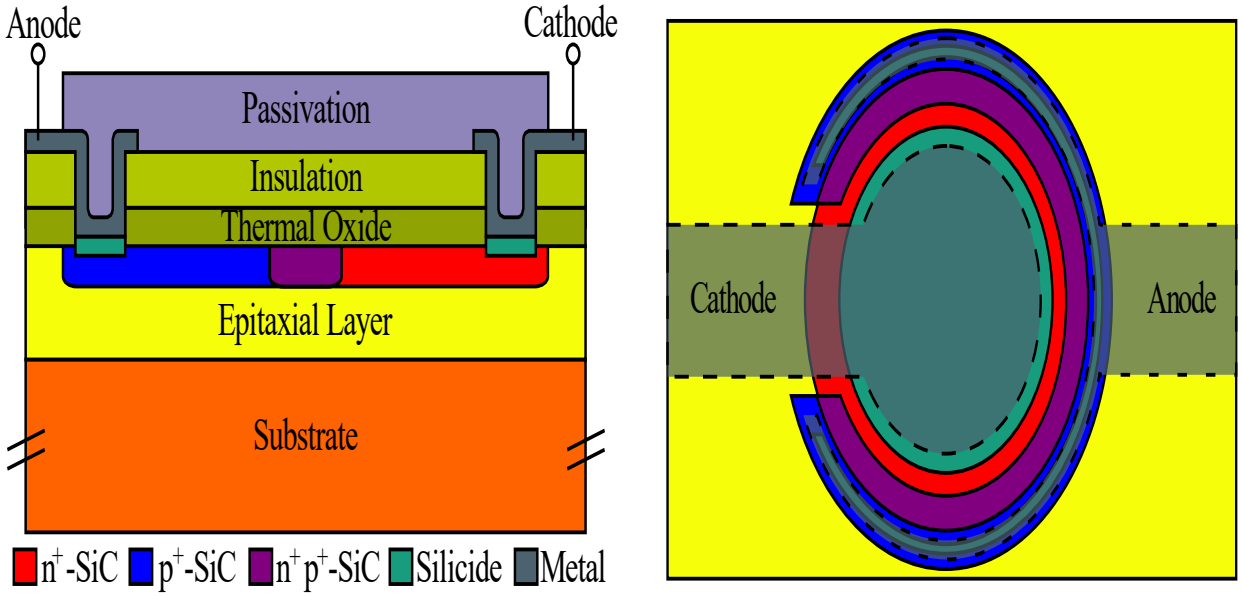

Fig. 4. Schematic cross section (left) and top view (right) of the manufactured tunneling diode on c-plane and a-plane wafers. In the top view the overlying metal layers are shown semi-transparent, and the insulation layers are omitted for better visibility of the underlying structures.

an attodry800 closed-cycle cryostat and a HP4145B semiconductor analyzer. For these measurements the range was changed to 10 V to −80 V with the current being limited to 10 mA in reverse mode to avoid extensive heating. Emission spectra in forward and reverse bias were recorded at 300 K using a Zeiss MCS CCD UV-NIR spectrometer with a glass fiber positioned closely above the device.

Electrical Properties at Room Temperature.

In Fig. 5 (left) exemplary representative I-V characteristics of an a-plane and c-plane tunneling diode are shown. As can be seen, both diodes show diode-like behavior in forward bias, confirming the successful process transfer from c-plane to a-plane substrates. In reverse bias, both devices show a significant tunneling current originating from trap-assisted tunneling of charge carriers in the p^+n^+ region. This current is not a leakage current, as pin-diodes manufactured in the same process without overlapping doped regions show blocking behavior for these applied voltages [18]. Increasing the reverse voltage further, increases the current and in turn also the light emission. In the region marked with the green circle, the emission becomes visible by human eye and the spectral analysis of the emitted light was carried out.

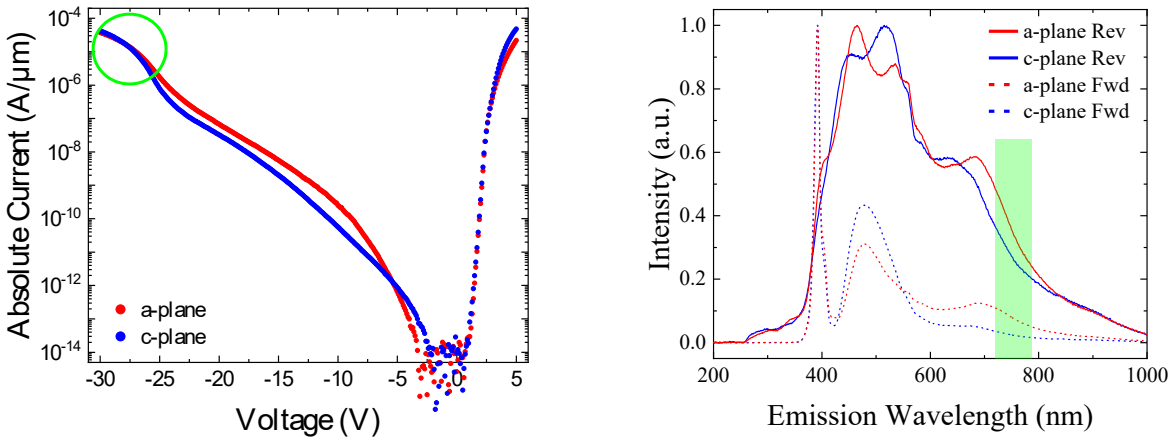

Fig. 5. Left: comparison of the I-V characteristics of the a-plane and c-plane tunneling didoes at room temperature. Right: electroluminescence emission spectra in forward (LED mode) and reverse biasing (tunneling mode) for the a-plane and c-plane tunneling diodes.

Electroluminescent Behavior at Room Temperature.

Electroluminescence spectra, as shown in Fig. 5 (right), were recorded under both forward and reverse bias conditions, revealing distinct emission characteristics for the two operating modes. Under forward bias, the devices operate in an LED-like regime, exhibiting a sharp emission peak at a wavelength corresponding to the bandgap energy, accompanied by additional defect-related emission at longer wavelengths [19].

In reverse bias, the emission originates predominantly from tunneling-assisted radiative recombination between donor and acceptor states in the co-implanted region. As donors and acceptors cannot occupy the same lattice site, tunneling is facilitated by the presence of an electric field and the resulting band bending. The emitted spectrum in this regime is broad, reflecting the variation in energetic separation between donor and acceptor levels, which depends on the spatial distance between individual donor-acceptor pairs in the biased device [20]. The small deviations in the local maxima and minima of the spectra of a-plane and c-plane samples are attributed to interference effects caused by the slightly different thicknesses of the overlying passivation layers.

As highlighted in the green box in Figure 5 (right), a significant portion of emission was also observed from 730 nm to 785 nm, which is the range used for off-resonant excitation of the V_{Si} defect, thus making these devices a promising co-integrated light source.

Electrical Properties at Cryogenic Temperatures.

As can be seen in Fig. 6, the devices remain operational at reduced temperatures down to 4 K. Light emission is still visible to the human eye, similar to operation at room temperature.

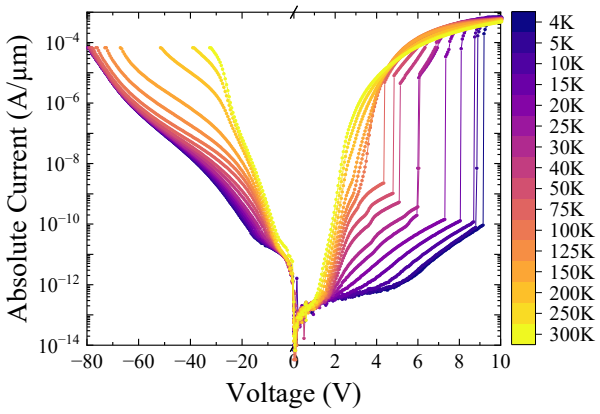

Fig. 6. I-V characteristics of the a-plane tunneling diode for different measurement temperatures. Note the different x-axis scaling for forward (LED mode) and reverse (tunneling mode) voltages. In reverse bias the current was limited to 10 mA to avoid extensive heating.

Under forward bias, the onset behavior changes markedly due to carrier freeze-out at low temperatures. In this regime, charge carriers must first be ionized by free carriers accelerated by the applied electric field [21] before contributing to conduction. This process is analogous to avalanche breakdown, but it requires significantly smaller fields because the energy difference between the dopant levels and their corresponding bands is relatively small. As the temperature decreases, a greater field energy is required for carrier activation, resulting in a higher voltage threshold for the re-ionization process. Once re-ionization occurs, the current rapidly transitions to the diode behavior as observed at room temperature. This transition is not associated with a heating effect; thermal effects occur on a different timescale and were investigated separately (not shown). Notably, the power levels at which this field-assisted re-ionization sets in are much lower than those associated with thermal effects.

In reverse bias, higher electric fields are necessary to achieve the same tunneling current as at room temperature, consistent with rising bandgap and thus breakdown voltage of the device at cryogenic temperatures [22].

Summary

CMOS-compatible fabrication processes, including ion implantation, thermal oxidation, and contact formation, were successfully transferred from c-plane to a-plane 4H-SiC wafers. pMOS transistors produced on a-plane wafers exhibited comparable I_{on}/I_{off} ratios and mobilities to c-plane devices, with a threshold voltage shift from −7.1 V to −12 V. Tunneling diodes fabricated on the a-plane wafers emitted broadband light with a substantial spectral component suitable for off-resonant excitation of silicon vacancy centers. This emission remained stable at cryogenic temperatures.

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