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# Isolation of Cumulative Heavy-Ion Induced Trench Degradation Effects within a Commercial 4H-SiC Double Trench MOSFET

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**Abstract.** Cumulative heavy-ion irradiation effects were investigated in a commercial 4H-SiC double trench MOSFET through a combination of cyclotron experiments and TCAD simulations. Devices were exposed to continuous $^{124}\text{Xe}^{35+}$ ion strikes at a linear energy transfer (LET) of 63 MeV·cm²/mg under drain biases from 100 to 400 V. Experimental results revealed the onset of permanent drain and gate leakage at voltages as low as 200 V, with degradation rates increasing by several orders of magnitude at higher bias. Post-irradiation measurements confirmed trench oxide rupture and source leakage path formation, establishing single-event leakage current (SELC) as the dominant degradation mechanism. In contrast, TCAD simulations of isolated ion strikes predicted catastrophic single-event burnout (SEB) only at or above 250–300 V, highlighting the critical role of cumulative damage processes that are not captured in single-strike models. These findings demonstrate that permanent leakage-driven degradation effectively extends the SELC zone beyond conventional SEB thresholds, reducing the safe operating area of trench-based SiC MOSFETs. The results have significant implications for derating strategies in space applications, where current SEB-focused guidelines may underestimate vulnerability, and highlight the need for radiation-hardening by device design to ensure long-term reliability.

## Introduction

Wide bandgap (WBG) semiconductors such as 4H-silicon carbide (SiC) have become critical enablers for next-generation high efficiency, temperature, and voltage power electronics. Compared to silicon (Si), SiC offers a critical electric field nearly an order of magnitude higher, a threefold higher thermal conductivity, and superior electron saturation velocity [1]. These material advantages allow SiC devices to operate with thinner drift layers and higher blocking voltages, enabling compact devices with lower conduction and switching losses. Consequently, SiC metal -oxide-semiconductor field effect transistors (MOSFETs) are increasingly displacing Si insulated gate bipolar transistors (IGBTs) in the 650–1700 V range, particularly in applications demanding high efficiency and fast switching.

Among SiC device topologies, the double trench MOSFET has emerged as a commercially relevant architecture due to its compact cell pitch and ability to shield the gate oxide from peak electric fields. Narrow cell geometries reduce specific on-resistance and chip area, while the lower gate configuration minimizes switching losses and provides resilience under fault conditions [2]. These advantages make trench MOSFETs attractive candidates for space systems, where efficiency directly translates into lower power budgets, reduced thermal management requirements, and decreased payload weight.

Despite these benefits, SiC power devices face significant challenges when exposed to the radiation environment of space, where single-event effects (SEE) induced by heavy ions or cosmic particles can compromise long-term reliability. The majority of qualification strategies have focused on preventing single-event burnout (SEB), a catastrophic mode of failure driven by localized avalanche breakdown and thermal runaway. Therefore, literature derating guidelines for SiC space applications typically emphasize maintaining safe operating voltages well below the SEB threshold [3, 4].

However, growing evidence suggests that cumulative SEE-induced degradation may occur well before catastrophic burnout, particularly in trench-based structures. SiC devices in space can be exposed to heavy-ion fluences exceeding $10^7$ particles/cm² with LET values above 60 MeV·cm²/mg over the course of a 10-year mission, making repeated strike effects a realistic concern [5]. Recent studies have documented the onset of single-event leakage current (SELC), defect generation, and gradual trench degradation under continuous irradiation [6-8]. These mechanisms may result in permanent leakage paths, compromised blocking capability, or degraded gate insulation - failure modes that do not manifest as immediate device destruction but can still render the component unsuitable for mission use. This evolving understanding challenges the adequacy of SEB-focused derating strategies for WBG devices.

In this work, we investigate cumulative SEE degradation in a commercial 4H-SiC double trench MOSFET through a combination of cyclotron irradiation experiments and Sentaurus TCAD simulations. Devices were subjected to continuous $^{124}\mathrm{Xe}^{35+}$ ion strikes at linear energy transfer (LET) of 63 MeV·cm²/mg, across a range of drain bias voltages. Experimental results reveal the progressive development of drain and gate leakage currents at voltages as low as 200 V, indicating the presence of permanent structural damage to both source and gate trenches. Complementary TCAD simulations reproduce transient strike dynamics, including current surges and local lattice heating, and help identify the vulnerable device features most responsible for degradation. By isolating the onset of cumulative degradation and contrasting experimental outcomes with simulated SEB thresholds, this study provides new insights into failure precursors in SiC trench MOSFETs.

## Methodology

The device selected for this study was a commercially available 750 V SiC double trench MOSFET. The trench-gate structure features a compact cell pitch with deep gate and source trenches, offering both conduction efficiency and oxide field shielding [2]. Prior to irradiation, the device underwent baseline electrical characterization to establish transfer characteristics and leakage behaviour, ensuring that subsequent degradation could be attributed solely to irradiation.

Heavy-ion experiments were carried out at the UCLouvain Cyclotron Facility, using a beam of $^{124}\mathrm{Xe}^{35+}$ ions with a LET of 63 MeV·cm²/mg. and ion penetration depth of approximately 73 μm in 4H-SiC, sufficient to traverse the full active region of the device. Devices were mounted in a vacuum chamber and biased in the off-state across a drain-source voltage range of 100 to 400 V while subjected to a constant ion flux, thereby replicating the conditions of repeated single-event strikes. The device testing board consisted of current limiting resistors placed on gate and drain side to protect the respective SMUs in case of explosive breakdown of the MOSFET under test, while a 1 nF coupling capacitor is used to ensure correct constant voltage biasing while the device is actively bombarded with heavy ion flux. These components are selected according to ESA standards for single-event effect testing [9]. Real-time monitoring of gate and drain leakage currents was performed throughout irradiation, allowing progressive degradation trends to be identified. Following irradiation, full current–voltage sweeps were repeated, including gate-source and drain-source leakage tests, as well as transfer measurements, to quantify permanent shifts in device behaviour. The total active flux seen by the device is calculated by the device active area of $6\times10^{-6}$ m².

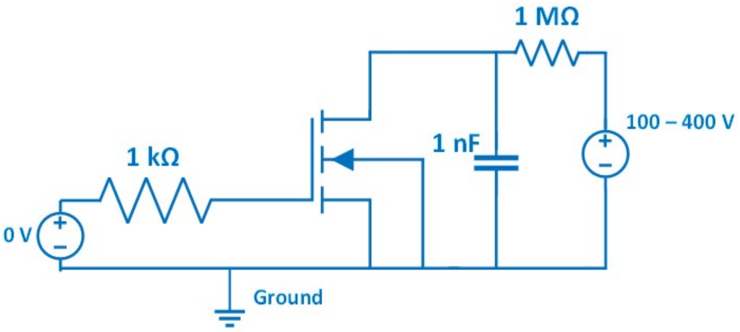

**Fig. 1.** Heavy ion board circuit schematic for commercial device testing.

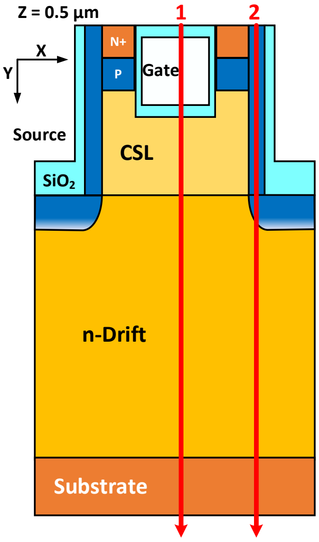

**Fig. 2.** Cross-sectional view of the commercial double trench MOSFET illustrating two simulated heavy ion strike paths: 1) at gate strike 2) at source strike.

Complementary single-event simulations were performed in Synopsys Sentaurus TCAD to compare the experimental conditions and isolate the underlying failure mechanisms. The simulated device structure was previously benchmarked and validated in a prior study [10], reproducing the key geometrical and doping profiles of the epitaxial drift layer, source/body regions, and trench oxides. The key parameters of the simulated device can be seen in table.1. Heavy-ion strikes were modelled as Gaussian electron–hole pair generation along a cylindrical track, calibrated to the experimental LET and penetration depth. Strike locations were varied at two key points of vulnerability: 1) at the gate trench and 2) at the source trench to examine the relative susceptibility of these regions, seen in Fig.2. Transient simulations were carried out with a time step up to 1 ns after heavy ion impact, capturing the resulting current surges and lattice temperature evolution under drain biases from 10 - 400 V.

This combined methodology enabled direct correlation between experimental degradation phenomena and simulated single-event dynamics, providing a framework to interpret the onset of leakage-dominated failure modes in the double trench architecture.

**Table 1.** Summary of key device design geometry and parameters.

| Symbol | Definition | Values | Units |
|---|---|---|---|
| $t_{CSL}$ | Charge storage layer thickness | 2.6 | µm |
| $t_{cell}$ | Cell pitch | 2 | |
| $t_{sub}$ | Substrate thickness | 140 | |
| $t_d$ | Drift region thickness | 6.8 | |
| $N_{CSL}$ | Charge storage layer doping | $5\times10^{16}$ | $cm^3$ |
| $N_d$ | Drift region doping | $1.5\times10^{16}$ | |
| $N_{sub}$ | Substrate doping | $1\times10^{19}$ | |
| $V_{th}$ | Threshold Voltage | 4.81 | V |
| $R_{on,sp}$ | Specific on-resistance | 1.69 | $m\Omega.cm^2$ |
| $BV_{max}$ | Max. Breakdown Voltage | 1001 | V |

## Experimental Results

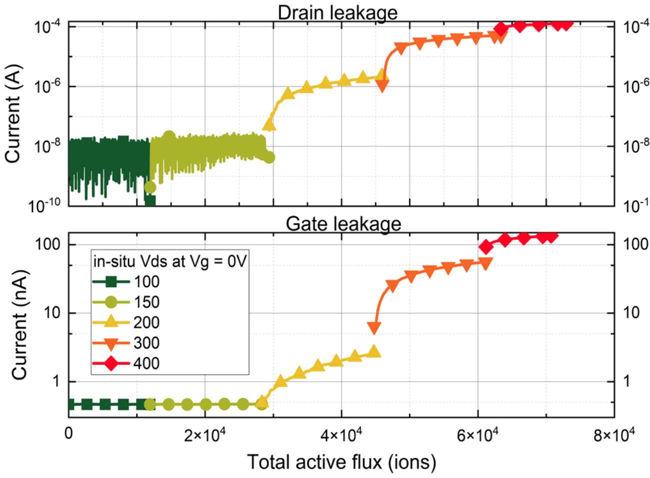

**Fig. 3.** Experimental drain and gate leakage currents of the commercial double trench MOSFET under cumulative heavy ion strikes at increasing blocking voltage (100 to 400 V).

The progressive evolution of leakage currents in the double trench MOSFET during cumulative heavy-ion irradiation is illustrated in Fig.3. At drain biases up to 150 V, the device exhibits stable behaviour with no measurable increase in gate or drain leakage. However, from 200 V onwards, degradation became apparent. Successive irradiation under these conditions results in a permanent rise in both gate and drain leakage currents, reaching values of approximately 140 nA and 120 µA, respectively, at the end of the exposure sequence (400 V). This behaviour is consistent with SELC phenomena reported in modern literature [6-8]. Even at lower 'safe operating' voltages there is device failure via the formation of permanent leakage pathways within the trench regions. One possible explanation for why there is no instantaneous destruction of the device could be due to the continuous heavy-ion irradiation flux. This creates a continuous high electric field beneath the gate, promoting charge trapping and gradual oxide degradation, forming leakage paths across the dielectric. This pre-damaged path allows charge dissipation at high voltages, limiting field build-up and preventing full SEB despite reaching the simulated burnout threshold. The comparison with a commercial diode response at the same experimental conditions in Fig.4 further emphasises this point: whereas the diode undergoes abrupt SEB with no intermediate degradation region, the trench MOSFET demonstrates progressive leakage-dominated failure. This suggests that oxide-influenced SELC is the primary limiting factor in trench-based structures.

The degradation rate extracted from cumulative irradiation testing is shown in Fig. 5, highlighting the increase in both drain and gate leakage pathways as a function of blocking voltage with each ion strike. At drain biases below 150 V, the degradation rate remains negligible, consistent with the absence of measurable leakage shifts in real-time monitoring. However, from 200 V upwards, both drain and gate degradation rates increase sharply with bias, with drain leakage progressing by nearly five orders of magnitude between 200 - 400 V. Gate degradation follows a similar trend, though at a lower absolute rate, reflecting the comparatively less stressed area of the gate trench oxide.

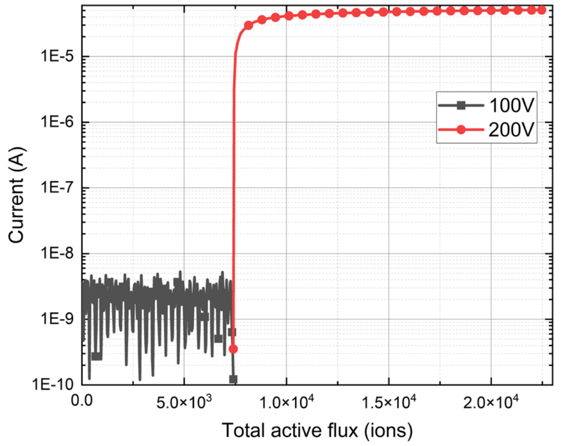

**Fig. 4.** Experimental leakage currents of a commercial diode under cumulative heavy ion strikes at increasing blocking voltage (100 to 200 V), showing clear SEB.

This behaviour indicates that permanent SELC damage effectively extends the safe operating area of the device into regions traditionally considered safe by SEB-based derating guidelines. In conventional single-event frameworks, the catastrophic burnout threshold defines the boundary of device survival. By contrast, in this device architecture, cumulative trench degradation introduces a zone of permanent leakage growth that precedes burnout, thereby reducing the effective safe operating area. In other words, even when catastrophic SEB is not triggered, the accumulation of SELC damage erodes device reliability at voltages well below the expected burnout threshold.

The manifestation of this cumulative degradation is further examined through post-irradiation I–V measurements. As shown in Fig.6, the pre-irradiation condition of the commercial MOSFET exhibits only a small leakage path dominated by the gate–drain overlap region. Following irradiation, a dramatic increase is observed, with both the gate–source and gate–drain characteristics rising into the mA range and displaying nearly identical behaviour. This convergence strongly indicates rupture of the gate trench oxide, establishing a direct conduction path across gate to drain through the oxide.

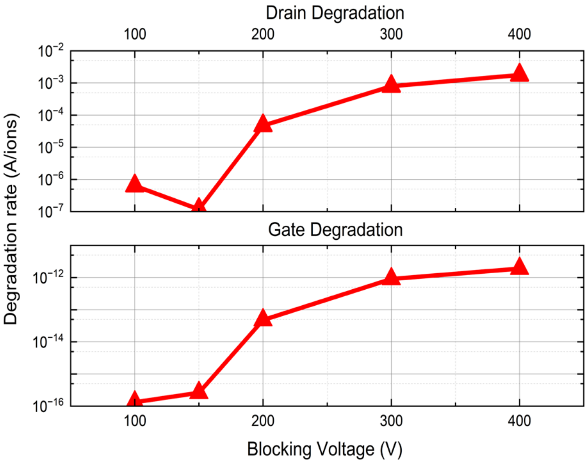

**Fig. 5.** Degradation rate (A/ions) of a) drain and b) gate of the commercial MOSFET with response to increasing blocking voltage (100 to 200 V).

Despite the clear trench rupture seen in Fig.6, the pre- and post-irradiation comparison of the transfer response in Fig.7 shows channel functionality. While the on-state current was reduced, the overall transconductance profile remained recognisable, demonstrating that gate control was not fully compromised. The most likely explanation is that rupture occurred locally within specific trench regions, rather than uniformly across the active area, leaving enough intact channel area for the device to sustain limited functionality.

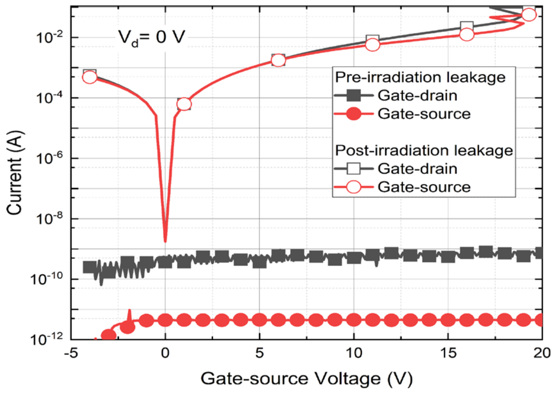

**Fig. 6.** Comparison of pre- and post-irradiation gate-drain and gate-source leakage current with gate-source voltage sweep between -5 to 20 V at $V_d = 0$ V.

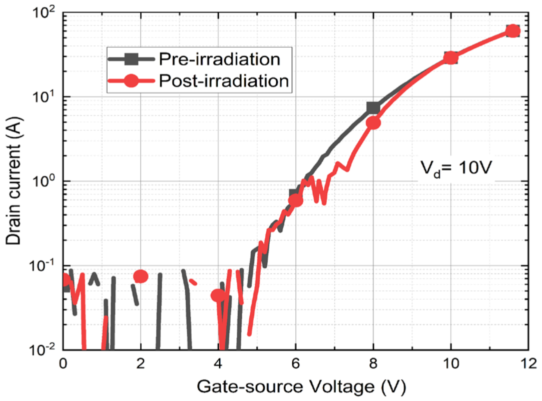

**Fig. 7.** Comparison of pre- and post-irradiation drain current with gate-source voltage sweep between 0 to 12 V at $V_d$ = 10 V.

## Simulation Results

To interpret the experimental degradation phenomena, transient single-event simulations were performed using the double trench MOSFET structure benchmarked against previously validated models. Throughout the simulations, the peak electric field was monitored during heavy ion strike, with the device not reaching the critical electric field at any blocking voltage up to 400 V.

Fig.8 shows the transient drain current induced by a single heavy-ion strike under different blocking voltages. At all blocking voltages 10 - 400 V, the ion strike produces a sharp current surge, which persists for several nanoseconds before decaying, irrespective of blocking voltage and heavy ion location (gate or source). However, the peak source current rises with blocking voltage, approaching 60 mA at 400 V. By contrast, the monitored gate current transient seen in Fig.9 shows minimal impact change at all blocking voltages. However, the gate heavy ion strike does increase the peak gate current by an order of magnitude due to the more charge being swept through the gate terminal. The rise in lattice temperature is the biggest indicator of thermal runaway within the device. In Fig.10, the simulated SEB threshold is 250 V for a source strike and 300 V for a gate strike. This is due to the more active sweep of charge through the gate terminal in the event of a gate strike. In the heavy ion events below the SEB threshold, the device temperature begins to reduce without thermal runaway, consistent with conventional single-strike expectations. This divergence highlights a key discrepancy: while simulations predict burnout only at or above 250 V, experimental results revealed permanent leakage degradation already at 200 V.

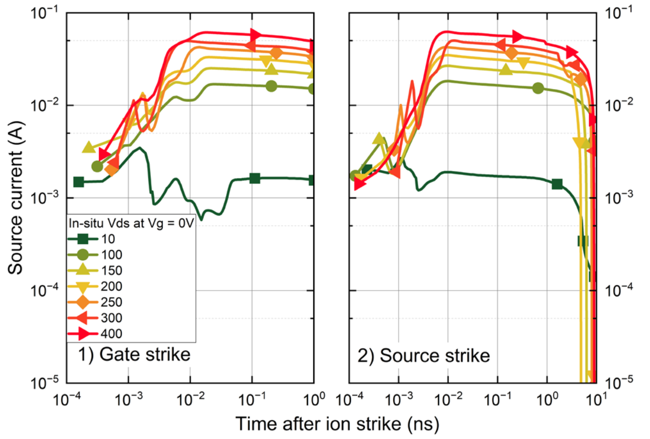

**Fig. 8.** Simulated $^{124}Xe^{35+}$ ion strike response for source leakage current at varying reverse bias voltage (10 to 400 V).

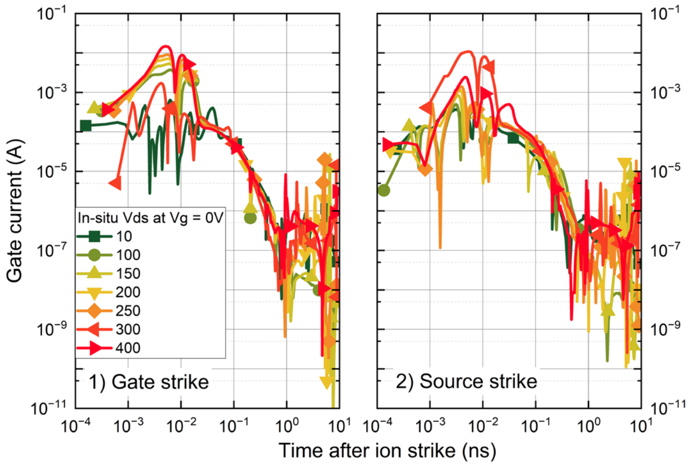

**Fig. 9.** Simulated $^{124}Xe^{35+}$ ion strike response for gate leakage current at varying reverse bias voltage (10 to 400 V).

The difference suggests that cumulative irradiation effects, mainly progressive oxide weakening and localized trench damage, reduce the effective failure threshold in practice. Because the present simulations model single isolated strikes, they do not capture the gradual degradation pathways observed experimentally. Nevertheless, the simulations identify the gate and source trenches as the most critical regions of vulnerability, supporting the interpretation that trench oxide rupture and source leakage paths govern the observed experimental failure modes.

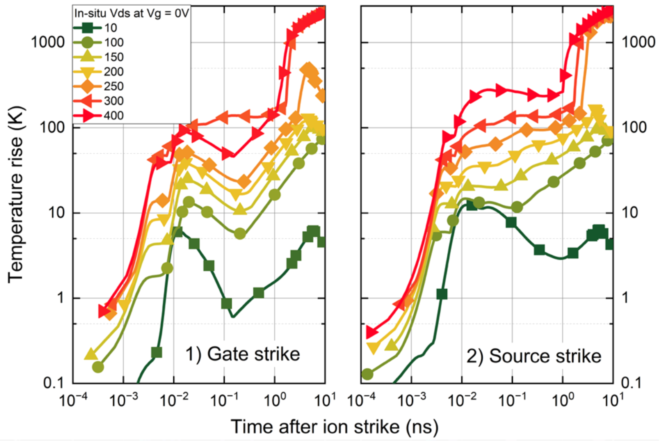

**Fig. 10.** Simulated $^{124}Xe^{35+}$ ion strike response for rise in lattice temperature from 300 K at varying reverse bias voltage (10 to 400 V).

## Conclusion

This work has demonstrated that cumulative heavy-ion irradiation induces progressive degradation in a commercial 4H-SiC double trench MOSFET, even at drain biases well below the simulated burnout threshold. Experimental testing revealed the onset of permanent drain and gate leakage at 200 V, with degradation rates increasing sharply at higher voltages. Post-irradiation measurements confirmed trench oxide rupture and source leakage path formation, establishing single-event leakage current SELC as the dominant degradation mode in this architecture.

Sentaurus TCAD simulations reproduced the transient current and thermal response of individual heavy-ion strikes, predicting catastrophic burnout only at or above 250–300 V. The divergence between simulation and experiment highlights the importance of cumulative irradiation effects, such as progressive oxide damage, which are not captured by single-strike models. Together, these findings confirm that the gate and source trenches are the most vulnerable features in double trench MOSFETs and that oxide-mediated SELC damage can extend the effective degradation zone beyond conventional SEB thresholds.

The implications for space applications are significant. Conventional derating strategies based solely on SEB thresholds may overestimate the safe operating area of trench-based SiC MOSFETs, as permanent leakage-driven damage can accumulate under realistic ion fluences long before catastrophic burnout occurs. Therefore, this work further supports the ongoing literature that derating strategies must be re-defined to better predict long-term reliability in space environments, and radiation-hardening by device design is required to push SiC into this market.

## References

[1] X. She, A. Q. Huang, O. Lucia, and B. Ozpineci, "Review of silicon carbide power devices and their applications," *IEEE Transactions on Industrial Electronics,* vol. 64, no. 10, pp. 8193-8205, 2017.

[2] P.M.Gammon. "Rohm Gen 4: a Technical Review." https://www.pgcconsultancy.com/post/rohm-gen-4-a-technical-review.

[3] J. L. Titus, "An updated perspective of single event gate rupture and single event burnout in power MOSFETs," *IEEE Transactions on nuclear science,* vol. 60, no. 3, pp. 1912-1928, 2013.

[4] A. Witulski *et al.*, "Single-event burnout of SiC junction barrier Schottky diode high-voltage power devices," *IEEE Transactions on Nuclear Science,* vol. 65, no. 1, pp. 256-261, 2017.

[5] W. Atwell, S. Koontz, and E. Normand, "Practical applications of cosmic ray science: Spacecraft, aircraft, ground based computation and control systems, and human health and safety," in *AIP Conference Proceedings*, 2013, vol. 1516, no. 1: American Institute of Physics, pp. 107-116.

[6] C. Martinella *et al.*, "Heavy-ion effects in SiC power MOSFETs with trench-gate design," *IEEE Transactions on Nuclear Science,* vol. 71, no. 8, pp. 1440-1446, 2024.

[7] C. Martinella *et al.*, "Heavy-ion microbeam studies of single-event leakage current mechanism in SiC VD-MOSFETs," *IEEE Transactions on Nuclear Science,* vol. 67, no. 7, pp. 1381-1389, 2020.

[8] H. G. de Medeiros *et al.*, "Exploring the relation between SEEs caused by heavy-ion irradiation and defects in SiC devices," *IEEE Transactions on Nuclear Science,* 2025.

[9] ESCC, "Single event effects test method and guidelines, ESCC Basic Specification No. 25100," ed.

[10] K. Melnyk, P. M. Gammon, A. B. Renz, Q. Cao, V. A. Shah, and M. Antoniou, "Analysis and Performance Trade-Offs of State-of-the-Art 4H-SiC Trench MOSFET Technology," in *2024 IEEE Energy Conversion Congress and Exposition (ECCE)*, 2024: IEEE, pp. 6764-6770.