Key Engineering Materials
ISSN: 1662-9795, Vol. 1056, pp 79-83
doi:10.4028/p-pv3S4F

Submitted: 2025-09-13
Revised: 2025-12-25
Accepted: 2026-01-31
Online: 2026-05-20

In-Situ Measurement of the Gain Stage of a SiC JFET Operational Amplifier under Gamma Ray Irradiation

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Keywords: SiC, JFET, operational amplifier, gamma ray, wide bandgap semiconductors, integrated circuit, harsh environment.

Abstract. In this study, we conducted in-situ measurements on a SiC JFET operational amplifier operating under gamma-ray irradiation. It shows that the radiation did not affect the output waveform or voltage gain, but shifted the output offset voltage. This shift may result mainly from holes generated by irradiation and trapped in the oxide layer, which modified the I-V characteristics of the level-shifting diodes. It can be compensated by applying bias voltage, and it may also be prevented by optimizing the diode structure and/or circuit topology.

Introduction

Silicon carbide (SiC) is recognized for its outstanding material properties, including high thermal conductivity, high breakdown electric field, and radiation hardness [1]. These attributes make SiC devices promising candidates for next-generation electronics in extreme environments such as aerospace missions and nuclear instrumentation systems. Recent advances have enabled the fabrication of SiC-based MOSFETs, JFETs, and ICs with high temperature and radiation tolerance [2-4]. However, only a few studies have investigated irradiation effects in operating conditions [5,6]. For circuits deployed in actual systems, operation under irradiation is inevitable, and understanding real-time behavior is critical for ensuring stable performance.

In this work, we performed in-situ characterization of a SiC JFET operational amplifier during γ-ray irradiation. The results indicate that while the irradiation had no observable effect on the output waveform or voltage gain, it caused a shift in the output offset voltage. This shift is attributed primarily to irradiation-induced holes trapped in the oxide layer, which alter the I–V characteristics of the level-shifting diodes. The offset shift can be effectively compensated by adjusting the bias voltage and may be mitigated in future designs through optimization of the diode structure and/or circuit topology.

Experimental

The SiC JFET was fabricated using ion implantation to form a stripe-shaped n-type channel region surrounded by p+-type gate regions in n- epitaxial layer ($3 \times 10^{16}\mathrm{cm}^{-3}, 5\mu\mathrm{m}$) [7]. Figure 1(a) and (b) show the schematic draw of our lateral n-type SiC JFET and the SEM cross-sectional image of the channel region. Figure 1(c) and (d) show the transfer and output characteristics, respectively. The device operates in normally-on mode, with a threshold voltage of -3.7V. At $V_{\mathrm{GS}} = 0\mathrm{V}$ and $V_{\mathrm{DS}} = 10\mathrm{V}$, the transfer conductance is about $g_m \cong 30\mu\mathrm{S}$ while the output resistance $r_o \cong 5\mathrm{M}\Omega$. Their product gives the maximum voltage gain in the common source amplifier, that is $A_v^{max} = g_m r_o \cong 150$.

As shown in Figure 2(a), the operational amplifier consists of three stages: differential input stage, gain stage, and source-follower output stage (buffer stage). Normally-on JFETs with gate-source short connections were used as current sources and active resistors, while PN junction diodes served as level shifters. To facilitate stage-by-stage evaluation, each stage was wire-bonded and connected to external pads on the package, avoiding multilayer interconnects (Fig. 2(b)).

Figure 2(c) shows the Bode plot, *i.e.*, the voltage gain and phase as a function of frequency, for the gain stage, where the supply voltages are set to be $V_{\mathrm{DD}} = 20\mathrm{V}$ and $V_{\mathrm{SS}} = -20\mathrm{V}$, the bias voltage V_{Bias2} to be from -14V to -15V, and the input signal amplitude is 0.1V. The DC gain is about 35dB and the cutoff frequency is around 1kHz. Red and light blue marks show the data obtained before irradiation and after the total dose of 50kGy. It shows that the properties are unchanged.

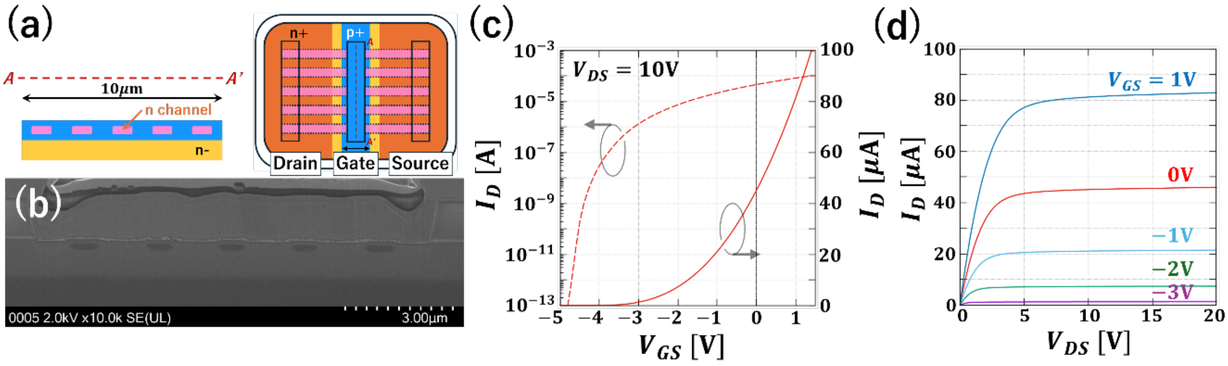

Fig. 1. (a) Schematic draws of the lateral n-type SiC JFET. Left: cross-sectional view. Right: top view. (b) Cross-sectional SEM image of SiC JFET channels. (c) Transfer characteristics of a normally-on SiC JFET at V_{DS}=10V. Solid and dotted lines indicate linear (right axis) and log (left axis) plots, respectively. The drain current at V_{GS}=0V is about 45μS. (d) Output characteristics of a normally-on SiC JFET from V_{GS}=-3V to 1V.

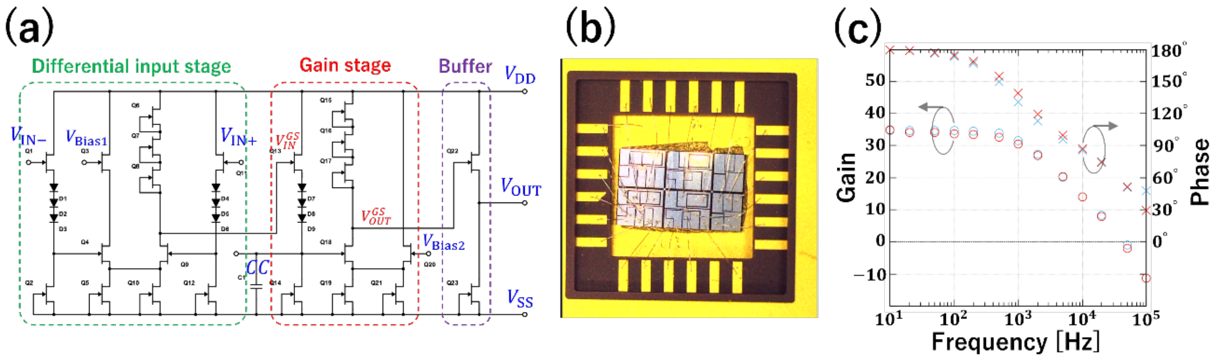

Fig. 2. (a) Circuit diagram of the n-type SiC JFET Operational Amplifier (OpAmp) with differential input, gain and buffer stages. (b) Picture of a wire bonded SiC JFET OpAmp. (c) Bode plot for the gain stage of SiC JFET OpAmp before (red) and after (light blue) 50kGy gamma-ray irradiation. Left axis: gain (circles). Right axis: phase (cross marks).

Gamma-ray irradiation was performed at the Takasaki Institute for Advanced Quantum Science (QST) using a Co-60 source with a dose rate of 2.17kGy/h under room temperature, atmospheric conditions, and normal room-light laboratory conditions. The packaged SiC OpAmp was mounted on a printed circuit board and connected to external instruments via 10 m cables, enabling real-time monitoring outside the irradiation chamber. Input signals, supply voltages, and output signals were recorded continuously during the irradiation.

Results

Figures 3(a) and (b) show the input waveform (yellow) and output waveform (light blue) before γ-ray irradiation and 10 minutes after the start of irradiation. The input signal was a 100 Hz sine wave with an amplitude of 0.1 V, and the circuit was operated with a supply voltage of ±20 V and a bias voltage of −14 V. No increase in output waveform noise or change in voltage gain was observed during irradiation. In contrast, the output offset voltage decreased by approximately 2 V due to irradiation.

Figure 3(c) shows the time evolution of the offset voltage shift. The offset voltage dropped sharply immediately after the start of irradiation and then its rate of change became more gradual after 20 minutes. After the 60-minute irradiation was completed, the offset voltage slowly recovered, reaching a value approximately 1.2 V below its original level about one hour after the end of irradiation (corresponding to a recovery ratio of roughly 40%).

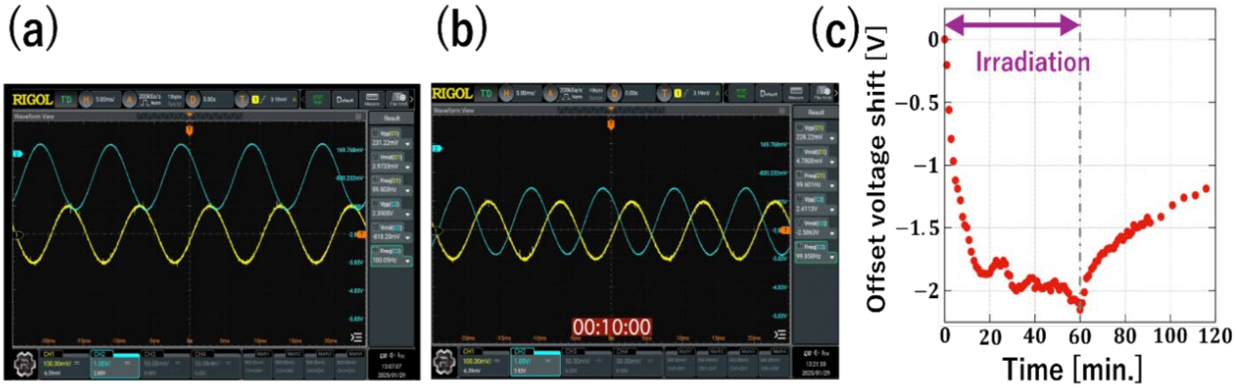

Fig. 3. (a) Snapshot of input (yellow) and output (light blue) waveforms before the gamma-ray irradiation. (b) Snapshot of waveforms during the gamma-ray irradiation. The output offset voltage decreased by approximately 2 V due to irradiation. (c) Time evolution of the offset voltage shift. The irradiation starts at 0 min. and ends at 60 min.

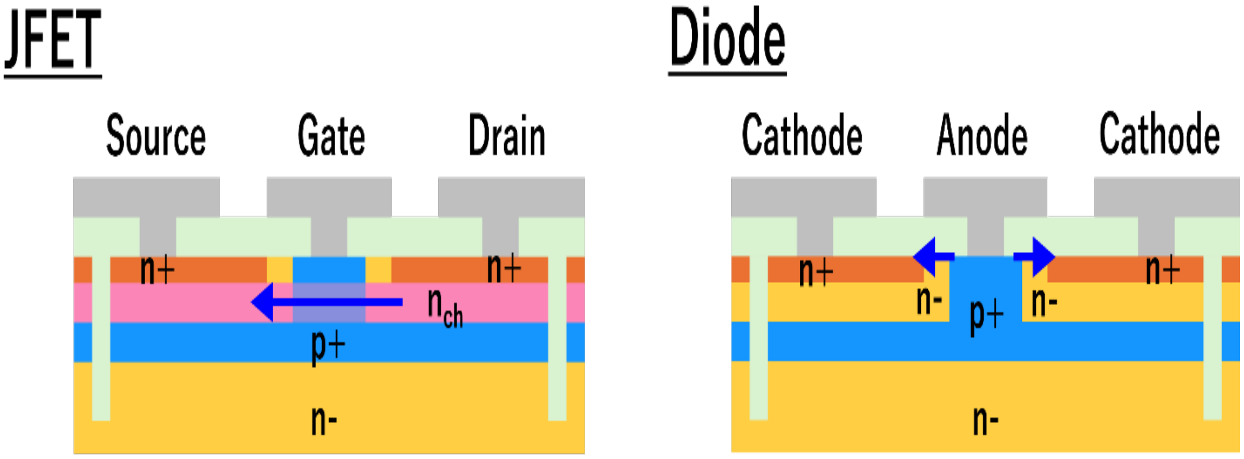

Fig. 4. Lateral schematic of the JFET (left) and level-shifting diodes (right). While current (indicated by blue arrows) flows through the bulk region in the JFET, in the level-shifting diodes it mainly flows near the SiC/SiO_2 interface within the n^- layer.

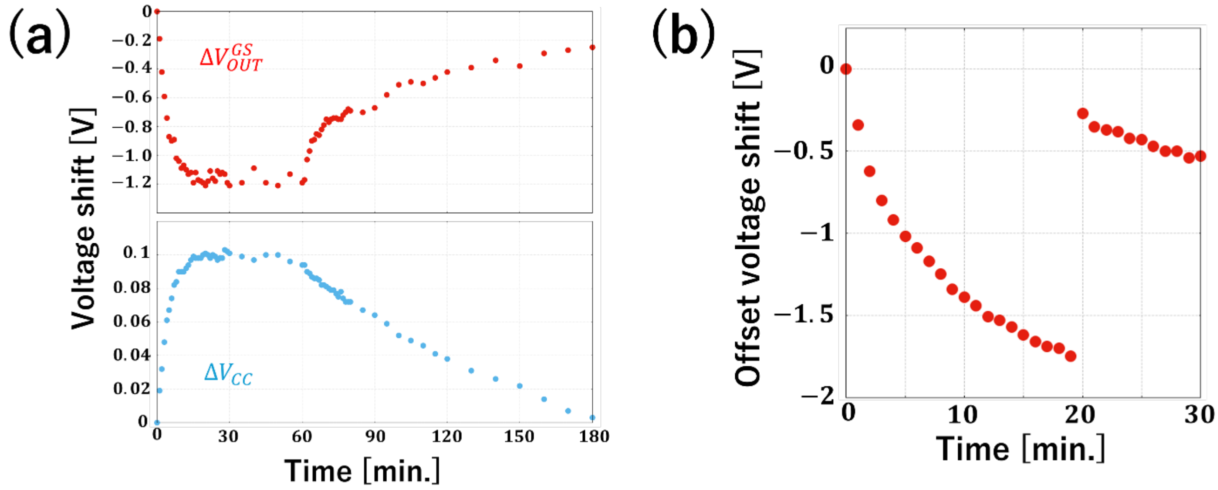

Fig. 5. (a) Output offset voltage (upper panel) and the node voltage after level shifting (lower panel) measured simultaneously as a function of time. The irradiation starts at 0 min. and ends at 60 min. (b) the time evolution of the output offset voltage when the bias voltage was increased by 0.1 V, 20 minutes after the start of irradiation.

Discussion

Now let us discuss the possible cause of the output offset shift. Figure 4 shows a lateral schematic of the JFET and level-shifting diodes that constitute the gain stage. While current (indicated by blue arrows) flows through the bulk region in the JFET, in the level-shifting diodes it mainly flows near the SiC/SiO_2 interface within the n^- layer.

During γ-ray irradiation, electron–hole pairs are generated in the SiC bulk, at the SiC/SiO_2 interface, and in the SiO_2 bulk, and these carriers are separated by the electric field present between the anode and cathode electrodes in diodes. Among them, the holes trapped in defects within the SiO_2 bulk are considered to be the least likely to be collected by the electrodes. When these holes accumulate near the interface, the band bending at the SiC/SiO_2 interface in the n^- layer becomes more pronounced, which increases the electron concentration near the interface and consequently reduces the forward resistance of the diode.

As a result, for a given current, the voltage drop across the diode decreases under irradiation. This reduction in voltage drop causes the post-level-shift node potential in the gain stage circuit to increase. Meanwhile, the differential input on the opposite side is fixed by the bias voltage, leading to an imbalance in the differential pair and an increase in the current through the left-hand path. Since the JFET located at the upper part of the left-hand path operates as an active resistor, the increased current results in a larger voltage drop across this element, which in turn lowers the output potential.

Figure 5(a) shows the output offset voltage (upper panel) and the node voltage after level shifting (lower panel) measured simultaneously as a function of time. It can be seen that the decrease in the output offset voltage correlates with the increase in the post-level-shift node voltage, supporting the above discussion.

Finally, figure 5(b) shows the time evolution of the output offset voltage when the bias voltage was increased by 0.1 V, 20 minutes after the start of irradiation. These results indicate that the shift of the output offset voltage can be compensated by a small adjustment of the bias voltage, corroborating that the observed phenomenon is primarily caused by the change in the voltage drop across the diodes.

Summary

In this study, we performed in-situ measurements of a SiC JFET operational amplifier under gamma-ray irradiation. The results indicate that radiation exposure did not affect the output waveform or voltage gain but causes a shift in the output offset voltage. This shift is likely due to holes generated by irradiation and trapped in the oxide layer, which altered the I-V characteristics of the level-shifting diodes. The offset shift can be compensated by applying an appropriate vias voltage and may also be mitigated through optimization of the diode structure and/or circuit topology.

Acknowledgement

This work was partially supported by the commissioned research fund provided by F-REI(JPFR25010501), and JSPS KAKENHI (S), Grant Number JP24H00035.

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