

1200V Lateral SiC Schottky Diode Radiation Hardness Enhancement

Z. Yuan^{1,a*}, V. Kotagama^{1,b}, B. Zhou^{1,c}, P. Gammon^{1,d}, M. Antoniou^{1,e*}

¹School of Engineering, University of Warwick, Coventry, CV4 7AL, UK

^aZhaoxue.Yuan@warwick.ac.uk, ^bviren.kotagama@warwick.ac.uk, ^cBailing.zhou@warwick.ac.uk,
^dp.m.gammon@warwick.ac.uk, ^eMarina.Antoniou@warwick.ac.uk

Keywords: Silicon Carbide, Schottky diode, Lateral device, RESURF device, Radiation hardness, Single event effect, Single event burnout.

Abstract. Radiation-hardened SiC power devices are essential to prevent leakage degradation and catastrophic failures such as SEE and SEB. Lateral device structures lower the risk of contact shorting by providing greater physical separation between conductive regions. Wider device geometries also improve radiation tolerance, as larger dimensions can accommodate charge buildup with less effect on device performance. In addition, RESURF structures enhance robustness by shifting the high electric field into the bulk, which reduces the impact of radiation-sensitive interface states on breakdown.

Introduction

Spaceborne electronics are continuously exposed to radiation from galactic cosmic rays, solar particle events, and trapped particles in Earth's magnetic field. These radiation sources induce several forms of degradation in semiconductor devices, including Total Ionizing Dose (TID), Displacement Damage (DD), and Single-Event Effects (SEE)[1]. TID causes cumulative charge trapping and interface state generation caused by prolonged exposure to ionize radiation, leading to shifts in threshold voltage and increased leakage current. DD introducing lattice defects introduced by high-energy particles such as neutrons or protons, which degrade carrier mobility and lifetime. SEE as a Transient or destructive events triggered by a single energetic particle[2]. Depending on severity, SEEs may result in soft errors like single-event upset (SEU), where a logic state is flipped, or hard errors such as single-event burnout (SEB), which permanently damages the device[3].

The impact of SEE on semiconductor device depend strongly on the *Linear Energy Transfer (LET)* of the particle, as well as *device biasing*, and *circuit layout*[4]. LET represents the energy deposited per unit path length as an ion traverses the semiconductor and is typically expressed in units of MeV·cm²/mg[5]. Typically, the LET value that a device can tolerate, and the single-event burnout (SEB) threshold voltage are critical parameters in assessing radiation resilience[6]. For instance, a 1200 V-rated SiC power MOSFET exhibits an SEB threshold voltage of approximately 330 V when subjected to a LET of 20 MeV·cm²/mg[7].

A reverse-biased PN junction struck by a heavy ion undergoes multiple phases, including charge deposition[6], transient current flow, and potential device failure with leakage current degradation as a key signature. The applied voltage bias strongly influences these effects: under higher reverse bias, the electric field in the depletion region is stronger, which accelerates carrier separation and increases the likelihood of avalanche multiplication. This enhances the peak transient current generated by the ion strike, potentially triggering destructive single-event effects such as SEB. Conversely, at lower bias, the electric field is weaker, reducing the multiplication effect but increasing the collection time for carriers, which can lead to slower recovery and elevated transient leakage.

Device structures can be optimized to enhance charge collection efficiency and suppress parasitic effects, thereby increasing the SEB threshold voltage. Additionally, selecting appropriate materials and doping profiles can mitigate the impact of high-LET radiation, ensuring reliable operation in space environments.

Lateral device structures are particularly attractive in this context, as they inherently avoid contact shorting (Fig.1) and can be scaled laterally to provide additional current drive, thereby compensating for transient charge collection during radiation strikes.

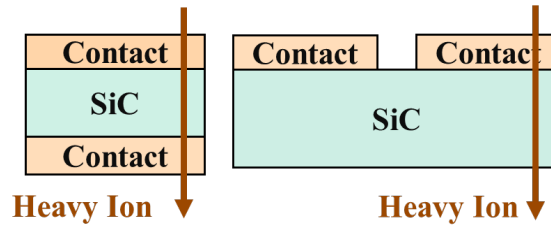


Fig. 1. Comparison between vertical device (left) and lateral device (right) under heavy ion strike.

For high-voltage applications, reduced surface field (RESURF) structures are widely employed due to their ability to distribute the electric field laterally and vertically, thereby improving breakdown performance[8]. A conventional RESURF device typically relies on a uniformly doped N-type drift region (Fig.2), which suffers from excessive leakage current and limited breakdown voltage under edge-related field crowding[9]. To overcome these issues, advanced termination schemes such as field plates and corner protection structures have been proposed[10]. More recently, the two-zone RESURF approach has been introduced, in which vertically stacked N-regions with different doping concentrations are employed[11]. This configuration enhances electric field control and significantly improves breakdown voltage, although it comes at the expense of higher on-resistance due to the presence of lightly doped drift regions.

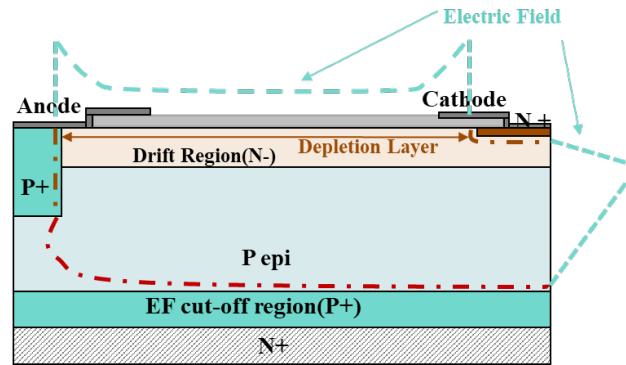


Fig. 2. RESURF device cross section with Electrical Field and depletion region.

Process

In the optimization of RESURF-based lateral devices, a *Two-Zone (TZ)* structure is introduced to generate an additional electric field peak, thereby improving the breakdown voltage compared with a conventional *Single-Zone (SZ)* design. In the SZ device, both Zone-1 and Zone-2 share the same doping concentration, which limits the degree of electric field modulation and results in lower breakdown capability. In contrast, the TZ structure employs a lightly doped Zone-1 combined with a more heavily doped Zone-2, creating an auxiliary electric field peak (Fig.5) that enhances depletion and supports higher voltage blocking (Fig.4)

Further improvement is achieved with the *Two-Zone P-ring (TZP)* structure, where a P-ring is implemented at the anode corner to suppress leakage current, while a highly doped bottom layer in Zone-1 compensates for the resistance introduced by the additional field-control features. This combined approach enables both reduced leakage and maintained on-resistance, offering an effective trade-off between breakdown voltage and conduction loss.

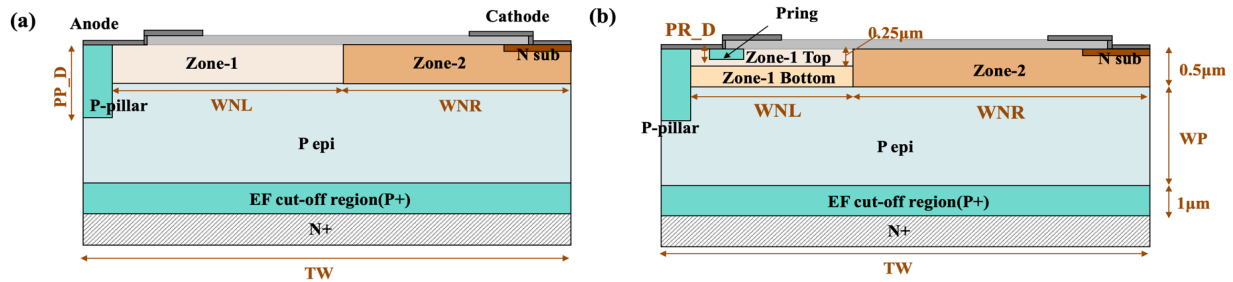


Fig. 3. (a) Layout of TZ RESURF SBD (b) Layout of TZP RESURF SBD.

The designed device employs a P-type epitaxial layer with a doping concentration of $5 \times 10^{15} \text{ cm}^{-3}$, thickness of $11 \mu\text{m}$, and width TW of $22 \mu\text{m}$. This structural Table 1, providing a reference for design optimization and comparison with alternative RESURF- configuration supports a breakdown voltage of approximately 1700 V, while maintaining an on-resistance as low as $20 \text{ m}\Omega \cdot \text{cm}^2$. Such performance highlights the effective trade-off achieved between high-voltage blocking capability and low conduction loss, which is essential for wide-bandgap power devices intended for both terrestrial and space applications. The structural parameters of the device are summarized in based architectures.

Table 1. Dimensions of the Single-Zone, Two-Zone and Two-Zone-P ring RESURF SBDs.

Property	Value(μm)	Property	Value(μm)
WP	11	WNL	7.5/ 9/ 10.75
TW	22	WNR	14/ 12.5/ 10.75
P Ring width	1	Oxide thickness	0.2
P-pillar Depth	2.5		

Result

Compared with the SZ and TZ structures, the proposed TZP device exhibits a clear advantage by suppressing leakage current while maintaining a high breakdown voltage (BV) and achieving a reduced on-resistance (R_{on}) (Fig.4). The incorporation of the P-ring at the anode corner effectively blocks potential leakage paths, thereby improving off-state performance without compromising conduction characteristics in the on-state.

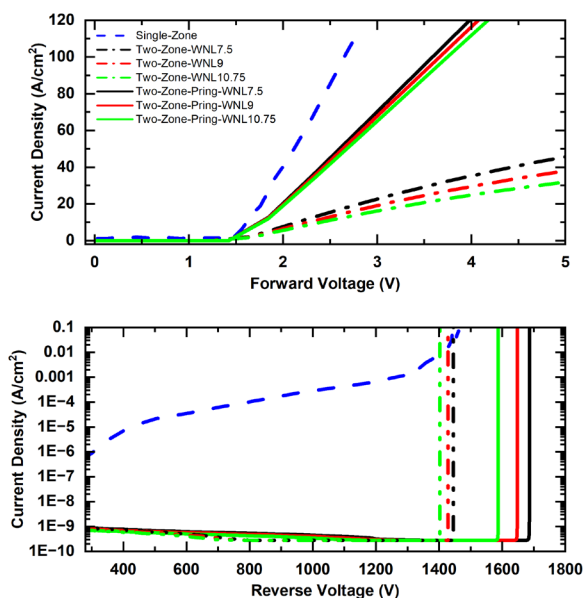


Fig. 4. On-state and off-state characteristics of SZ (dotted), TZ (solid), and TZP (dashed).

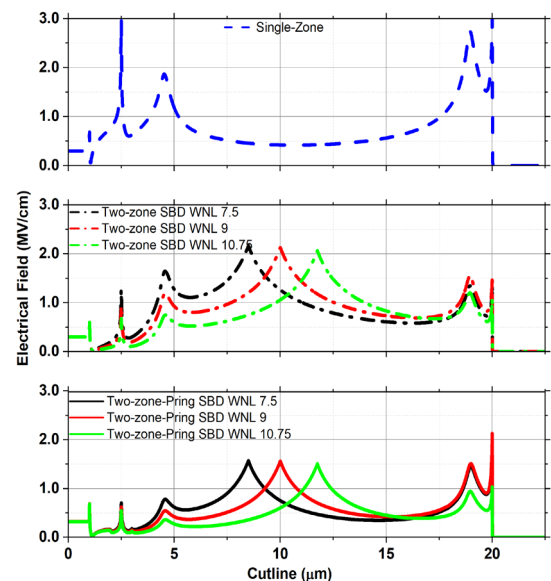


Fig. 5. Off-state lateral surface electric field of RESURF SBDs (SZ, TZ, TZP) before avalanche, 10 nm below the interface.

The incorporation of TZ and TZP structures leads to a more uniform electric field distribution, which facilitates faster recovery after irradiation. As shown in Fig.6, under an LET of $60 \text{ MeV}\cdot\text{cm}^2/\text{mg}$ and a reverse bias of 1000 V, when the ion strike occurs at the device center (the location of the middle electric-field peak, corresponding to the boundary between Zone-1 and Zone-2), the TZP device shows only a 300 K temperature rise. In contrast, the SZ and TZ counterparts exhibit much larger increases of approximately 1500 K and 400 K, respectively. The enhanced field control in the TZP structure effectively suppresses localized field crowding, thereby reducing peak temperature rise and limiting excess leakage current following an SEE event, highlighting its potential for deployment in radiation-intense environments such as space applications.

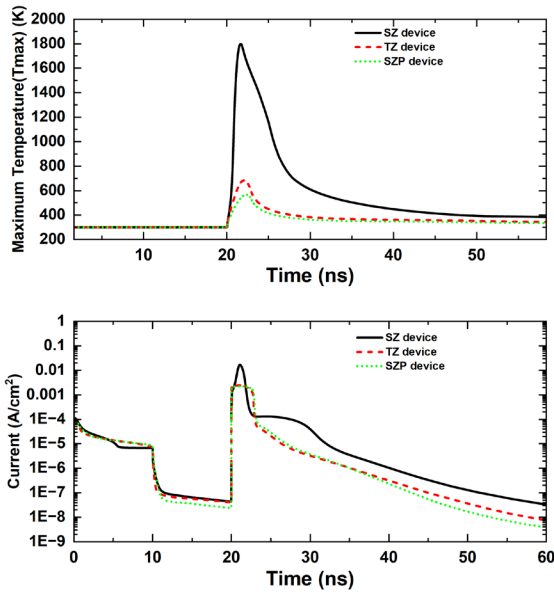


Fig. 6. Temperature and leakage current of the SZ, TZ and TZP after SEE.

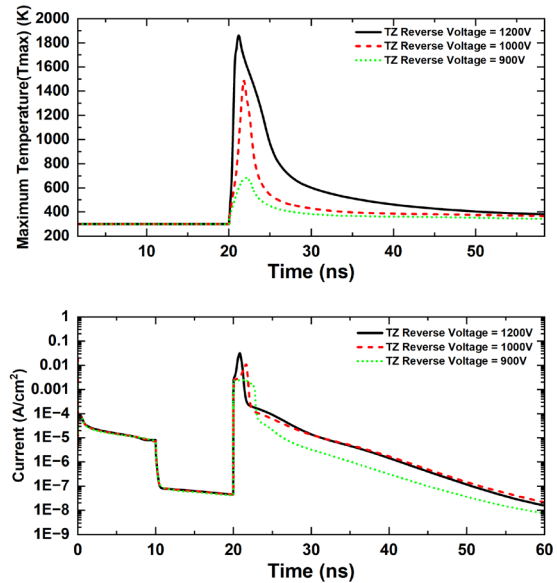


Fig. 7. Temperature and leakage current of the TZ device under different reverse bias voltages.

At higher reverse bias ($>1000\text{V}$), the electric field (EF) increase accelerates the separation and collection of electron and hole pairs generated by the ion strike. In Fig.7, when blocking voltage is 1200V this rapid charge separation improves transient current response, also induces stronger energy dissipation within the lattice, resulting, the localized lattice temperature rises significantly and caused higher leakage current, increasing the likelihood of thermal runaway and device degradation.

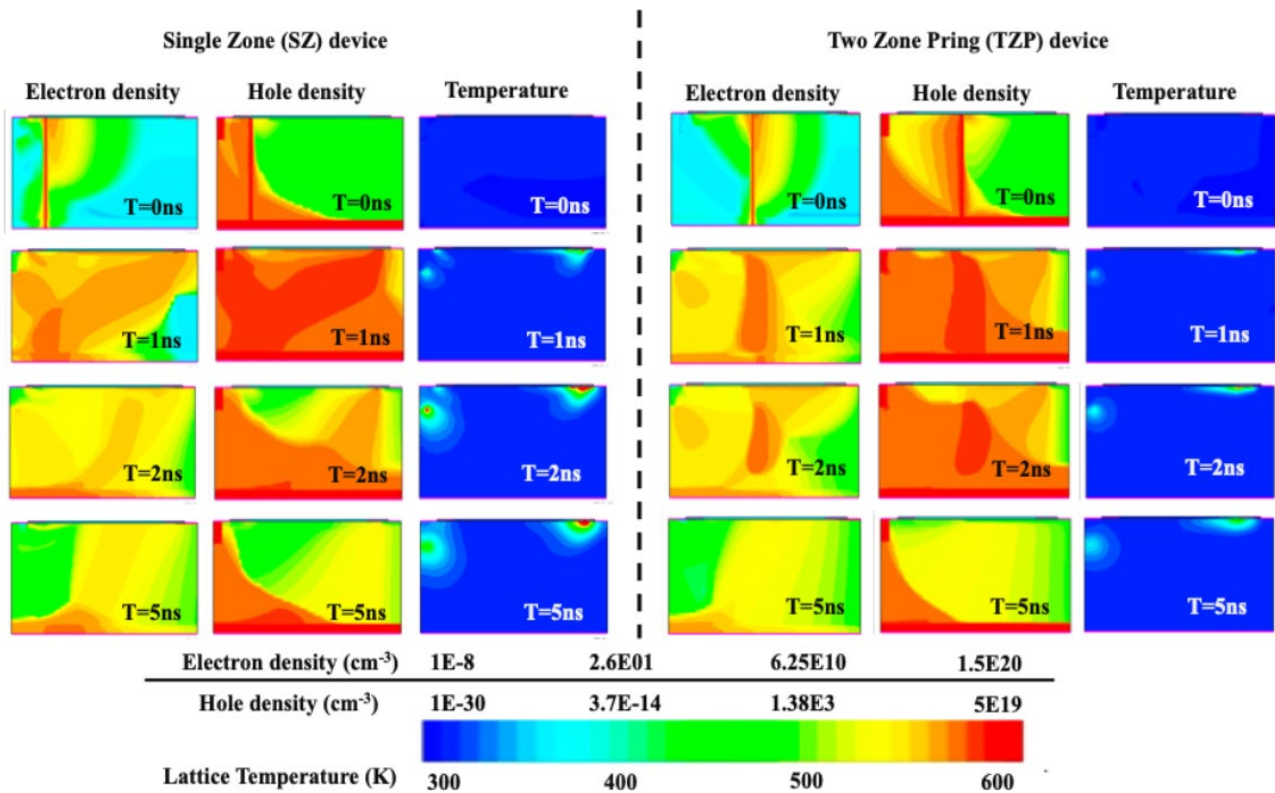


Fig. 8. Electron and hole density distributions, together with lattice temperature, at 0ns, 1ns, 2ns, and 5ns after an SEE strike for both SZ and TZP devices.

Fig.8 illustrates the evolution of electron and hole density distributions, as well as the lattice temperature, at different times following an SEE strike. The results show that the highest temperature rise occurs in the P-pillar and N⁺ regions. These areas are particularly weak because the localized charge deposition and strong electric field concentration accelerate carrier multiplication and heat generation, which can potentially lead to thermal runaway or permanent device damage. Compared with the SZ device, the TZP structure shows lower peak temperature and more confined carrier distribution, indicating improved robustness against SEE strike.

The performance of lateral TZ and TZP RESURF devices is strongly influenced by the doping concentration and depth of the P-ring at the anode corner. In Fig.9 and Fig.10, increased P-ring doping and depth have a direct impact on the peak electric field at the anode corner following a heavy ion strike, significantly reducing localized field crowding and lowering the associated peak electric field.

In addition, increasing the P-ring depth not only improves electric field modulation but also contributes to reducing the maximum lattice temperature following heavy-ion strikes. By mitigating localized field crowding at the anode corner, a deeper P-ring suppresses hot-spot formation, thereby lowering the risk of thermal runaway and enhancing the device's resilience to single-event effects. However, this improvement comes at the cost of increased hole injection into the drift region, which raises the device's on-resistance (from 21.07mΩ·cm² to 25.13mΩ·cm² with P ring depth changed from 0.05μm to 0.25μm).

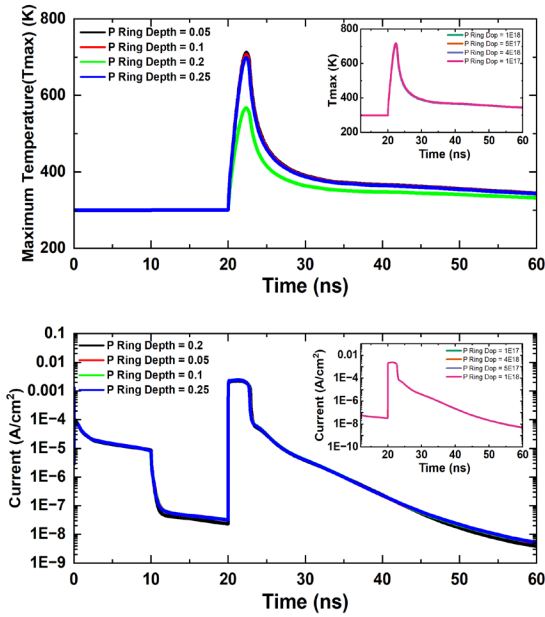


Fig. 9. Temperature and leakage current evolution in the TZP device after SEE, depend on P-ring doping concentration and depth at 1000V blocking voltage.

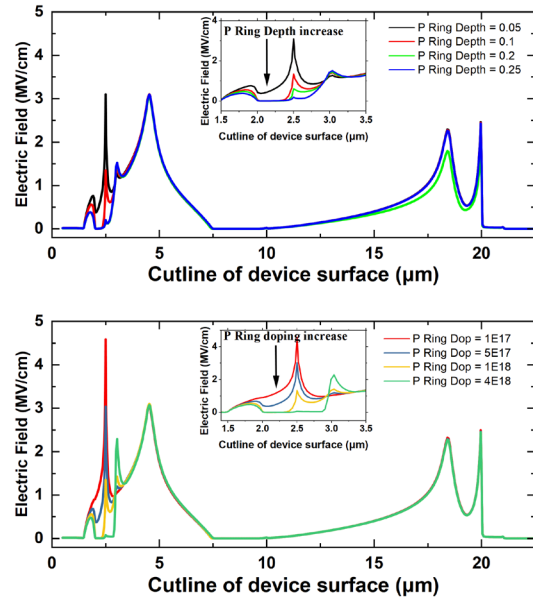


Fig. 10. Lateral surface electric field of the TZP SBD at 1 ns after SEE strike, extracted 10 nm below the interface at 1000V blocking voltage.

The Contact Open Length (COL) plays a critical role in balancing conduction and recovery performance in lateral RESURF devices. Increasing the COL allows more current to flow through the contact, thereby reducing the on-resistance (R_{on}) and enhancing forward conduction. As shown in Fig.12, increasing the COL from $1\mu\text{m}$ to $5\mu\text{m}$ reduces the device resistance from approximately $20\text{m}\Omega\cdot\text{cm}^2$ to $11\text{m}\Omega\cdot\text{cm}^2$, demonstrating the strong influence of contact geometry on conduction performance.

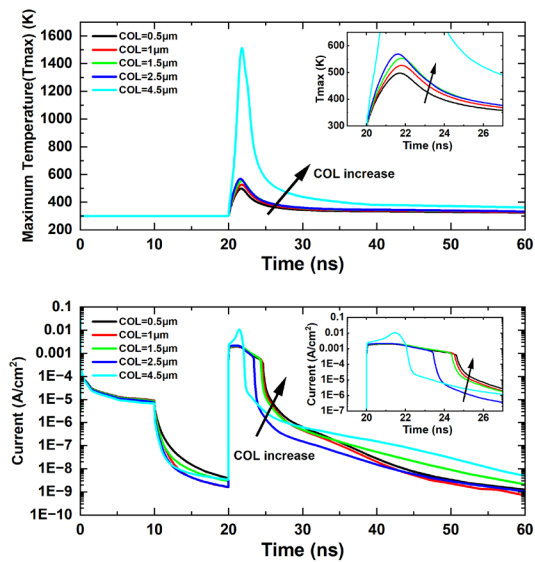


Fig. 11. Temperature and leakage current variation over time in the double RESURF device with differences by COL after SEE at 1000V blocking voltage.

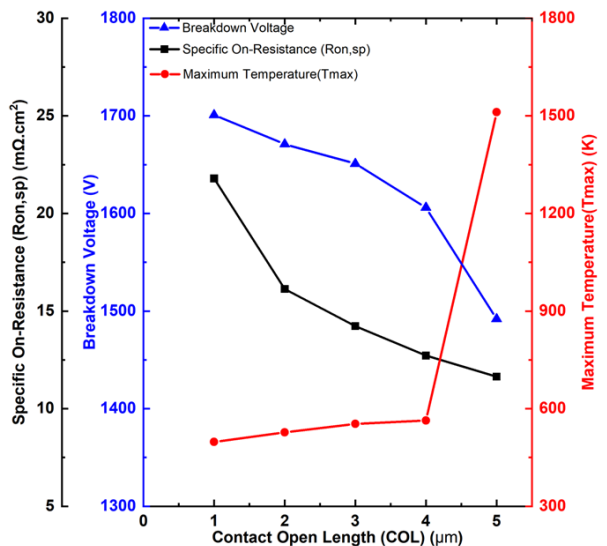


Fig. 12. R_{on} , BV, and maximum temperature of the double RESURF device after SEE, with variations distinguished by column (COL).

However, as shown in Fig.13, longer COL can impede the efficient collection of injected holes back to the P+ region, potentially affecting charge recovery and post-event leakage suppression. Careful optimization of COL is therefore essential to achieve a compromise between low Ron and effective off-state performance, particularly under radiation-induced transient conditions.

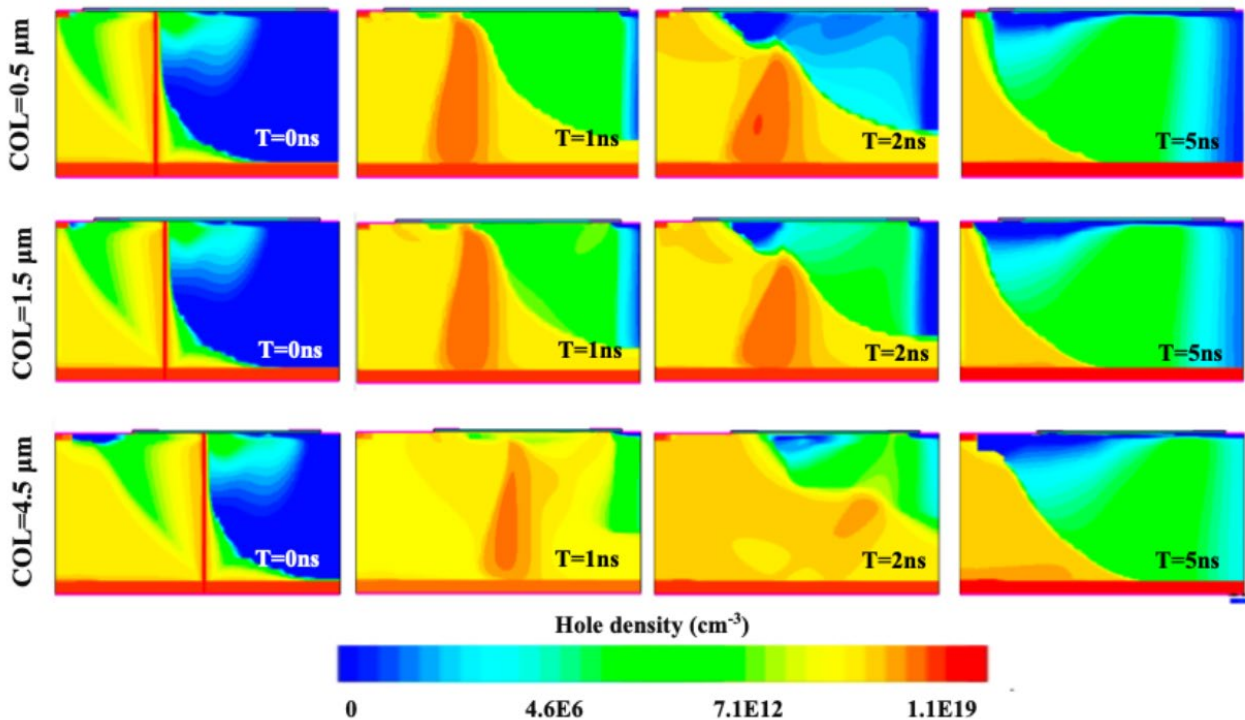


Fig. 13. Hole density distributions of different COL devices at 0ns, 1ns, 2ns and 5ns after an SEE strike.

Summary

The integration of RESURF structures into lateral SiC diodes offers an effective strategy for achieving a well-balanced device performance profile. The combination of TZP and double RESURF structures in lateral SiC diodes enable the simultaneous realization of high breakdown voltage, low specific on-resistance, suppressed leakage current, and improved tolerance to single-event effects (SEE). The addition of P-ring structures plays a critical role in alleviating edge-related electric-field crowding, which not only enhances breakdown robustness but also contributes to faster post-irradiation recovery. Furthermore, this configuration permits the use of higher N-type doping concentrations in the drift region, thereby lowering Ron while maintaining reliable off-state blocking characteristics. Collectively, these design features highlight a robust pathway for developing high-voltage, radiation-hardened SiC power devices. In addition, the incorporation of a P-pillar region facilitates more efficient collection of avalanche-generated charge carriers, which further strengthens the device's resistance to catastrophic failure mechanisms under heavy-ion irradiation.

These findings offer valuable guidelines for the design of next-generation wide-bandgap power devices, particularly for applications in radiation-rich environments such as space electronics. The combination of structural optimization and radiation-hardening design presents a promising pathway for deploying high-performance SiC devices in both terrestrial and extraterrestrial high-voltage systems.

References

- [1] J.-M. Lauenstein, M. C. Casey, R. L. Ladbury, H. S. Kim, A. M. Phan, and A. D. Topper, "Space radiation effects on SiC power device reliability," in *2021 IEEE International Reliability Physics Symposium (IRPS)*, 2021: IEEE, pp. 1-8.
- [2] P. Hazdra, S. Popelka, V. Záhlava, and J. Vobecký, "Radiation damage in 4H-SiC and its effect on power device characteristics," *Solid state phenomena*, vol. 242, pp. 421-426, 2016.
- [3] A. Sengupta *et al.*, "Impact of heavy-ion range on single-event effects in silicon carbide power junction barrier Schottky diodes," *IEEE Transactions on Nuclear Science*, vol. 70, no. 4, pp. 394-400, 2023.
- [4] A. Sengupta *et al.*, "Single-Event Effects in Heavy-Ion Irradiated 3-kV SiC Charge-Balanced Power Devices," *IEEE Transactions on Nuclear Science*, vol. 71, no. 8, pp. 1447-1454, 2024, doi: 10.1109/TNS.2024.3381964.
- [5] C. Martinella *et al.*, "Heavy-ion induced single event effects and latent damages in SiC power MOSFETs," *Microelectronics Reliability*, vol. 128, p. 114423, 2022.
- [6] A. Akturk, J. McGarrity, S. Potbhare, and N. Goldsman, "Radiation effects in commercial 1200 V 24 A silicon carbide power MOSFETs," *IEEE Transactions on Nuclear Science*, vol. 59, no. 6, pp. 3258-3264, 2013.
- [7] C. Martinella *et al.*, "Heavy-ion effects in SiC power MOSFETs with trench-gate design," *IEEE Transactions on Nuclear Science*, vol. 71, no. 8, pp. 1440-1446, 2024.
- [8] M. Imam, M. Quddus, J. Adams, and Z. Hossain, "Efficacy of charge sharing in reshaping the surface electric field in high-voltage lateral RESURF devices," *IEEE Transactions on Electron Devices*, vol. 51, no. 1, pp. 141-148, 2004.
- [9] I. o. Electrical and E. Engineers, *2022 IEEE 9th Workshop on Wide Bandgap Power Devices & Applications (WiPDA)*. IEEE, 2022.
- [10] J. Matsuda, "High reliability and low switching loss dual RESURF 40 V N-LDMOS transistor with grounded multi-step field plate," *Journal of Technology and Social Science*, vol. 7, no. 1, pp. 1-12, 2023.
- [11] Y. Qi, P. M. Gammon, A. B. Renz, V. Kotagama, G. W. C. Baker, and M. Antoniou, "Lateral 1200V SiC schottky barrier diode with single event burnout tolerance," *Power Electronic Devices and Components*, vol. 8, p. 100068, 2024.