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Study of Interface Traps and Scattering Mechanisms in the 4H-SiC MOS Channel Using Gated Hall Measurements

Suman Das[1,a], Daniel J. Lichtenwalner[1,b*], Shane R. Stein[1,c] and Sei-Hyung Ryu[1,d]

[1]Wolfspeed, Inc., 4600 Silicon Drive, Durham, NC 27703, USA

[a]suman.das@wolfspeed.com, [b*]daniel.lichtenwalner@wolfspeed.com, [c]shane.stein@wolfspeed.com, [d]sei-hyung.ryu@wolfspeed.com

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Abstract. Gated Hall measurements of lateral MOSFET devices can be used to directly measure the inversion layer free carrier density and carrier Hall mobility. From this measurement the total number of charged interface traps (N_{IT}) can be extracted. This provides useful insight into the degree of Coulomb scattering expected. By obtaining gated Hall data from 4° off-axis Si-face (0001) 4H-SiC MOSFETs with varied p-well doping levels, mobility limiting components can also be estimated. For these samples it is observed that interface trapped charge is almost half of the total inversion charge, and thus Coulomb scattering dominates at low Vgs or low transverse (or normal) effective field; while phonon scattering may dominate at moderate effective field, and surface roughness only limits mobility at gate fields higher than the rated usage, or at doping levels much higher than 2×10^{18} cm^{-3}.

Introduction

Although the oxide reliability and threshold stability of Si-face (0001) 4H-SiC MOSFETs is relatively good using the established thermal oxidation and NO anneal process [1], it is known that improvements in channel mobility are possible [2], and better measurements of channel properties can be helpful to fully understand the limits of performance. Gated Hall measurements have been found to be a useful way to extract not only carrier mobility (Hall mobility), but also the free carrier density (carriers/cm^2) and total trapped charge (N_{IT}) [3-7]. When performing gated Hall measurements on samples with varied p-well doping levels, the mobility limiting components can more accurately be extracted. This enables a more complete understanding of the interface properties, regarding the limiting factors controlling the inversion-layer channel mobility.

Experimental

Figure 1(a) shows a top view and Fig. 1(b) shows a schematic cross-section of the fabricated MOS gated Hall bar. The Hall bar is fabricated on a Si-face (0001) 4° off-axis 4H-SiC n-type wafer with low doped n-type epilayers, on uniform Al-doped implanted p-well layers (1 um in depth) with doping values of 2×10^{17}, 4×10^{17}, 1×10^{18} and 3×10^{18} cm^{-3}. This is a long channel (L_{ch}=1 mm, W_{ch}=200 um) lateral MOSFET with Hall voltage contacts, designed to minimize errors due to geometric effects [8]. The gate oxide is a typical thermal oxide passivated with a NO anneal. All samples have the same P+ and N+ doped regions, the same activation anneal, and the same gate oxidation process. The only difference between samples is the implanted Al p-well concentrations.

DC Hall measurements are performed at room temperature using a Lakeshore FastHall system with a gate bias option and a 1 Tesla permanent magnet. The Vgs is stepped from the threshold (V_T) value to a Vgs above device use fields to cover a wide range of data for each of the samples measured. As the V_T increases for higher doped samples, a narrower data range is obtained as doping increases. The Vgs has been converted to effective normal field as described by Noguchi [5], using η = 1/3, and a Hall scattering factor of unity used for mobility and free carrier calculations from the Hall data.

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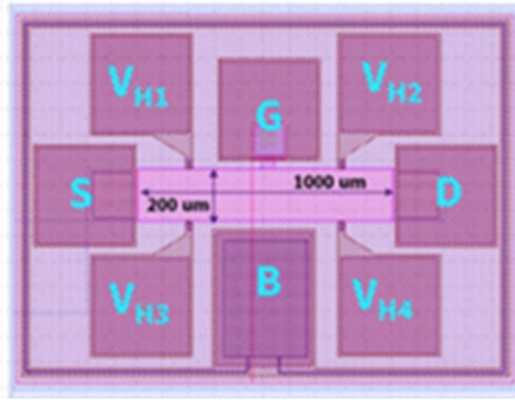

Fig. 1(a). Top-view schematic of a gated Hall MOSFET. L_{chan} = 1 mm, and W_{chan} = 200 um.

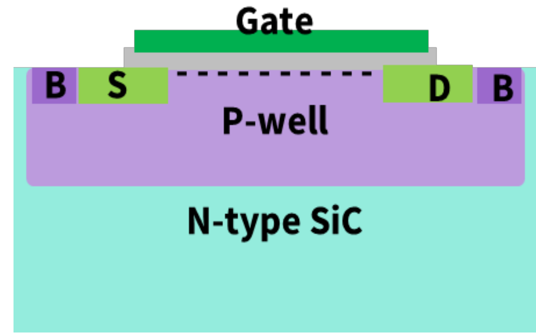

Fig. 1(b). Schematic cross section of a gated Hall MOSFET along the channel length. In gated Hall only inversion charge (dotted line) is measured as a function of Vgs.

Results and Discussion

Figure 2 shows the measured (a) field-effect (μ_{FE}) and (b) Hall mobility (μ_{Hall}) for different p-well doping concentrations at room temperature. The difference between μ_{FE} and μ_{Hall} occurs due to the high density of interface traps, and the assumption in the field-effect calculation that the carrier concentration is determined only by oxide thickness and dielectric constant (disregarding trapped charge). Gated Hall allows the free charge (Ns or n_{free}, cm^{-2}) to be measured as a function of Vgs. The interface trapped charge (N_{IT} or n_{trap}, cm^{-2}) is then determined by subtracting the measured free charge from the total inversion charge. The total charge at the interface is obtained using a split C-V measurement between G to S-D keeping the B contact grounded. A typical split C-V measurement at 5kHz is shown in Fig. 3, from which integration shows the total channel charge on the right y-axis (after subtracting gate to N+ overlap capacitance). The total charge density (n_{total}) measured is consistent with the value calculated from the measured T_{ox} and C_{ox}. The occupied trapped charge density (n_{trap}) for all samples is plotted in Fig. 4, obtained from the gated Hall measured value of n_{free} (data points) subtracted from the measured total charge (n_{total}). In order to show the data together more clearly, the Vgs is scaled by the V_T. It appears that a slight increase in n_{trap} is observed as doping increases. This could be a result of the fermi level change with doping, resulting in more filled traps at a given Vgs - V_T. Of note is that the charged interface trap density is similar to that of the free carriers, and even up to the rated Vgs use conditions nearly half of all inversion layer carriers are trapped.

To observe the overall effect of all scattering mechanisms at the channel, the Hall mobility can be modeled from the individual mobility limiting components, namely the bulk mobility limiting factors (μ_{Bulk}), Coulomb limited mobility (μ_C), surface phonon limited mobility (μ_{Ph}), and surface roughness limited mobility (μ_{SR}). The Coulomb limited mobility can then be calculated from the measured Hall mobility using Mattheissen's rule:

$$\frac{1}{\mu_C} = \frac{1}{\mu_{Hall}} - \frac{1}{\mu_{Bulk}} + \frac{1}{\mu_{Ph}} + \frac{1}{\mu_{SR}} \quad (1)$$

The field (E_{eff}) dependence of μ_{Ph} and μ_{SR} are taken from previous observations in literature [3,5,9,10]. Values for the bulk mobility are chosen based on the doping levels, and the surface phonon limiting term is taken as being close to that of other reports [4,5] using the ideal exponent ($E_{eff}^{-0.33}$). The surface roughness limiting term was chosen such that it corresponds closely to the ideal functional form (E_{eff}^{-2}). All prefactors are adjusted such that the data for all doping levels is fit well, and the extracted coulomb scattering term follows a power law relationship to Ns or n_{free} [5].

In Fig. 5 the Hall mobility versus effective normal field (E_{eff}) is plotted for the sample with 2×10^{17}cm^{-3} p-well doping. The red dotted line is the fit to the data considering all the scattering components.

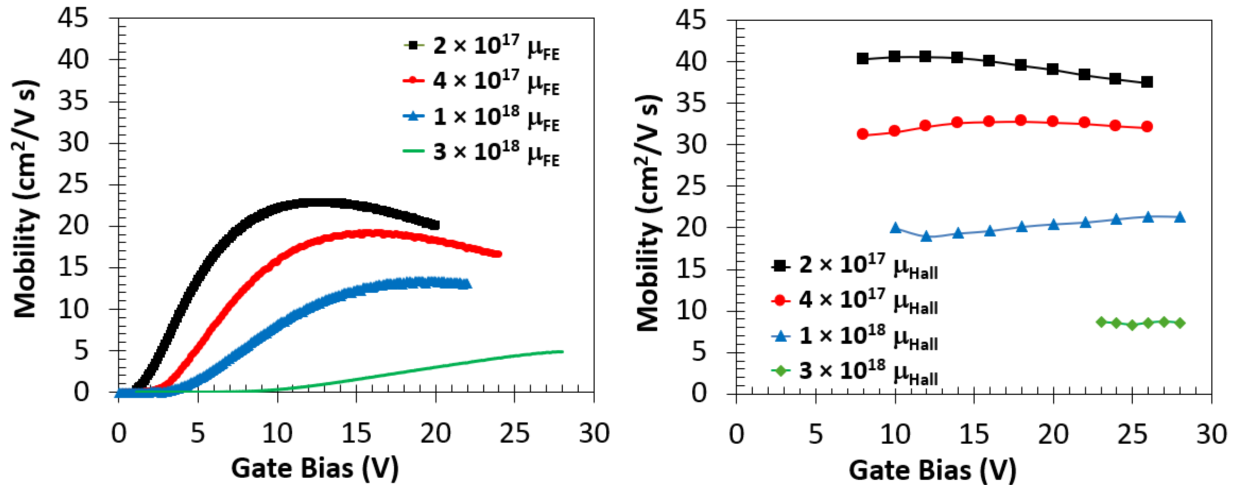

Fig. 2. Comparison of (a) the field-effect mobility measured from Id-Vgs curves, and (b) the Hall mobility. The field-effect mobility will be lower when there is trapped charge, due to the way that the field-effect mobility is calculated.

The Coulomb limiting values have been extracted as discussed above, shown by green dots and fit empirically using a logarithmic function of E_{eff} (maintaining a power law function of Ns). The data can be fit nicely using almost the same surface phonon scattering term as used by others [4,5], with a slightly lessened effect of surface roughness, which is process-dependent. For each sample, the Coulomb scattering term is obtained as described above, and is different for each p-well doping.

Figure 6 shows the effect of these scattering mechanisms on the samples with different doping concentrations. The values of μ_{Ph} and μ_{SR} used are identical for all samples; however, the values of μ_{Bulk} and μ_C change due to doping. We observe that the μ_C drops with increasing p-well concentration. This holds for a fixed temperature; all data shown is at room temperature. The data overall indicates that for these samples, at low Vgs near V_T and above, Coulomb scattering effects limit the channel mobility. This is not surprising due to the high N_{IT} measured directly from these gated Hall devices. At higher Vgs values surface phonon effects dominate for samples with doping $<2\times10^{18}$ cm^{-3}. Only at Vgs or E_{eff} values above typical use values, or for samples with doping much higher than 2×10^{18} cm^{-3}, do surface roughness effects come into play for these samples.

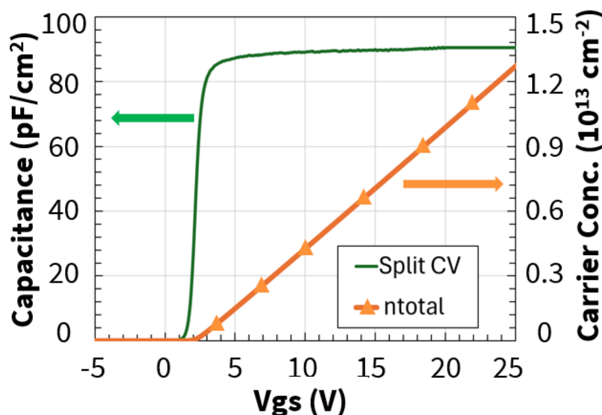

Fig. 3. Split C-V from G to S-D with Base grounded. Frequency is low (5kHz) to measure most of the interface charge.

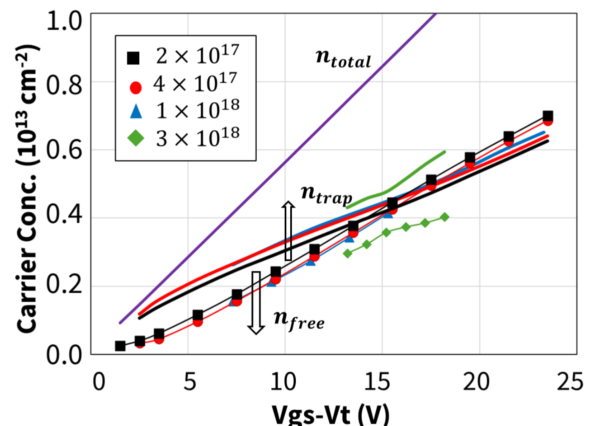

Fig. 4. Calculated trap levels n_{trap} from the measured Hall free carriers and ideal charge n_{total}. Doping has only a small effect on n_{trap} levels.

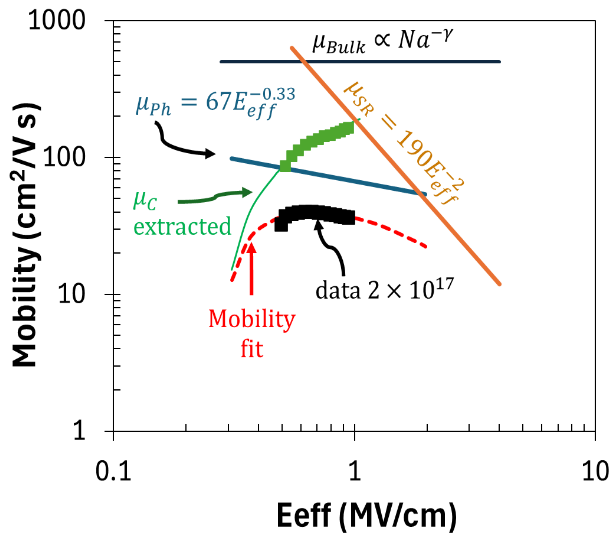

Fig. 5. Graph showing how the Coulomb scattering effects (μ_C) can be obtained from the measured Hall mobility, fixing the terms for bulk, surface phonon, and surface roughness.

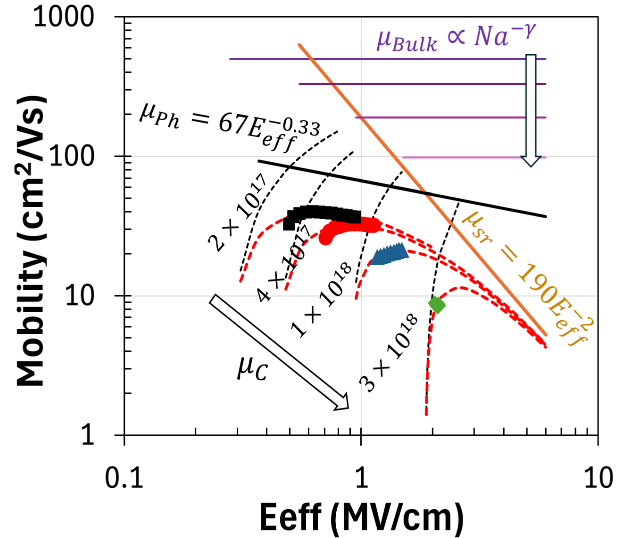

Fig. 6. Graph showing how the mobility limiting terms affect all doping levels, and how the mobility limiting effects are Eeff dependent.

Summary

Gated Hall measurements of Si-face 4H-SiC MOSFETs with NO-annealed thermal gate oxide show clearly that Coulomb and surface phonon effects dominate in limiting the channel mobility at low and medium Vgs or E_{eff} values. Surface roughness effects are minimal in these samples and are only observed to limit the channel mobility at very high Vgs or E_{eff} values, or for samples with doping levels much higher than 2×10^{18} cm^{-3}. The high interface trap density is the main mobility limiting effect (Coulomb effects) that could be improved if the interface passivation were improved or near interface oxide traps were reduced.

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