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Anomalous Reverse Recovery of Body Diode in 4H-SiC Superjunction DMOSFET

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Abstract. We report an anomalous reverse-recovery (RR) of the body diode in a 3.3 kV 4H-SiC superjunction (SJ) DMOSFET: at 77 K, $Q_{RR,sp}$ increases by 1.4×–3.5× versus room temperature and 5× versus 195 K, and J_{PR} increases by >2×, while t_{RR} changes by only <30ns. A clear dependence of $Q_{RR,sp}$ on the ramp rate at 77K indicates the $Q_{RR,sp}$ is not due to additional depletion charge. Current-controlled negative resistance (CCNR) is also observed solely for the SJ body diode at 77K. The voltage waveforms strongly suggest the additional $Q_{RR,sp}$ is due to dynamic breakdown of the SJ due to transient charge imbalance of the pillars caused by delayed hole emissions of the deep acceptors. The anomalous behavior is qualitatively reproduced in simulation. We also benchmark a 3.3kV Charge Balance (CB) 4H-SiC DMOSFET along with the SJ device from 77–423 K using an inductive double-pulse test. For T > 77 K the switching for both devices is dominated by the depletion capacitance (weak $Q_{RR,sp}$ dependence on the ramp rate): the SJ device turns off faster (t_{RR} = 0.3–0.8× CB), is snappier (t_B/t_A = 0.23–0.56× CB), and shows larger J_{PR} (1.8–2.8× CB) while recovering less charge ($Q_{RR,sp}$ = 0.4–0.8× CB). The CB device shows the expected increase of $Q_{RR,sp}$ with temperature and only modest t_{RR} temperature variation. Overall, the CB device provides softer, predictable RR without a cryogenic anomaly, whereas SJ delivers the shortest t_{RR} above 77 K but exhibits the 77 K anomalous increase and is consistently snappier.

Introduction

The 4H-SiC power DMOSFET has emerged as a competitive alternative to Si equivalents due to the wide bandgap of 4H-SiC enabling thinner drift regions and higher doping for the same breakdown voltage, leading to a dramatic reduction in $R_{ON,sp}$. While a wide bandgap enables the large critical electric field that makes 4H-SiC competitive for unipolar devices, it also leads to a higher on-state voltage for bipolar devices, including the 4H-SiC DMOSFET integral body diode. Additionally, the 4H-SiC DMOSFET body diode exhibits certain undesirable switching characteristics. While demonstrating a much-faster reverse recovery (RR) than Si body diodes, they tend to exhibit increased snappiness which can lead to large voltage overshoots and increased power loss [1]. Thus, the anti-parallel body diode inherently present in all DMOSFETs is often shorted by a Schottky diode in switching applications of the 4H-SiC DMOSFET, increasing costs.

Charge balance (CB) and superjunction (SJ) drift layers improve the on-state performance of the 4H-SiC DMOSFET by improving the trade-off between BV and $R_{ON,sp}$ [2,3]. However, the improved on-state performance enabled by the CB and SJ drift-layer can be counteracted by degraded RR performance, as observed in the Si SJ integral diode, where excessive oscillations are caused by rapid changes of the SJ capacitance with voltage [4]. Knowledge of the RR characteristics is therefore required in order to evaluate the trade-offs of different power MOSFETs in circuit applications.

This study evaluates and compares the RR performance of the body diodes of GE (General Electric) 3.3kV 4H-SiC CB and SJ DMOSFETS, from liquid nitrogen temperatures up to 423K. The static performance of the DMOSFETs have previously been characterized in [5]. An anomalous RR is consistently observed for the SJ DMOSFET at 77K. A mechanism for the observed anomalous RR is hypothesized and simulated.

Methodology

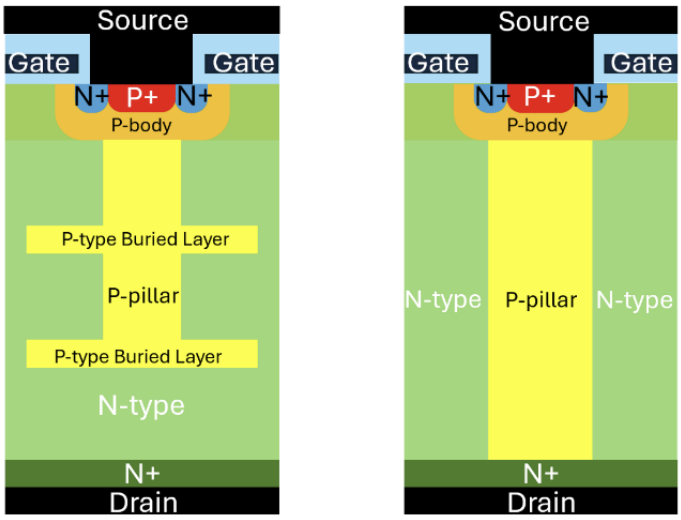


Fig. 1. Full-Cell Cross-Section of CB and SJ Vertical DMOSFETs

Devices and structures. Inductive RR measurements are performed on GE 3.3 kV 4H-SiC charge-balance (CB) and superjunction (SJ) DMOSFETs packaged in TO-247. Full-cell cross-sections for the conventional (Conv), CB, and SJ vertical DMOSFETs are shown in Figure 1. The CB architecture is implemented through intermittent shallow Al implants interleaved with the growth of a 12 µm n-type epitaxial layer (1×10^{16}cm^{-3}) to form buried charge-balance regions that act as electric-field dividers, enabling higher drift-layer doping at a fixed breakdown voltage. Intermittent vertical P-type "bus" pillars (12 µm depth) are realized via high-energy Al implantation (> 20 MeV) to tie the buried CB layers to the P$^+$ source/anode for hole supply. The SJ device employs alternating vertical P- and N-type pillars (5 µm pillar width) formed with the same high-energy implantation approach; pillar dopings are 1×10^{16}cm^{-3}. Both CB and SJ stacks are scalable to higher voltage ratings. For the 3.3 kV DMOSFETs studied here, the drift region thickness is 24 µm.

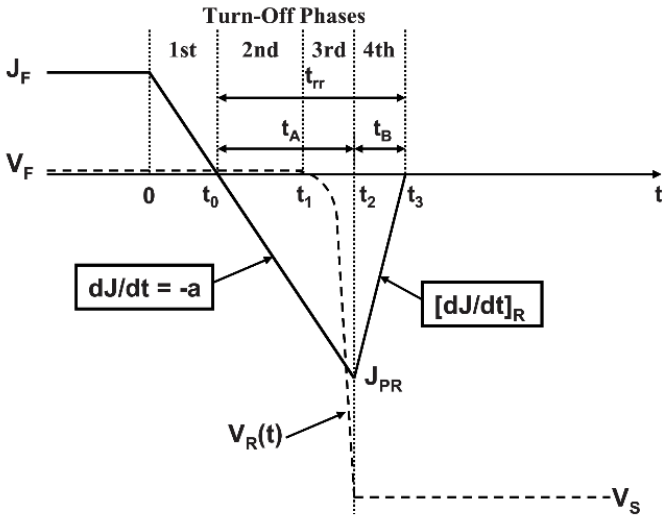
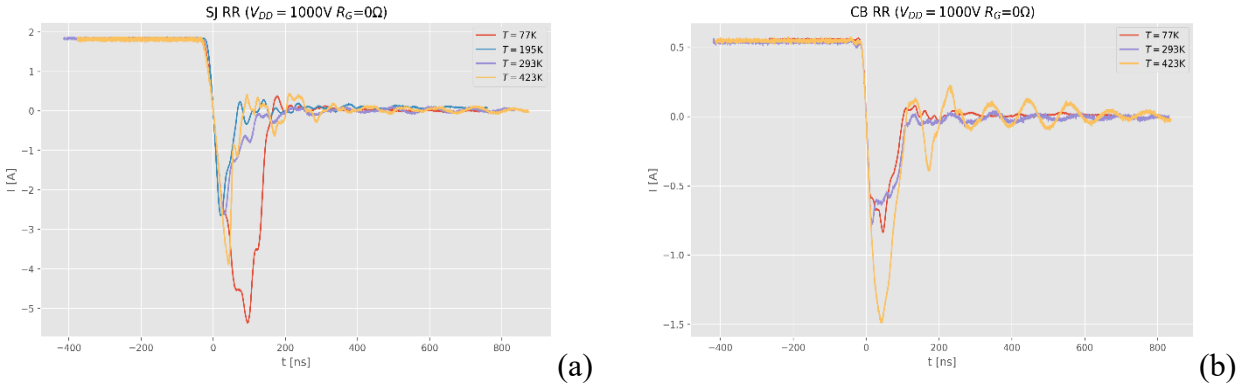


Fig. 2. Schematic reverse recovery switching waveforms and the associated performance parameters [6]

Temperature control. Cryogenic data are taken in liquid nitrogen (77 K) and in a dry-ice/isopropanol bath (195 K). High-temperature (HT) measurements use a temperature-controlled hot plate at 423 K (150 °C). Devices are soaked at the setpoint prior to testing to ensure thermal equilibrium.

Inductive reverse-recovery setup. RR of the body diode is characterized with a standard inductive double-pulse circuit. An 18mH inductor is used as the load. The gate and source of the 4H-SiC SJ or CB DMOSFET are shorted and the body diode is used as the freewheeling diode. The RR waveform is measured at the start of the second pulse. Duty cycles of <1% are used to minimize device self-heating. Given the differing device areas, a current density (J_F = 50A/cm^2) is targeted. The pulse width is set in order to achieve the target J_F. The ramping rate (di/dt) is varied by varying the external gate resistance between 0Ω, 50Ω, and 100Ω of the bottom transistor. Lead lengths are minimized in order to minimize parasitic inductance. Switching parameters are extracted according to Figure 2.

Experiments and Results



(a) (b)

Fig. 3. Sample RR Current Waveforms for 4H-SiC SJ (a) and CB (b) body diodes.

Switching Characteristics. Excluding the SJ cryogenic anomaly at 77 K, both CB and SJ body diodes exhibit capacitance-dominated reverse recovery over 77K-423K and V_R=0.5-1kV at J_F = 50Acm^{-2}. $Q_{RR,sp}$ has only a weak dependence on dJ/dt (Figure 4a), consistent with conventional 4H-SiC body diodes where an implantation-damage "tail" near the junction limits the lifetime and causes minority carriers to recombine before they can be extracted, leaving the depletion charge extraction to dominate the RR waveform [1,7]. In this regime the 4H-SiC SJ body diode does not exhibit the excessive oscillations reported for the Si SJ body diode [4]. The fast minority carrier recombination in the damage layer of the implanted pillars suppresses the pre-depletion current build-up that produces the oscillations due to a large di/dt once the pillars pinch off. This is clearly seen in Figure 10 as the SJ begins supporting significant voltage only 10-20ns after the current-zero crossing, indicating the current almost immediately consists of extracted depletion charge. Consistent with increasing minority carrier lifetime with temperature, Figure 4b shows that the CB diode demonstrates the expected increasing $Q_{RR,sp}$ with temperature, whereas the temperature trend of the SJ diode remains relatively flat, indicating that the switching remains capacitance dominated even at higher temperatures. A minority carrier charge extraction component begins to be detectable for the CB diode at 423K, as indicated by the slight positive slope of $Q_{RR,sp}$ vs dJ/dt at 423K. Finally, the best snappiness characteristics for both diodes is seen at room temperature (Figure 7).

Comparison. Above 77K, the SJ device generally exhibits faster turn-off, with the SJ exhibiting a t_{RR} 0.3x-0.8x that of the CB (Figure 9). The larger t_{RR} of the CB device is expected due to increased resistance from the P-bus tying the charge sheet layers together introducing a larger RC time constant. As expected, the SJ is consistently snappier than the CB device, with a t_B/t_A of about 0.23x-0.56x that of the CB device. This is expected as the pillars must fully pinch-off before significant voltage can be supported, leading to a large drop in capacitance. The same mechanism drives the larger J_{PR} (1.8x-2.8x) of the SJ devices. Despite the larger J_{PR}, the SJ exhibits a smaller $Q_{RR,sp}$ than the CB, approximately 0.4x-0.8x that of the CB due to the smaller t_{RR}. Interestingly, unlike the SJ, the CB

shows only minimal variation of switching time with temperature. These comparisons hold across the differing dJ/dt values caused by varying the external gate resistance of the bottom MOSFET in the DPT set-up.

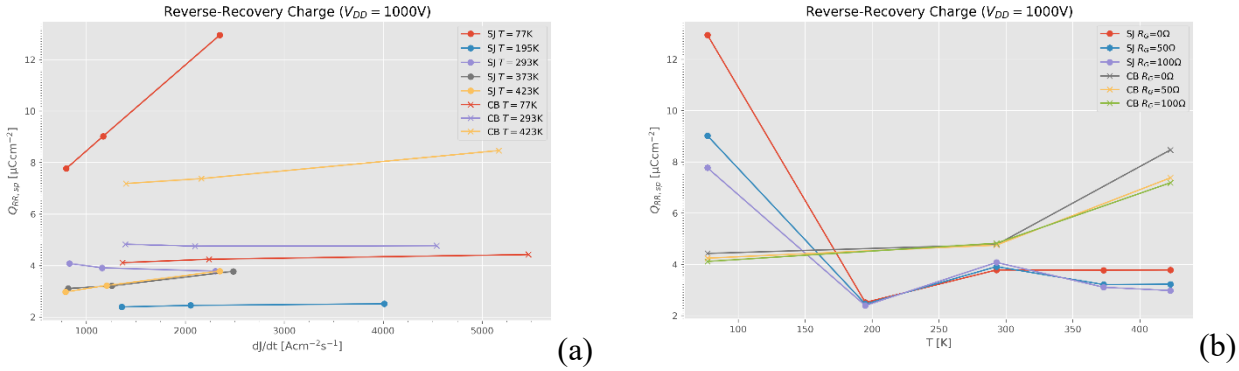


Fig. 4. $Q_{RR,sp}$ dependence on dJ/dt (a) and temperature (b) for 4H-SiC CB and SJ Body Diode

Anomalous Cryogenic RR. At 77K, the SJ body diode exhibits an anomalous increase in $Q_{RR,sp}$ of 3.5x compared to room temperature (RT) and 5x relative 195K. This behavior remains across multiple tested SJ devices. This is the opposite trend than what is expected from the well-documented trend of the minority carrier lifetime increasing with temperature. Thus, $Q_{RR,sp}$ for the SJ becomes 1.9x-3.0x then that of the CB under matched conditions. The RR is no longer junction-capacitance dominated as $Q_{RR,sp}$ has a clear dependence on the ramp rate in Figure 4. A larger slope of $Q_{RR,sp}$ vs reverse voltage at 77K was also observed, indicating additional extracted charge besides the depletion charge. The increased $Q_{RR,sp}$ remains clear even when J_F is reduced to 20A/cm^2. In contrast, the SJ at 195K shows an almost pure junction-capacitance dominated waveform, with $Q_{RR,sp}$ remaining within 1% across the three different ramp rates. In Figure 8, a shallow voltage dip is consistently seen around ~200-300V for the SJ at 77K which is absent in the voltage waveforms taken at other temperatures.

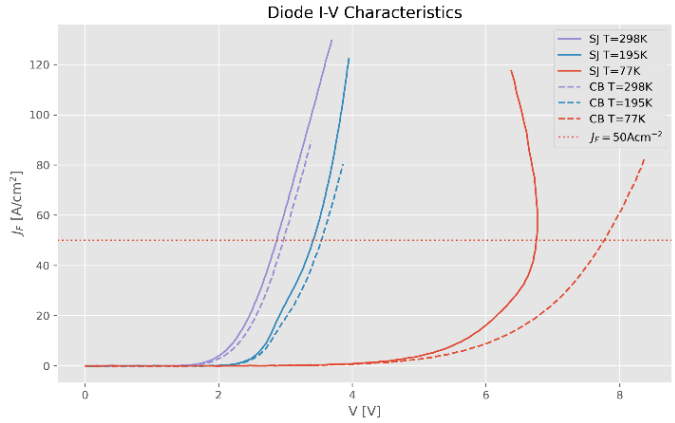


Fig. 5. Static I-V Characteristics for the 4H-SiC CB and SJ Body Diodes at various temperatures.

CCNR Behavior in SJ. In the process of investigating the origin of the anomalous RR behavior of the SJ diode at 77K, static I-V characterization was performed and are shown in Figure 5. A short pulse width (80μs, for a duty cycle of 1.9%) was used to minimize device self-heating. The turn-on knee increases at lower temperatures due to an increase in the junction barrier height as the Fermi level moves towards the band edges. Decreased acceptor ionization also induces a large series resistance in the diode. CCNR behavior is observed solely for the SJ device triggered at J_F=50Acm^{-2}. The current decay tail at the end of the second pulse is investigated to determine the operating point of the SJ device during switching and is shown in Figure 6a. No CCNR behavior is observed in the transient I-V of the SJ diode.

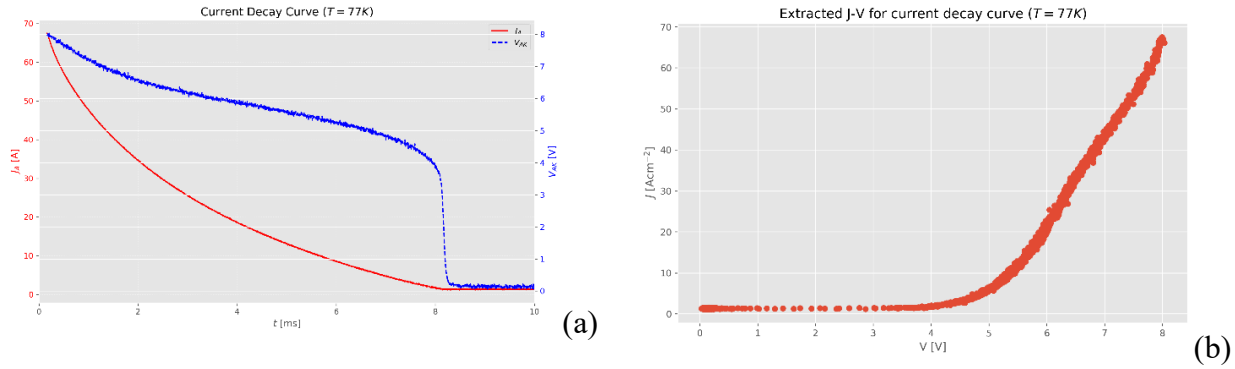


Fig. 6. (a) The current decay curve through the 4H-SiC SJ body diode at the end of the second pulse (b) Extracted J-V characteristics from the current decay pulse.

Analysis and Discussion

Switching Characteristics. The CB body diode addresses several shortcomings of the conventional 4H-SiC DMOSFET body diode while preserving the core advantage over Si. Turn-off remains capacitance-dominated and fast across the tested conditions (t_{RR} = ~100–350 ns), yet the recovery is markedly softer: at room temperature t_B/t_A can exceed 10 and, aside from 77 K, was greater than 1.4 in 9/9 RT scenarios tested and in 8/9 HT scenarios tested. The softer recovery reduces voltage overshoot and loss without sacrificing speed. Coupled with the CB drift region's improved $R_{ON,sp}$-BV trade-off, this yields a device that combines better on-state performance with more benign reverse recovery, diminishing the need to short the CB body diode with a Schottky diode. Outside 77 K, the SJ body diode retains the same advantages of the conventional 4H-SiC body diode over Si diodes (fast turn-off and comparatively low J_{PR} due to the capacitance-dominated switching) while still retaining the principal drawback of increased snappiness (t_B/t_A > 1.4 in only 9/15 RT scenarios tested and in 0/15 HT scenarios tested). This snappiness limitation, however, is intrinsic to the SJ structure as it is due to the requirement of pillar pinch-off prior to significant voltage being supported. However, the 4H-SiC SJ does not suffer from excessive oscillations typical of Si SJ structures because the switching is depletion-capacitance dominated.

Comparison. The results favor the CB body diode for RR performance as it preserves fast, capacitance-dominated switching while remaining substantially less snappy than the SJ due to the lack of the pillar pinch-off constraint. It has a predictable temperature dependence, with $Q_{RR,sp}$ increasing with temperature from 77K-423K, and almost no variation in switching time with temperature at matching conditions.

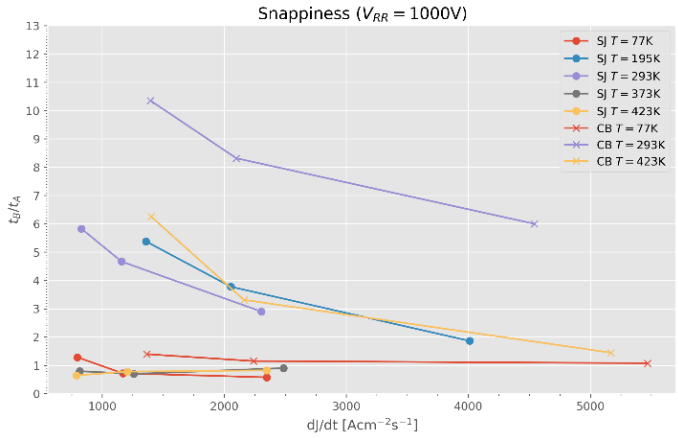


Fig. 7. Dependence of snappiness on dJ/dt at various temperatures for the 4H-SiC CB and SJ Body Diodes.

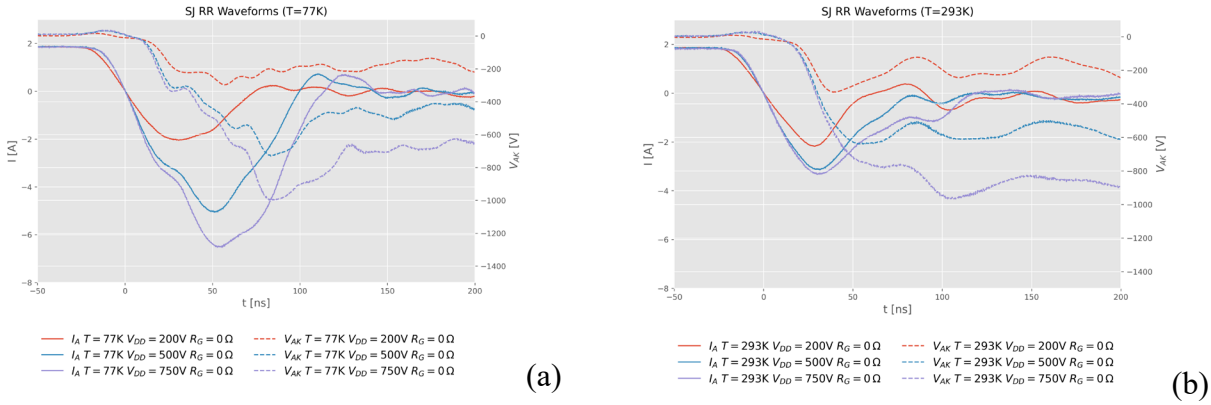


Fig. 8. Voltage waveforms during RR for 4H-SiC SJ Body Diode.

Anomalous Cryogenic RR. There are two possible sources for the additional $Q_{RR,sp}$ observed in the SJ RR at 77K. The additional extracted charge is either present *before* the RR is initiated (in the on-state) or is generated *during* the RR. The expected trend of decreasing lifetime with decreasing temperature predicts a reduction in stored minority carriers in the on-state (before initiation of RR) at 77K compared to RT. The voltage zero-crossing temperature dependence (Figure 10) rules out a large increase in the stored minority carrier charge in the on-state, as such an increase would also increase t_I compared to RT. The measured decrease in t_I at 77K compared to RT correlates with an expected lower lifetime at 77K. Observing Figure 8, a consistent negative differential resistance (NDR) is observed around $-V_{AK}$ =200V-300V. NDR during RR has been previously observed in [8] and was attributed to dynamic breakdown. The breakdown voltage of the SJ rapidly decreases with the degree of charge imbalance [9]. While in [8], dynamic breakdown was caused by large transient current densities significantly modifying the background doping, the current densities in this case cause only a <0.01% modification in pillar doping. Rather, [9] reveals a plausible mechanism. For the SJ to support voltage, both the p-pillar and the n-pillar need to deplete. Depletion of the p-pillar is driven by hole emission of the acceptors. Due to the deepness of the Al acceptor level in 4H-SiC, the hole emission time at 77K can exceed the switching time scale. For optimally designed SJ pillars, the lateral electric field at pillar pinch-off (when significant voltage begins to be supported) is equal to the critical electric field. If the p-pillars remain undepleted due to the large hole emission time at 77K, the local electric field can exceed the critical field, causing avalanching. Since the avalanching happens at a high-voltage and large current, it is accompanied with significant local self-heating. The local self-heating decreases the hole emission time and locally depletes the p-pillar, compensating the n-pillar and reducing the electric field below the critical field. The large local electric field also decreases hole emission time through the Poole-Frenkel effect. Thus, destructive breakdown is avoided through negative feedback as the large electric fields leading to avalanching also create the condition to deplete the p-pillar and reduce the local electric field by compensating the donors in the n-pillar.

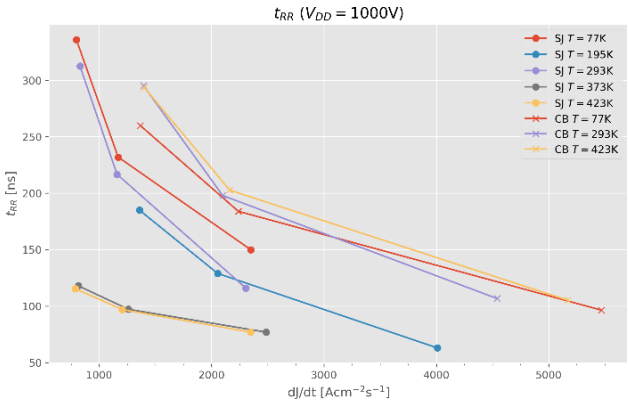


Fig. 9. Dependence of the reverse recovery time (t_{RR}) on dJ/dt at various temperatures for the 4H-SiC CB and SJ body diode.

Simulations. We investigate our hypothesis by performing RR simulations of the 4H-SiC SJ DMOSFET using TCAD Sentaurus. Figure 11a shows the RR simulation of the SJ at 300K as a baseline. In Figure 11b, a large (>100x) increase is seen in I_{PR} when modeling the acceptors as traps located 0.2eV above the valence band with $\sigma_n = \sigma_p = 1E\text{-}15cm^{-2}$ and using the default Sentaurus Poole-Frenkel model. Figure 11c reproduces the NDR characteristic seen in the SJ RR at 77K, but the diode is no longer capable of turning off. When self-heating effects are also included (Figure 12), all observed characteristics are reproduced: (1) a large increase in $Q_{RR,sp}$ compared to room temperature, and (2) an NDR dip during the RR. The simulations are only a qualitative reproduction, as I_{RP} exceeds 100A in the simulation. However, doping significantly reduces the thermal conductivity of 4H-SiC [10], especially at low temperature where the undoped thermal conductivity reaches a peak, and this effect was not modeled. A reduced thermal conductivity enhances self-heating and reduces the switching time and I_{RP} of the simulated SJ body diode.

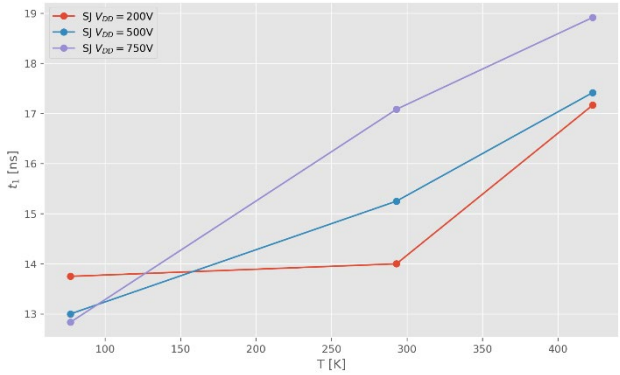
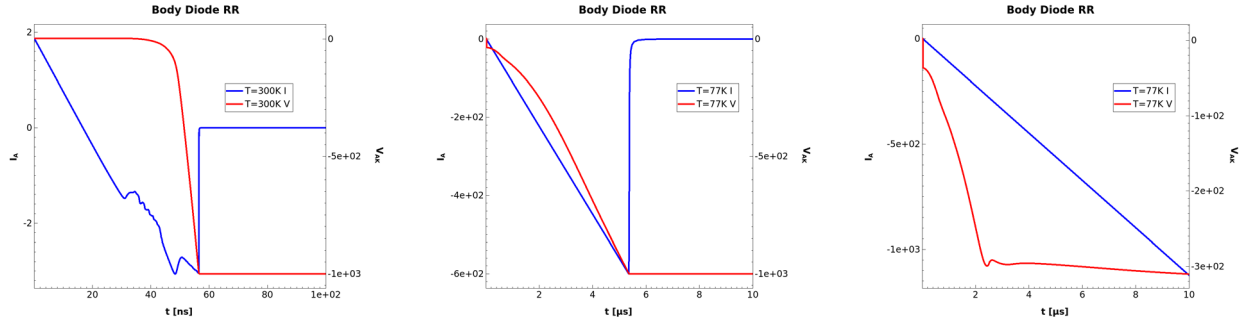
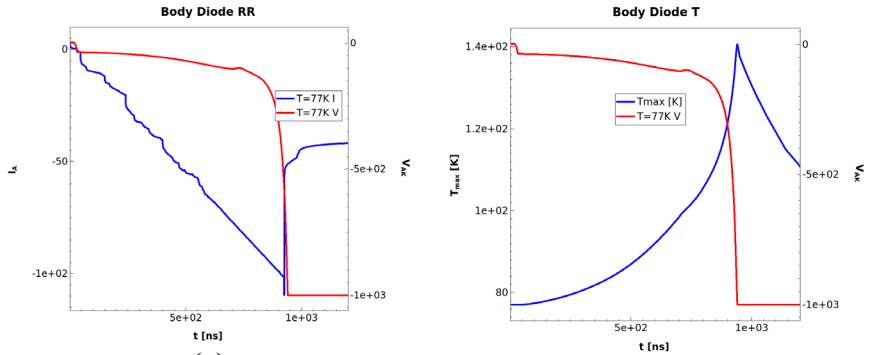


Fig. 10. Temperature Dependence of the voltage zero-crossing time (t_1) at various reverse voltages.



(a) (b) (c)

Fig. 11. Simulated RR of 4H-SiC SJ Body Diode. (a) 300K RR (b) 77K RR, including temperature and electric-field hole emission time of acceptors (c) Same as (b), but including avalanche generation.



(a) (b)

Fig. 12. Simulated RR characteristics of 4H-SiC SJ Body Diode including self-heating effects and electric-field and temperature-dependent hole emission time for acceptors. (a) RR waveform, (b) Maximum temperature inside device during RR.

Conclusion

RR is characterized for 3.3 kV 4H-SiC SJ charge-balance CB DMOSFET body diodes from 77–423 K using an inductive double-pulse. For T > 77 K, both are capacitance-dominated: SJ turns off faster (t_{RR} = 0.3–0.8× CB), is snappier (t_B/t_A = 0.23–0.56× CB), and shows larger J_{PR} (1.8–2.8× CB) while recovering less charge ($Q_{RR,sp}$ = 0.4–0.8× CB). CB remains fast (tRR ≈ 100–350 ns), has softer recovery (t_B/t_A > 1.4 in essentially all non-cryogenic cases), and follows a predictable temperature trend ($Q_{RR,sp}$ increases with T with modest t_{RR} variation). At 77 K the SJ shows an anomalous RR: $Q_{RR,sp}$ increases by 1.4×–3.5× vs room temperature and 5× vs 19 K, J_{PR} increases by >2×, and t_{RR} changes by <30 ns; $Q_{RR,sp}$ also regains sensitivity to ramp rate and VR and persists at J_F = 20 A/cm^2 (vanishing by 7.5 A/cm^2). Static I-V shows current-controlled negative resistance (CCNR) only for the SJ at 77 K, but transient decay during RR does not; we therefore have no evidence that CCNR directly causes the anomalous $Q_{RR,sp}$. TCAD including deep-acceptor emission and field/temperature-assisted effects qualitatively reproduces the cryogenic trends. Overall, CB is the safer default across temperature (fast, soft, predictable; no cryogenic anomaly), while SJ offers the shortest t_{RR} above 77K at the cost of higher snappiness and a 77K charge increase.

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