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Dynamic Conduction Behavior of SiC-MOSFETs in the Sub-Threshold Regime and the Impact of Deep Oxide Traps to the Channel Depletion

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Abstract. This paper investigates the dynamic conduction behavior of silicon carbide (SiC) MOSFETs in the sub-threshold regime. We demonstrate that controlled gate bias preconditioning, combined with time-resolved electrical measurements in thermal equilibrium, reveals a notable drift in the source-drain voltage V_{sd}. The direction of this drift depends on the polarity of gate preconditioning and is directly related to variations in the channel conduction. These effects are shown to be attributed to charge release from deep oxide traps, leading to a gradual shift in the flat-band voltage (V_{fb}) over time. Experimental results reveal that these dynamic effects are most prominent in the depletion and weak inversion regimes. Our findings highlight the influence of oxide trap dynamics on the body diode forward voltage (V_f) and its significance for the reliability of SiC devices, specifically in its role as the temperature-sensitive parameter.

Introduction

Despite their revolutionary characteristics, SiC MOS-FETs exhibit unique challenges, particularly related to sub-threshold conduction, as well as their correlation to V_f. Previous studies have shown that V_f, as a temperature-sensitive electrical parameter (TSEP), exhibits pronounced time dependence [1, 2] and is further affected by the applied gate bias [3]. This dynamic V_f may lead to inaccuracies in junction temperature estimation, causing over- or under-stress conditions during reliability tests. To illustrate this effect, Fig. 1 shows an example where the cooling curve of the body diode in a discrete SiC-MOSFET was measured at different V_{gs} after being subjected to identical heating conditions through the active channel. The results reveal that the temperature response during cooling significantly differs between measurements, demonstrating that the influence of gate bias cannot be neglected. Huerner et al. [4] investigated the influence of gate voltage on the forward conduction properties of the body diode. The study showed that the current path through the channel remained significant even for gate voltages below the threshold voltage, creating an additional conduction path in parallel to the body diode. Their simulations further demonstrated that once the MOSFET enters depletion, the current through the channel becomes negligible and primarily flows through the body diode. However, the sub-threshold conduction and its correlation to the body-diode characteristics remain largely unexplored.

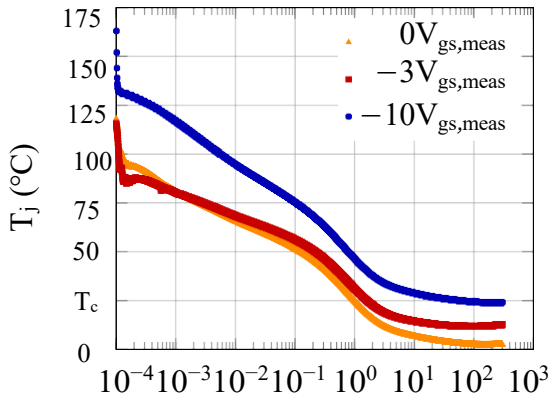

Fig. 1. Junction temperature cooling curve at different V_{gs} for a chiller temperature of T_c=25°C

Experimental Setup and Findings

To systematically analyze the dynamic conduction behavior, a Keysight B1505 parameter analyzer with the circuit configuration shown in Fig. 2 was used. A set of tests as shown in Tab. 1 was defined for these investigation. In Phase 1 (Pre-Conditioning), the SiC MOSFETs were subjected to controlled gate bias $V_{gs,pre}$, to reach either strong inversion or strong accu-mulation. After Phase 1, the gate bias was switched to different $V_{gs,meas}$ values, each initiating a voltage

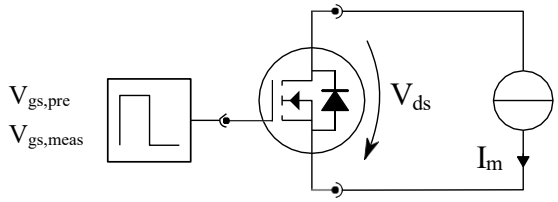

Fig. 2. Measurement circuit for measuring the dynamic conduction behavior

monitoring phase (Phase 2). During this phase, a measurement current of 10mA is continuously applied from source to drain to measure V_{sd}. This measurement current was chosen sufficiently small to make self-heating negligible. Multiple products from different manufacturers and different design technologies, including planar MOSFETs, trench MOSFETs with PN junctions, and planar MOSFETs incorporating embedded Schottky junctions (MPS), were used for these investigations. For represen-tation comparison, two device types —a planar MOSFET with a PN junction and a planar MOSFET with an MPS structure— were selected.

Table 1. Test Plan for measuring the dynamic conduction behavior

Phase 1: Pre-Conditioning			**Phase 2: Voltage-Monitoring**		**Measurement Current**
mode	$V_{gs,pre}$	time	$V_{gs,meas}$	time	I_m
strong Inversion	+15 V	60 s	−10 V . . . + 10 V	1000 s	10 mA
strong Accumulation	-15 V	60 s	−10 V . . . + 10 V	1000 s	10 mA

Fig. 3a shows the response measured at $V_{gs,meas}$ = −3 V for the two preconditioning modes outlined in Tab. 1. These graphs reveal several key observations: First, V_{sd} is clearly time-dependent, with the largest shift in ΔV_{sd} occurring at the transition from Phase 1 to Phase 2. Then the signal gradually converges to a steady-state value, exhibiting time constants of up to $\tau \approx 160s$.

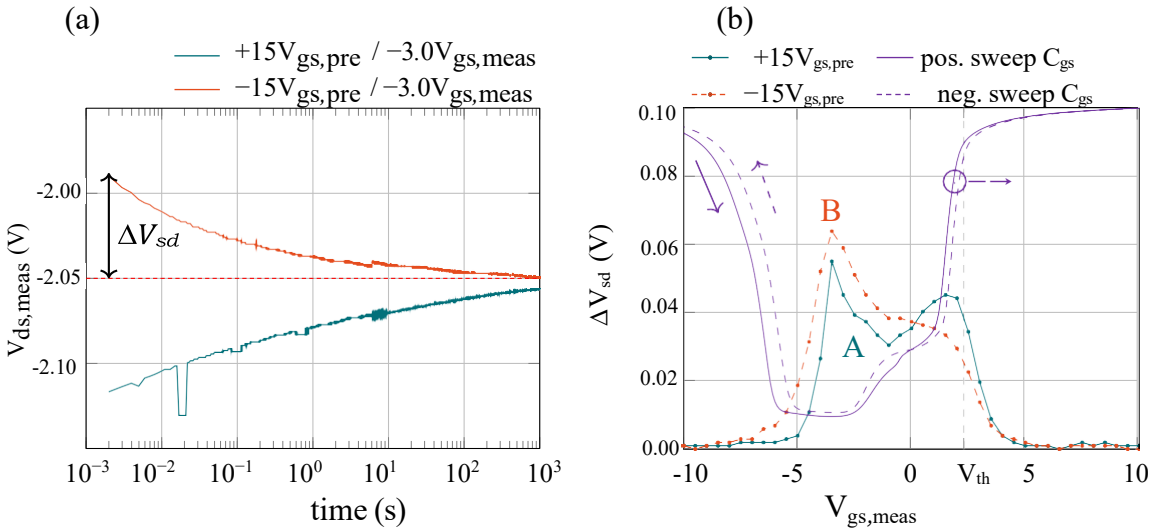

Fig. 3. (a) Dynamic reverse-conduction response after different gate-preconditioning voltages at −3 $V_{gs,meas}$ (b) ΔV_{sd} after different gate preconditioning at various gate voltages.

Interestingly, the preconditioning bias defines the drift direction, which exhibits an inverse settling behavior. However, the conduction levels ultimately converge to a common steady-state value, independent of the initial conditions. Comparing ΔV_{sd} with C_{gs} within the defined $V_{gs,meas}$ range from the Tab. 1 reveal a direct correlation to the channel conduction regimes, as shown in Fig. 3b. The dynamic effects are most pronounced during channel depletion and weak inversion, while they are considerably less significant under strong inversion and accumulation, as indicated by the C_{gs} curves. Furthermore, the direction of the voltage sweep in the capacitance measurement introduces a hystere-sis effect. Similarly, another hysteresis is evident in the ΔV_{sd} measurements, depending on the applied preconditioning. The amplitude of ΔV_{sd} is lower when the device is preconditioned in inversion com-pared to preconditioning in accumulation.

These findings indicate that the underlying mechanism in the dynamic V_{sd} cannot be explained solely by the body diode and is somehow linked to the MOS capacitor behavior. Therefore, mechanisms like self-heating and deep-level bulk crystal defects, can be excluded based on our measurements. Thus the behavior is related to an additional current path through the channel [4].

Flat-band voltage V_{sd} Shift

Fig. 4 illustrates a simplified representation model of the parallel conduction paths through the body diode and the channel. In this configuration, the channel conduc-tion is determined by the charges controlled through the MOS-capacitor and its electrostatics. Therefore, the flat-band voltage (V_{fb}) at the SiC/SiO_2 interface must now be taken into account. Eq. (1) defines the relation between V_{fb} and the built-in potential (V_{bi}) as a function of the metal/polysilicon work function (Φ_m), the semiconductor work function (Φ_s), and the trapped charges within the oxide ($-Q_{ox,t}/C_{ox}$). Any shift in V_{fb} directly influences the threshold voltage and, consequently, the degree of channel conduction.

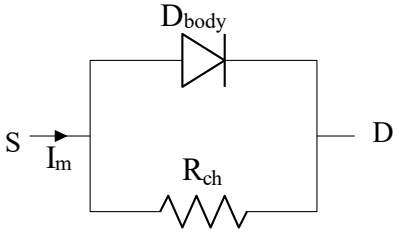

Fig. 4. Simplified representation model

$$V_{fb} = -V_{bi} = \Phi_m - \Phi_s - \frac{Q_{ox,t}}{C_{ox}} \quad (1)$$

According to Kang et al.[5] the trap charge related flat-band voltage shift can be expressed as ΔV_{fb} by Eq. (2).

$$\Delta V_{fb} = -\frac{Q_{ox,t}}{C_{ox}} = -\frac{1}{C_{ox}}\int_0^{tox}\frac{x}{t_{tox}}\rho(x)dx \longrightarrow \Delta V_{fb}(t) \propto \frac{Q(0)}{C_{ox}}e^{\frac{-t}{\tau}} \quad (2)$$

Based on this relation, the shift in ΔV_{fb} settles exponentially. This shift induces a corresponding variation in threshold voltage (ΔV_{th}), which reflects a change in channel resistance (ΔR_{ch}), and thus influences the source–drain voltage (ΔV_{sd}). To quantify the average variation of V_{fb} as a function of ΔV_{sd}, Figure 5 compares V_{sd} at t = 0 s and t = 6 s for various gate–source voltages (V_{gs}). For simplicity, it is assumed that V_{sd} has reached steady state after 6 s, such that the vertical difference at a given V_{gs} corresponds to ΔV_{sd}.

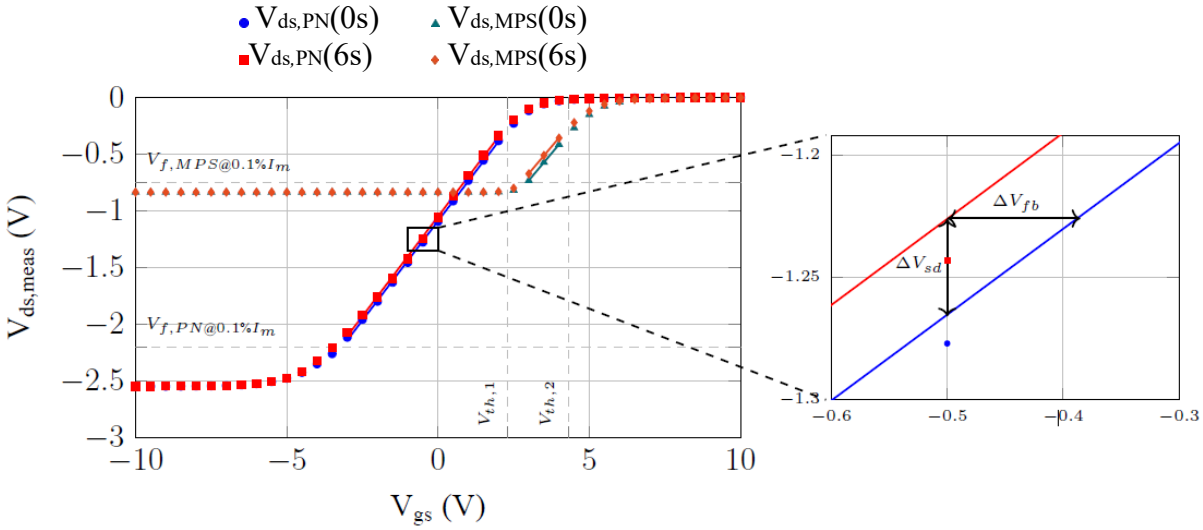

Fig. 5. Sub-threshold behavior at the beginning and end of the $V_{ds}(V_{gs})$ measurement at I_m = 10mA. It shows rendering trap dynamics due to V_{th} and PN-conduction properties. Zoom shows the average sub-threshold shift due to hole release and the resulting V_{fb} shift.

At the same time, at a fixed V_{sd}, the horizontal gap represents a ΔV_{gs}. This ΔV_{gs} shift is time-dependent and reflects the dynamics of the MOS capacitor, which are governed by trap dynamics expressed as ΔV_{fb}. The magnitude of the shift allows for an estimation of the amount of trap charges participating in the dynamic response, providing a visual representation of Eq. (2). Furthermore, the slope of the curves provides insight into sensitivity of the channel to charge changes at the gateoxide. This behavior demonstrates the proportional correlation between gate charge and channel conductance in this regime.

Another observation indicates that for gate voltages exceeding the V_{th}, the channel enters strong inversion, thereby reducing the sensitivity of conduction to shifts in V_{fb}. Once V_{sd} reaches the forward voltage of the PN/MPS junction, variations in the flat-band voltage become less pronounced, as the measurement current flows primarily through the body diode. The impedance of the body diode is dominating the depleted channel. This effect may occur even before accumulation of the channel and is particularly pronounced in MOSFETs with an integrated MPS junction.

Trap Dynamics Mechanics

As discussed in the previous section, the observed behavior of V_{sd} is driven by trap dynamics that affect the channel conduction. Kang et al. [5] attributed this trap dynamics to the presence of deep ox-ide traps exhibiting long tunneling time constants. The time constants are governed by the tunneling probability, which is, in turn, strongly dependent on the spatial position of the trap within

the oxide. Traps located deeper in the oxide, i.e., farther from the SiC/SiO_2 interface, exhibit significantly longer time constants than those near the interface, rendering them more difficult to detect during transient or fast measurements. Thicker oxides further exacerbate this effect, as the reduced tunneling probability for deeply embedded trap states results in more pronounced charge release over prolonged times. The following Eq. (3) provides a quantitative description of this phenomenon [6]. Φ_B, $\bar{h}$, E_c, E_t, m_{ox}^* and m_s^* represent the discontinuity between semiconductor and oxide, reduced Planck constant, conduc-tion band edge, trap energy level, effective electron masses in the oxide and in the semiconductor, respectively.

$$\tau(x) = \frac{m_{ox}^{*2} x\left(1+\frac{1}{2\eta 1 x}\right)}{2\pi^2\, \eta 2 \bar{h}^2 D_{it}} e^{2\eta 1 x} \text{ with } \eta_1^2 = \frac{2m_{ox}^*(\Phi_B + E_c - E_t)}{\bar{h}^2}, \eta_2^2 = \frac{2m_s^*(E_c - E_t)}{\bar{h}^2} \quad (3)$$

The analysis of trap dynamics indicates that the observed signal at Fig. 3a cannot be adequately represented by a single time constant. A deconvolution-based approach, applied across the temperature range, did not result in conclusive and reliable estimations of the activation energies associated with the participating trap states. Nevertheless, the extracted mean time constant of $\tau \approx 160$ s suggests that the tunneling probability of deep traps appears to dominate the overall time constant of the observed dynamic effect.

After a positive preconditioning, the oxide gradually releases holes, leading to a decreased channel depletion. Conversely, after a negative preconditioning, negative charges are released, increasing the channel depletion. Fig. 3a illustrates the dynamic reverse conduction behavior response and the presence of both deep positive and negative oxide traps at $-3\ V_{gs,meas}$ for positive (+15 V) and negative (−15 V) preconditioning respectively. The switching trap behavior dependence on the preconditioning voltage shows similar signatures attributed to dipole oxygen vacancies (e.g., $E^t_{\gamma 4}$ centers) [7].

Summary

This work investigates the dynamic conduction of SiC MOSFETs in the sub-threshold regime under conditions of low reverse current and thermal equilibrium. Gate-bias preconditioning is shown to induce inverted drifts in $V_{sd}(t)$, which converge toward a common steady state. The effect is most pronounced during channel depletion and weak inversion, consistent with the observed correlation between $V_{sd}(t)$ and $C_{gs}(V_{GS})$. The behavior is attributed to time-dependent flat-band shifts ($V_{fb}(t)$) arising from trap dynamics in the oxide. A characteristic time constant of $\tau \approx 160$s was extracted, indicating tunneling from traps located deep within the oxide. In regimes of strong inversion or strong depletion, the sensitivity to V_{fb} shifts diminishes, rendering the drift negligible. Alternative explanations such as self-heating or deep bulk crystal defects were systematically excluded. These findings carry practical implications for reliability assessment and for temperature sensing based on the diode forward voltage (V_f) as a TSEP: preconditioning and relaxation times must be carefully controlled or compensated to avoid bias in junction-temperature estimation. Future work will focus on the quantitative extraction of trap energy and depth distributions through extended temperature sweeps and complementary techniques (e.g., charge pumping, DLTS, scanning capacitance), as well as on assessing process and oxide-thickness dependencies to mitigate the observed drift.

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