Key Engineering Materials
ISSN: 1662-9795, Vol. 1057, pp 125-130
doi:10.4028/p-m0gjDq

Submitted: 2025-09-28
Revised: 2025-12-21
Accepted: 2026-02-26
Online: 2026-05-21

Influence of Cell Structure and Topology on C_{oss} of 4H-SiC MOSFET

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Keywords: Cell topology, Split-gate MOSFET, Output capacitance (C_{oss}), Abrupt drop phenomenon, Switching losses

Abstract. This study demonstrates that the output capacitance (C_{oss}) of a 4H-SiC MOSFET is proportional to the length of JFET (L_{JFET}) at a low V_{ds}, since under this condition, the gate-to-drain capacitance (C_{gd}) may account for nearly half of C_{oss}. Furthermore, when V_{ds} is low, the C_{oss} of MOSFETs with square and hexagonal cell topologies is approximately 20% and 25% higher than that of MOSFETs with the strip cell topology, respectively, due to larger JFET areas. However, when V_{ds} is higher, the C_{oss} of MOSFETs with square and hexagonal cell topologies is lower because of the lower drain-to-source capacitance (C_{ds}) resulting from smaller Pwell areas. The split-gate MOSFET can reduce C_{gd}, but the smaller poly-gate area decreases the depletion capability, resulting in a higher C_{ds}. As L_{JFET} of the MOSFET decreases, C_{gd} becomes lower, which may shorten the switching time, but due to the increased area of Pwell (L_{PW}), the reverse recovery current (I_{rr}) increases. This study proposes partially increasing the gate oxide thickness. Although this may slightly increase C_{ds}, the shorter switching time results in a 5% reduction in the turn-on switching loss (E_{on}).

Introduction

C_{oss} has a significant impact on the switching time and reverse recovery characteristics of MOSFETs [1], [2], [3]. C_{oss} consists of C_{gd} and C_{ds}, and C_{ds} consists of the sidewall and bottom capacitances of the Pwell (C_{SW} and C_{BT}) [4], [5], as illustrated in Fig. 1. Therefore, the structure and topology of both the JFET and Pwell significantly influence C_{oss} [6], [7]. However, their correlation and mechanisms have not yet been sufficiently studied. When V_{ds} is low, C_{oss} is dominated by C_{gd} and C_{SW}. At high V_{ds}, the JFET is fully depleted, C_{gd} and C_{SW} is saturated, and C_{oss} is then dominated by C_{BT} [5], [8], [9]. Therefore, the area of the JFET and the sidewall of the P-well affect C_{oss} more significantly at low V_{ds}, whereas the area of the bottom of P-well affects C_{oss} at high V_{ds}. This study investigated the influences of the variation of L_{JFET} and L_{PW}, as well as the split-gate structure on C_{oss}. Accordingly, the C_{oss} of MOSFETs with strip, square, and hexagonal cell topologies was compared. Furthermore, turn-on time (t_{on}), reverse recovery current (I_{rr}), and turn-on energy loss (E_{on}) of the MOSFETs with different L_{JFET} and L_{PW} were obtained by the double pulse test (DPT) in this study.

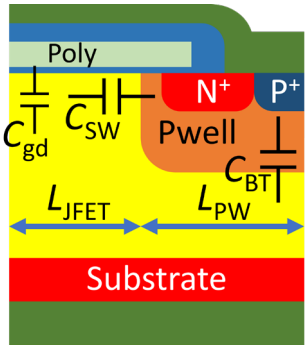

Fig. 1. Schematic and parasitic capacitances of the 4H-SiC MOSFETs in this study.

Experimental

The MOSFETs with strip, square, and hexagonal cell topologies were fabricated in this study, as shown in Fig. 2. The L_{JFET} and L_{PW} of the MOSFETs are listed in Table I. The concentrations of epitaxy and Pwell of the MOSFETs are approximately 8×10^{15} cm^{-3} and 2×10^{18} cm^{-3}, respectively. For comparison, the split-gate MOSFET was also fabricated, with the spacing between adjacent poly gates being 1.0 μm. The forward and reverse I_{ds}-V_{ds} curves and capacitances of MOSFETs were measured by Keysight B1505A, whereas the DPT was simulated using TCAD software, Sentaurus.

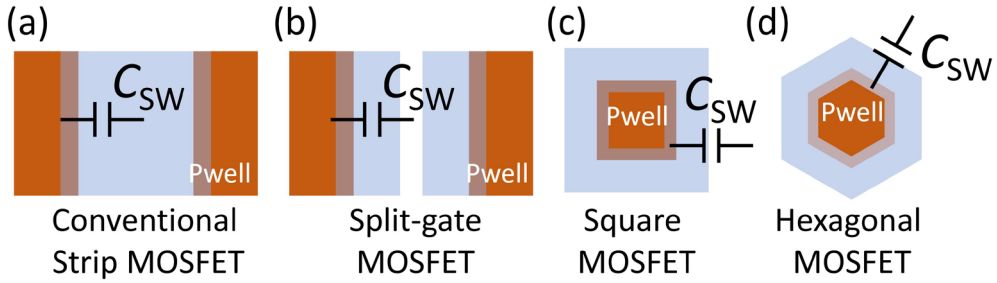

Fig. 2. The capacitances of MOSFETs with different cell structures and topologies. All the MOSFETs were fabricated in this study.

Table I. The structural parameters of MOSFETs fabricated in this study.

Topologies	Strip	Strip	Strip	Strip	Split-gate	Square	Hexagonal
L_{JFET} (μm)	2.4	2.2	2.0	2.2	2.2	2.4	2.4
L_{PW} (μm)	6.5	6.5	6.5	5.0	5.0	6.5	6.5

Results and Discussions

Fig. 3 shows that the on-resistance (R_{on}) of the hexagonal-cell and square-cell MOSFETs is approximately 21 % and 10 % lower than that of the conventional strip-cell MOSFET, respectively, because of the larger channel areas. Additionally, Fig. 4 shows that their breakdown voltages (BV) are nearly the same. According to Fig. 5, when V_{ds} is low (less than 10 V), C_{gd} represents approximately half of C_{oss} in the conventional strip-cell MOSFET, as indicated by the blue dashed and red dotted lines. In addition, since the abrupt drop occurs at a V_{ds} of 10 V, this implies that the JFET is fully depleted at this point. Therefore, when V_{ds} exceeds 10 V, both C_{gd} and C_{SW} become saturated, and C_{oss} is dominated by C_{BT}, as illustrated in Fig. 1.

As shown in Fig. 6, when V_{ds} is low, C_{oss} decreases as L_{JFET} is shortened from 2.4 μm to 2.0 μm, due to a reduction in C_{gd}. When L_{JFET} is shortened by 0.2 μm, C_{oss} decreases by 2%. However, as V_{ds} increases, the difference between C_{oss} of the various MOSFETs becomes small. This is because C_{gd} decreases more rapidly than C_{ds}, making its influence on C_{oss} less significant. After the abrupt drop, the C_{oss} of different MOSFETs are more consistent, because C_{BT} of each MOSFETs is similar.

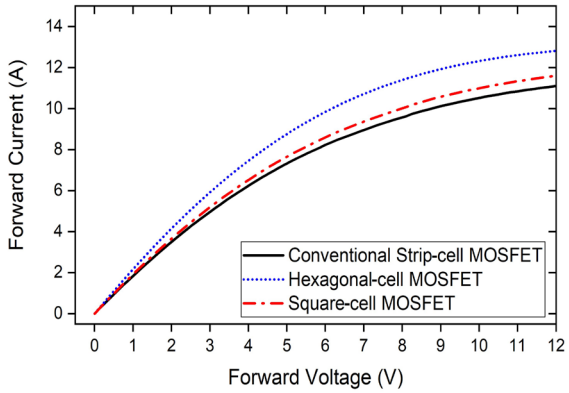

Fig. 3. The measured forward I_{ds}-V_{ds} curves of the MOSFETs with different cell topologies.

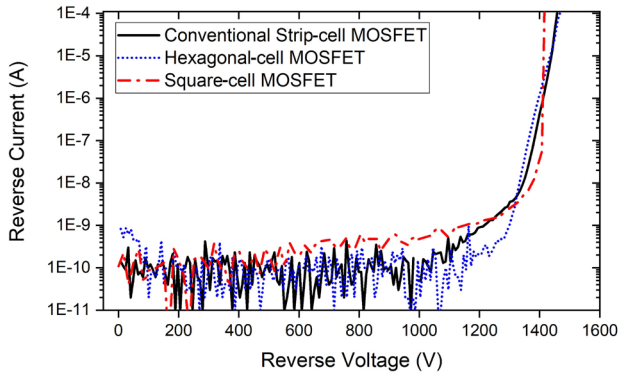

Fig. 4. The measured reverse I_{ds}-V_{ds} curves of the MOSFETs with different cell topologies.

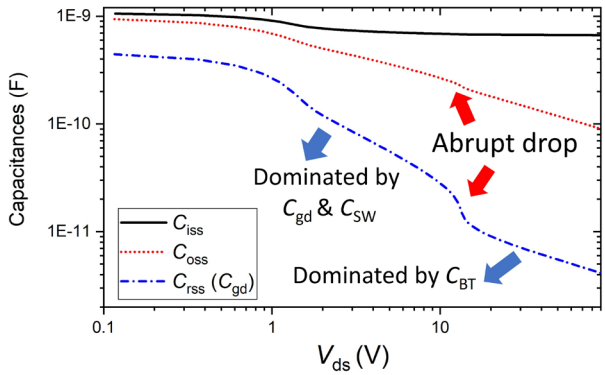

Fig. 5. The measured Ciss, Coss, and Crss (Cgd) of the conventional strip-cell MOSFET.

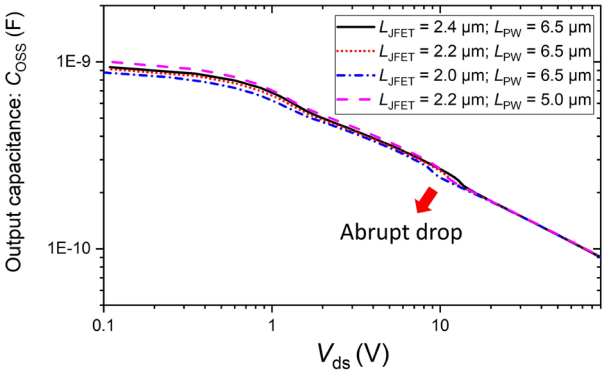

Fig. 6. The measured Coss of the conventional strip-cell MOSFETs with different L_{JFET} and L_{PW}.

From Fig. 7, at a low V_{ds}, the C_{oss} of the square and hexagonal-cell MOSFETs are 20% and 25% higher than that of the strip-cell MOSFET, respectively, because of the higher C_{gd} resulting from the larger JFET area and higher C_{SW} resulting from more sidewalls of Pwells. Nevertheless, after the abrupt drop, the C_{oss} of the square and hexagonal-cell MOSFETs becomes slightly lower than that of the strip-cell MOSFET, owing to their smaller P-well areas. Even though the difference in C_{oss} is relatively small, high-voltage switching can still cause considerable variations in space charge and significantly affect I_{rr}. Additionally, it can be inferred that when C_{oss} is higher at low V_{ds}, it may be lower at high V_{ds} when the chip area of the MOSFET is fixed.

As shown in Fig. 8, C_{gd} can be reduced not only by shortening L_{JFET} or decreasing the JFET area, but also by reducing the poly-gate area. Therefore, a split-gate MOSFET with the poly-gate length reduced by 1.0 μm exhibits a 28% reduction in C_{oss} at low V_{ds}. However, a smaller poly gate reduces the depletion capability of the MOSFET, leading to a higher C_{ds}. As a result, after C_{gd} saturates, the C_{oss} of the split-gate MOSFET may become higher than that of the conventional MOSFET, and the abrupt drop occurs later since the JFET should be fully depleted at a higher V_{ds}.

According to Fig. 9, when L_{JFET} decreases, C_{gd} is reduced, allowing the MOSFET to turn on more quickly. Therefore, the turn-on time (t_{on}) is shortened. However, I_{rr} may increase due to the larger P-well area, which leads to a higher C_{ds}. Hence, it can be concluded that there is a trade-off between t_{on} and I_{rr}. In addition, it is found that the MOSFET with L_{JFET} and L_{PW} of 2.2 μm and 6.5 μm, respectively, achieves an E_{on} of about 8% and 6% lower than those of the other two MOSFETs with L_{JFET} and L_{PW} of 2.0 μm and 6.5 μm, and 2.4 μm and 6.5 μm, respectively, as shown in Fig. 9.

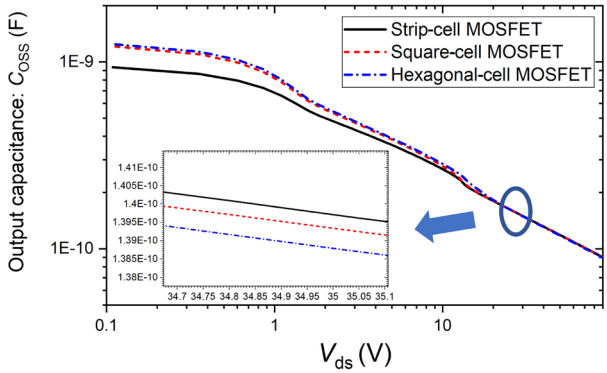

Fig. 7. The measured Coss of the MOSFETs with different cell topologies.

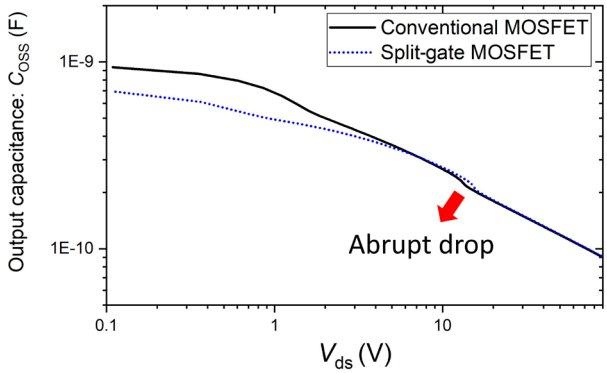

Fig. 8. The measured Coss of the conventional and split-gate MOSFETs.

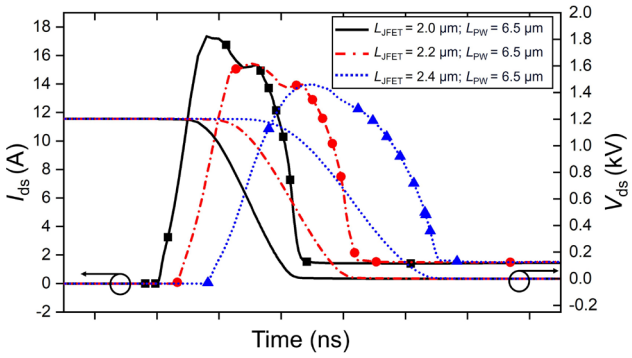

Fig. 9. The simulated turn-on waveforms of the MOSFETs with different structures during DPT.

In this study, a novel MOSFET with partially thickened gate oxide is proposed, as shown in Fig. 10. This design lowers C_{gd} by reducing the gate oxide capacitance, yet it does not significantly affect C_{ds}, since the depletion width of the P-N junction is maintained. As a result, the t_{on} of the novel MOSFET is slightly shorter than that of the conventional MOSFET, whereas the I_{rr} of both MOSFETs remains nearly the same, as shown in Fig. 11. Consequently, the E_{on} of the novel MOSFET is reduced by 5% compared with that of the conventional MOSFET.

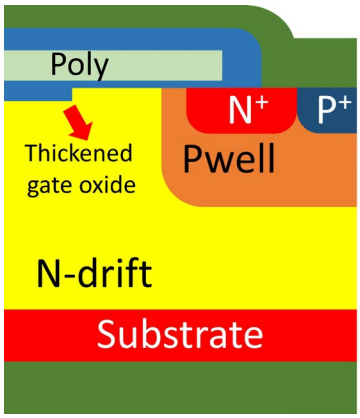

Fig. 10. Schematic of the novel MOSFET with a partially thickened gate oxide.

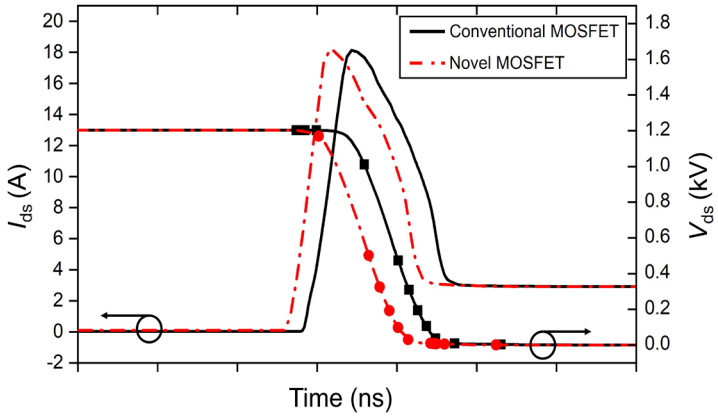

Fig. 11. The simulated turn-on waveforms of the conventional and novel MOSFETs during DPT.

Summary

Before the abrupt drop, C_{oss} is dominated by C_{gd} and C_{ds}, whereas after the abrupt drop, it is dominated only by C_{ds} because JFET is fully depleted. Hence, at low V_{ds}, MOSFETs with a longer L_{JFET} or a larger JFET area, such as hexagonal-cell and square-cell MOSFETs, exhibit higher C_{oss}. At higher V_{ds}, C_{oss} increases with the Pwell area. In addition, although the split-gate MOSFET can reduce C_{gd}, its inferior depletion capability not only delays the occurrence of the abrupt drop but may also lead to an increase in C_{ds}.

C_{gd} and C_{ds} depend on the areas of the JFET and P-well, respectively. Thus, a higher C_{gd} may correspond to a lower C_{ds}. Furthermore, t_{on} and I_{rr} depend on C_{gd} and C_{ds}, respectively. Consequently, a shorter t_{on} results in a higher I_{rr}. This indicates a trade-off between t_{on} and I_{rr}.

This study proposes a novel MOSFET with a partially thickened gate oxide, which shortens t_{on} but ensures that I_{rr} does not increase excessively. According to the simulation results, the E_{on} of the novel MOSFET is 5% lower than that of the conventional MOSFET.

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