Key Engineering Materials
ISSN: 1662-9795, Vol. 1057, pp 19-27
doi:10.4028/p-6BmS4C

Submitted: 2025-09-09
Revised: 2025-12-15
Accepted: 2026-03-21
Online: 2026-05-21

1.2 kV SiC MOSFET with Reduced Dynamic Losses Enabled by SiN Gate Dielectric

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Keywords: SiN, high-k, dynamic losses.

Abstract. This paper presents a comprehensive electrical evaluation of a 1.2 kV SiC vertical MOSFET incorporating a novel SiN gate dielectric. Compared to a reference device with thermally grown SiO_2, the proposed MOSFET achieves superior static performance and lower dynamic losses. Notably, the reduced losses stem from a lower gate–drain capacitance (C_{GD}). Furthermore, the novel MOSFET demonstrates superior thermal and electrical stability of the threshold voltage. All these findings underscore the potential of higher-k dielectrics to simultaneously optimize both static and dynamic performances in SiC power MOSFETs, paving the way for more efficient high-voltage power switches.

I. Introduction

Crystalline SiC MOSFETs, with their higher thermal conductivity and wider bandgap, deliver superior electrical performance at high frequencies compared to Si-based power switches [1]. However, integrating crystalline SiC as the transistor bulk material introduces notable processing challenges. Specifically, the growth of a SiO_2 layer on SiC substrates generates interface and oxide traps, which degrade the device's electrical performance [2]. To mitigate these issues, high-k dielectrics offer a promising alternative by potentially reducing interface trap concentration [3] and improving threshold voltage stability [4]. However, these static-performance gains may come at the cost of degraded gate leakage [5] and lower threshold voltage [6]. Moreover, the impact of the high-k gate dielectric on dynamic performances is not yet fully explored. In this work, we present a novel SiC MOSFET with a SiN gate dielectric that outperforms a reference device with SiO_2 gate oxide in both static and dynamic performances.

II. Electrostatic Properties

Two vertical MOSFET devices, sharing the same process flow, except for the gate-dielectric fabrication, are compared. The first split, labeled as "SiO_2", features a thermally grown gate-oxide layer in mixed O_2 and N_2 environment. The second split, labeled as "SiN", incorporates a SiN gate dielectric layer deposited by Low Pressure Chemical Vapor Deposition (LPCVD). The SiN film is made 62.5% thicker than the SiO_2 layer to reduce gate leakage. Fig. 1 shows the input capacitance (C_{iss}) vs. gate-source voltage (V_{GS}) graph. At V_{GS} = 15 V, C_{iss} saturates to a value approximately equal to the gate-dielectric capacitance (C_{ox}). We can express C_{ox} as:

$$C_{ox} = \frac{Ak\varepsilon_0}{t_{ox}}, \tag{1}$$

Where A is the gate area, k is the dielectric constant, ε_0 is the permittivity of free space, and t_{ox} is the gate dielectric thickness. After taking the ratio of (1), we obtain:

$$k^{SiN} = 1.84 \cdot k^{SiO2}, \quad (2)$$

which aligns well with reported values in literature for Si_3N_4 [7].

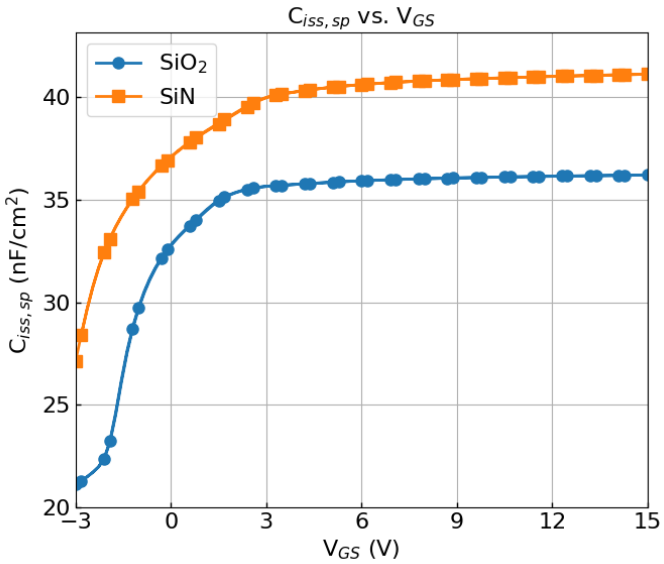
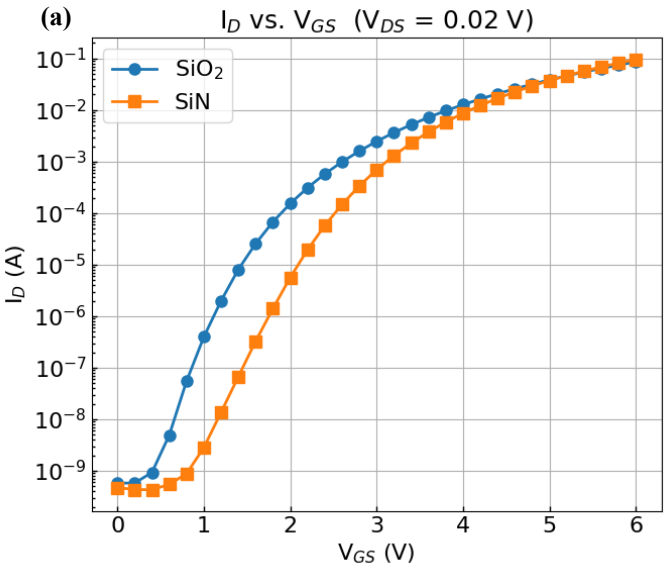


Fig. 1. Area normalized input capacitance ($C_{iss,sp}$) of the SiO_2 (blue) and SiN (orange) MOSFETs measured as V_{GS} ranges from -3 to 15 V.

The higher dielectric constant determines a higher C_{iss} and hence superior control of the channel carrier density with V_{GS}. This can be observed in **Fig. 2 (a)**, where we plot the subthreshold drain current (I_D) vs. V_{GS}, under a low drain-source bias (V_{DS}) of 20 mV. We calculate the average inverse subthreshold slope (STS^{-1}) up to V_{GS} = 6 V, showing STS^{-1}_{SiN} = 660 mV/dec, compared to STS^{-1}_{SiO2} = 750 mV/dec**.** To calculate the threshold voltage (V_{th}), the I_D vs. V_{GS} measurement is repeated on planar MOSFET structures. We extract the transconductance (g_m), defined as:

$$g_m = \frac{\Delta I_{DS}}{\Delta V_{GS}} \quad (3)$$

and we trace the x-axis intercept of the $I_D/(g_m)^{1/2}$ curves, as outlined by the method [8].



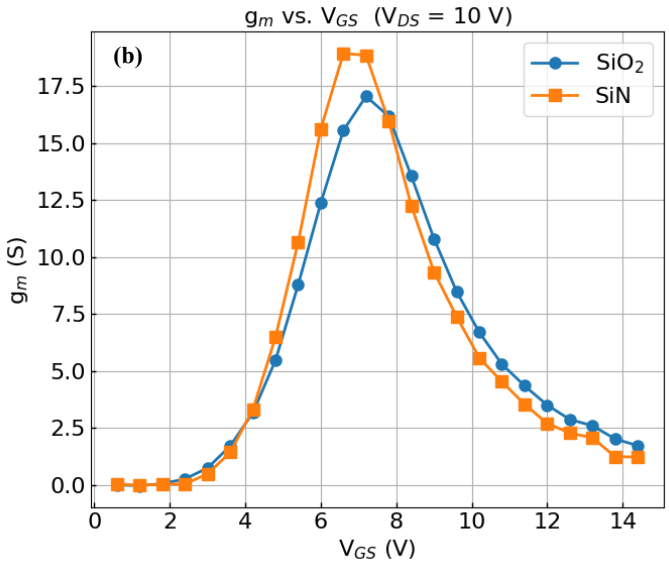


Fig. 2. (a) Subthreshold I_D-V_{GS} characteristics of the SiO_2 (blue) and the SiN (orange) MOSFETs, measured at V_{DS} = 20 mV. The average inverse subthreshold slope (STS^{-1}) values are displayed in the graph. **(b)** Transconductance (g_m) of both devices, measured at V_{DS} = 10 V while sweeping V_{GS} from 0 to 15 V.

We obtain V_{th}^{SiN}= 6.9 V and V_{th}^{SiO2} = 6.7 V, demonstrating a higher-k MOSFET with higher threshold voltage than the SiO_2 reference. In **Fig. 2 (b)**, the g_m of the vertical MOSFETs is compared in the high-power regime under V_{DS} = 10 V, with V_{GS} swept from 0 to 15 V. The SiN MOSFET exhibits an 11% higher peak g_m value, determined by the higher C_{ox}^{SiN}.
In **Fig. 3**, the voltage hysteresis (ΔV_{hyst}) of the two splits is compared using bidirectional V_{GS} sweeps at V_{DS} = 20 mV. The SiO_2 and SiN splits exhibit ΔV_{hyst} = 31 and ΔV_{hyst} = 17 mV, respectively, indicating improved turn-on/turn-off switching stability with the novel SiN gate dielectric.
Fig. 4 benchmarks the static performance of our SiC devices, including our baseline product "*m23*", against three competing 13 mΩ, 1.2 kV-rated SiC MOSFETs. The x-axis represents the V_{GS} values measured by forcing a 10 mA current under the V_{GD} = 0 V condition ($V_{th,10mA}$). The y-axis shows the on-state resistance values extracted at V_{GS} = 18 V for $I_{D,on}$ = 100 A ($R_{DS,on}$).

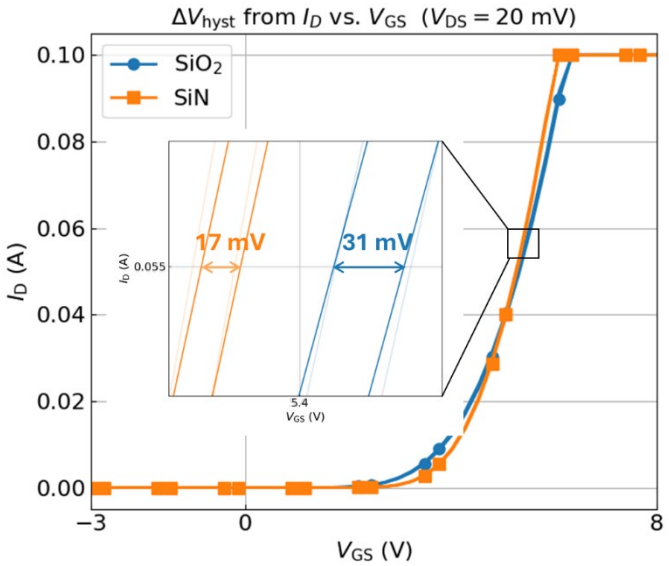


Fig. 3. Voltage hysteresis (ΔV_{hyst}) measured by bidirectional I_D-V_{GS} sweeps for currents up to $I_{D,compliance}$ = 100 mA, performed at 10 V/s of sweep rate.

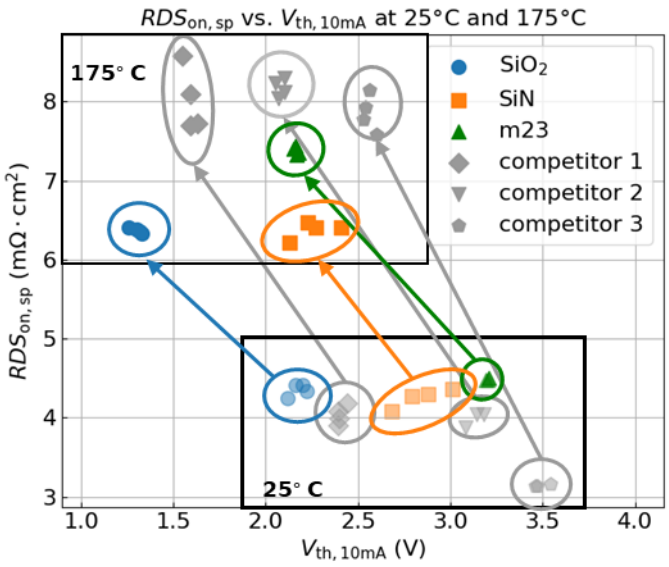


Fig. 4. Y-axis: On-state resistance ($R_{DS,on}$) measured at V_{GS} = 18 V and $I_{D,on}$ = 100 A. X-axis: Threshold voltage ($V_{th,10mA}$), defined as V_{GS} measured while forcing a 10 mA current with V_{GD} = 0 V. The compared splits include our SiO_2 (blue), our SiN (orange), our *m23* product (green), and three other 1.2kV-rated, 13 mΩ- commercial MOSFETs (grey). Transparent colors represent cold (25 °C) data, while opaque colors correspond to hot (175° C) measurements.

The results are compelling:

- Our vertical MOSFETs achieve the best $R_{DS,on}^{175° C}$, ranging between 21 and 26 mΩ.
- Our SiN vertical MOSFET demonstrates superior thermal stability of the threshold voltage ($V_{th,10mA}$), with only a 500 mV shift from 25° C to 175° C (all the other samples exhibit approximately a 1 V reduction). The high $V_{th,10mA}$ is beneficial for short-circuit-safe-operating-area (SCSOA) capability.

Table I. Summary of the static properties of the SiO_2 and the SiN vertical MOSFETs, including blocking performance and gate leakage ($I_{G,leak}$). The breakdown voltage (BV_{DS}) is defined at I_D = 250 µA with V_{GS} = 0 V, while the gate leakage current ($I_{G,leak}$) is measured at V_{GS} = 15 V.

Table I.

Split	Static electric performance					
	STS*$^{-1}$ *(mV/dec)	***Peak* g_m^{25} *(S)***	***V_{th}^{175} (V)***	***R_{DSon}^{175} (mΩ)***	***$I_{G,leak}^{25}$ (nA)***	***BV_{DS}^{25} (V)***
SiO_2	750	17	1.5	21.5	< 0.1	> 1200
SiN	660	19	2.25	22.5	< 0.1	> 1200

III. Dynamic Properties

In the MOSFET turn-on and turn-off processes, a large fraction of the switching losses is dissipated during the Miller Plateau phase [9]. At this stage, the speed of the output voltage (V_{DS}) transition is governed by the gate-drain component of the gate capacitance (C_{GD}) [9,10].

Fig. 5 shows a simplified model of the MOSFET gate capacitance, highlighting the C_{GD} component in red. Under an applied drain voltage (V_D), a depletion region of width w_{dep} forms in the drift region, with:

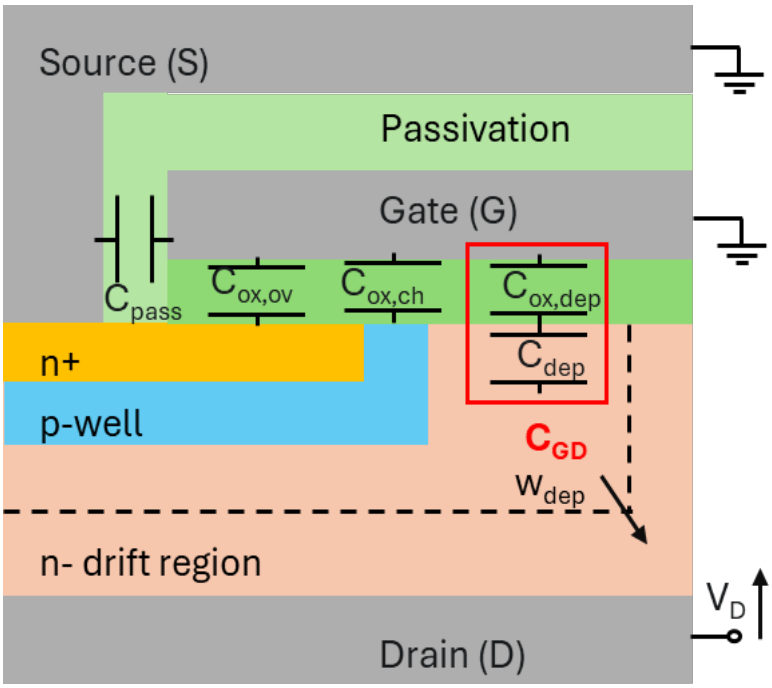


Fig. 5. Gate capacitance model of the vertical MOSFET, highlighting the gate-drain component (C_{GD}) in red, which is given by the series combination of $C_{ox,dep}$ and C_{dep}. $C_{ox,dep}$ is determined by the coupling between gate and oxide/semiconductor interface. C_{dep} arises from the charge modulation in the JFET and drift region. For increasing V_D voltages, the width of the depleted region (w_{dep}) increases.

$$C_{dep} = \frac{\varepsilon_{Si}}{w_{dep}(V_D, C_{ox})} \text{ [9].} \tag{4}$$

For sufficiently high V_D such that:

$$V_D \gg \frac{q\varepsilon_{Si}N_D}{2C_{ox}^2} \text{ [9],} \tag{5}$$

where q is the elementary charge, ε_{Si} is the silicon permittivity and N_D is the doping concentration, the depletion region width (w_{dep}) can be approximated by:

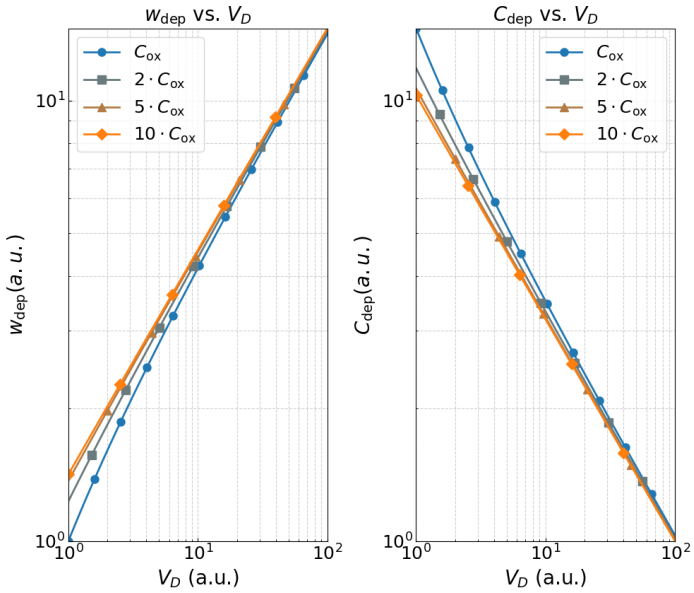


Fig. 6. (a) w_{dep} and **(b)** C_{dep} simulated qualitative trends as functions of V_D and gate oxide capacitance, from a nominal C_{ox} value up to ten times higher ($10 \cdot C_{ox}$). Both x- and y-axis are represented in log scale, to highlight the square root dependence to V_D. These trends assume sufficiently high V_D, as per Eq. (5).

$$w_{dep} \approx \sqrt{\frac{2\varepsilon_{Si}V_D}{qN_D}} - \frac{\varepsilon_{Si}}{C_{ox}} \text{ [9].} \quad (6)$$

From (6), w_{dep} is proportional to $\sqrt{V_D}$, with a correction term equal to $-\frac{\varepsilon_{Si}}{C_{ox}}$.

Fig. 6 (a) illustrates the qualitative trend of the depletion width (w_{dep}) as a function of increasing V_D, under the high V_D approximation of Eq. (5). The trends are shown for different gate oxide capacitances, from a nominal C_{ox} value up to ten times nominal ($10 \cdot C_{ox}$). The effect of a higher oxide capacitance is to induce a wider w_{dep}, especially at lower V_D voltages. Since the depletion capacitance (C_{dep}) is inversely proportional to w_{dep} (Eq. (4)), a higher oxide capacitance results in lower C_{dep} values, as depicted in **Fig. 6 (b)**.

Finally, C_{GD} is the series combination of $C_{ox,dep}$ and C_{dep}, with $C_{ox,dep}$ independent from V_D [9]. **Fig. 7** presents the C_{GD} values experimentally measured for a drain-to-gate voltage (V_{DG}) swept from 10 to 800 V, for both the SiO_2 and the SiN MOSFETs. For V_{DG} > 50 V, C_{GD} shows the same log-log trend as C_{dep} from **Fig. 6 (b)**, so, in this range, C_{GD} is mainly determined by the C_{dep} term. The SiN split exhibits a 5 % lower C_{GD} value on average in the V_{DG} range between 10 to 800 V.

The SiO_2 and SiN vertical MOSFETs were assembled on DBC substrates in the half-bridge configuration, comprising of one MOSFET on the high-side and one on the low-side, and measured according to the double-pulse testing (DPT) sequence, as described in [9].

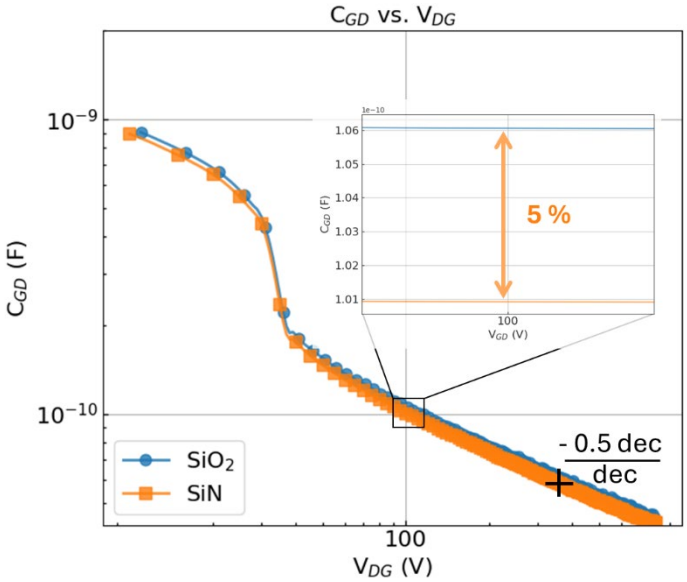


Fig. 7. C_{GD} of the SiO_2 (blue) and SiN (orange) MOSFETs measured by sweeping the gate-to-drain voltage (V_{DG}) from 10 to 800 V.

Fig. 8 (top), (center) and (bottom) show the turn-on waveforms at 125° C of the gate-source voltage (V_{GS}), drain-source voltage (V_{DS}) and drain current (I_D), respectively, at a stray inductance (L_S) of 50 nH, R_G = 40 Ω, and 800 V of DC link voltage. Before the Miller Plateau is reached, the SiO_2 MOSFET shows a slower dI_D/dt rate, due to the higher C_{iss} value. When the Miller Plateau is reached, the SiN MOSFET shows a faster dV_{DS}/dt rate, due to the lower average C_{GD} from 800 V to few V.

By reducing the R_G values, a faster turn-on process is achieved and, consequently, lower dynamic losses. **Fig. 9** presents the turn-on switching losses (E_{on}) measured for R_G = 10, 20 and 40 Ω. The SiN MOSFET exhibits comparable losses at lower di/dt rates, demonstrating a superior turn-on performance.

Fig. 10 (top), (center) and (bottom) show the turn-off waveforms at 125° C of the gate-source voltage (V_{GS}), drain-source voltage (V_{DS}) and drain current (I_D), respectively, at a stray inductance (L_S) of 50 nH, R_G = 40 Ω, and 800 V of DC link voltage. The lower C_{GD} of the SiN MOSFET determines a faster V_{DS} voltage ramp up, which in turns enables an earlier fall of the drain current I_D, yielding lower energy losses. For R_G = 10 Ω, large oscillations exceeding 20 V build up at the gate

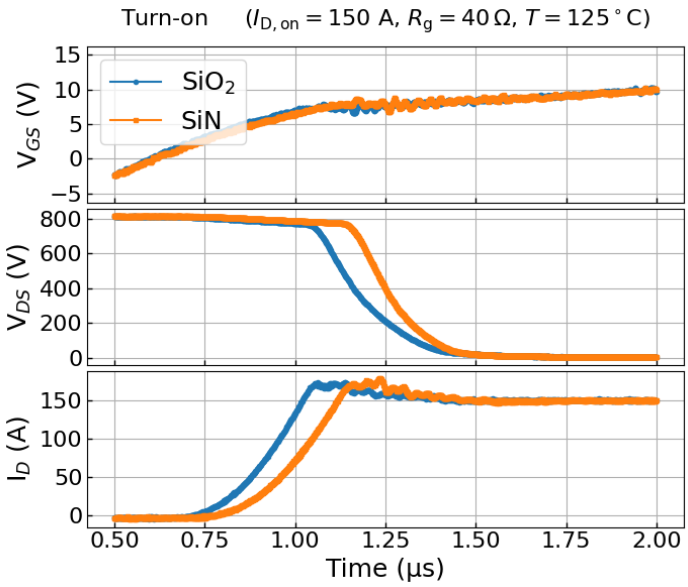


Fig. 8. Top: V_{GS} turn-on waveform, from -5 to + 15 V, at T = 125° C, using R_g = 40 Ω and $I_{D,on}$ = 150 A. **Center:** V_{DS} turn-on waveform. **Bottom:** I_D turn-on waveform.

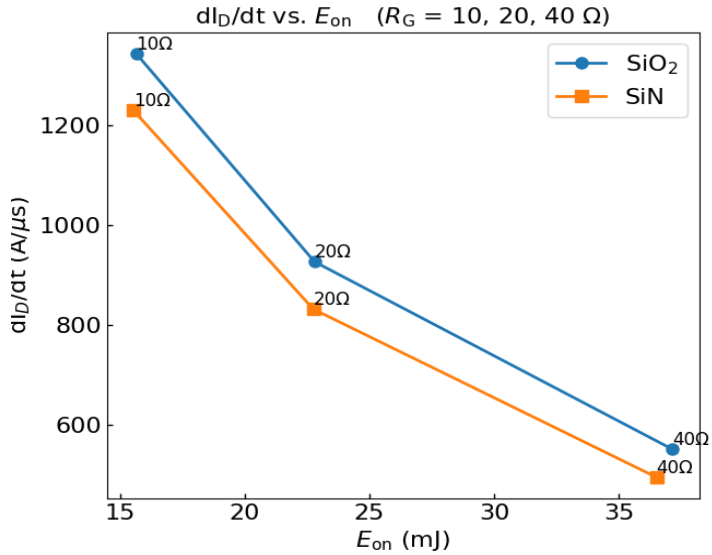


Fig.9. Turn-on dI_D/dt and switching losses (E_{on}) for R_G = 10, 20 and 40 Ω.

node (not shown). The peak amplitude of the V_{GS} oscillations (ΔV_{GS}^{peak}) was measured and plotted in **Fig. 11** against the turn-off losses (E_{off}), for R_G = 10, 20 and 40 Ω. The SiN MOSFET exhibits lower ΔV_{GS}^{peak} at lower E_{off}, proving a superior turn-off performance. The voltage oscillations observed at the drain node with R_G = 10 Ω are comparable in the two splits: $V_{DS,peak}^{SiO2}$ = 995 V and $V_{DS,peak}^{SiN}$ = 1007 V (not shown).

IV. Conclusions

We have presented a 1.2 kV rated vertical SiC MOSFET incorporating a SiN gate dielectric that outperforms a reference device with SiO_2 gate oxide in both static and dynamic performances. Notably, the SiN split demonstrates superior STS^{-1}, g_m, ΔV_{hyst}, $\Delta V_{th}^{25\rightarrow175°C}$, while also delivering lower E_{on} and E_{off} losses at comparable switching conditions. The reduced dynamic losses are attributed to the lower gate-drain capacitance (C_{GD}) observed with the SiN gate dielectric.

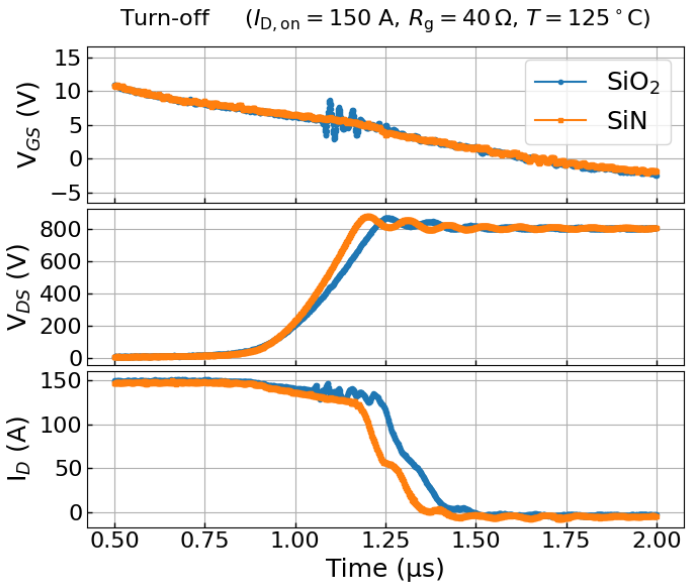


Fig. 10. Top: V_{GS} turn-off waveform, from + 15 to -5 V, at T = 125° C, using R_g = 40 Ω and $I_{D,on}$ = 150 A. **Center:** V_{DS} turn-off waveform. **Bottom:** I_D turn-off waveform.

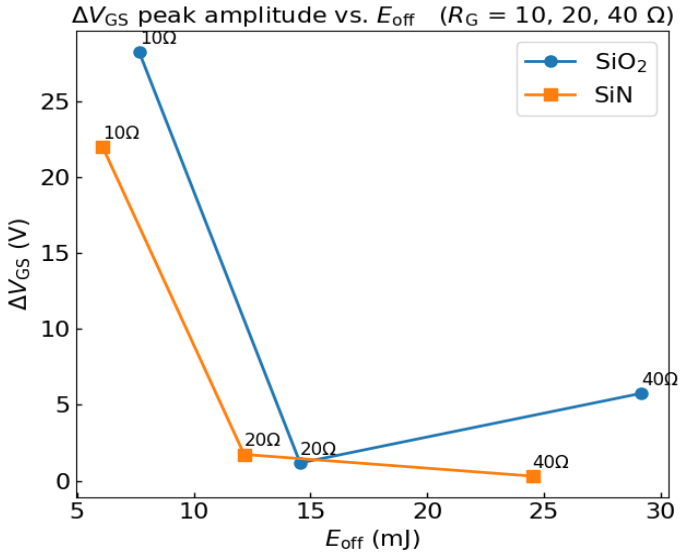


Fig. 11. Turn-off oscillations peak amplitude vs. losses (E_{off}) for R_G = 10, 20 and 40 Ω.

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