Key Engineering Materials
ISSN: 1662-9795, Vol. 1057, pp 29-34
doi:10.4028/p-IkqQM7
© 2026 The Author(s). Published by Trans Tech Publications Ltd, Switzerland.
Submitted: 2025-09-10
Revised: 2025-12-23
Accepted: 2026-03-08
Online: 2026-05-21

Investigation of SiC MOSFETs Gate Capacitance Peak with Biased Drain and its Relation with Transconductance

Ilaria Matacena[1,a*], Luca Maresca[1,b], Alessandro Borghese[1,c], Michele Riccio[1,d], Andrea Irace[1,e], Giovanni Breglio[1,f] and Santolo Daliento[1,g]

[1]Department of Electrical Engineering and Information Technology, University of Naples Federico II, Naples, Italy

[a]ilaria.matacena@unina.it, [b]luca.maresca@unina.it, [c]alessandro.borghese@unina.it, [d]michele.riccio@unina.it, [e]a.irace@unina.it, [f]breglio@unina.it, [g]daliento@unina.it

Keywords: capacitance measurements, capacitance peak, transconductance, gate capacitance.

Abstract. SiC MOSFETs still suffer from some open issues, such as the high density of defects existing at the SiC/SiO_2 interface. Traps distribution at such interface is complex and it affects the overall performance of the device. Traps influence both current-voltage (I-V) and capacitance-voltage (C-V) characteristics of a SiC MOSFET. In this work, we study the relation of Gate capacitance with biased Drain and transconductance with the aim of investigating the channel properties. The analysis is performed using both experimental setup and numerical framework. Experimental and numerical results both exhibit a sharp capacitance peak in the inversion region at a voltage where transconductance reaches its maximum.

Introduction

SiC MOSFETs are gradually replacing their Si counterparts in various applications, thanks to their higher performance. Besides being a wide bandgap material, SiC also exhibits a higher thermal conductivity [1], supplanting Si in power industry. Although SiC technology has experienced huge progress in last decades, there are some open challenges that have to be addressed. Among them the high defect density at SiC/SiO_2 interface is a crucial feature that has to be investigated since it can negatively influence important parameters, such as threshold voltage instability [2], channel mobility [3] and leakage current, affecting the performance of the overall device. Interface traps influence both current-voltage (I-V) and capacitance-voltage (C-V) characteristics of a SiC MOSFET. Due to the importance of SiC/SiO_2 interface defect density [4], several techniques have been investigated to characterize such interface. Among these, the most used methods are based on the measurement of impedance, and more in detail capacitance varying with voltage. These techniques are extensively employed across a wide spectrum of applications, including semiconductor devices and solar cells [5]-[13], as well as batteries [14]. The method is non-destructive and it enables a rapid characterization process. In the literature, most investigations on power devices have focused on MOS structures, where the low–high frequency capacitance technique can be applied [15]-[19]. In such structures, the capacitance response strongly depends on the applied frequency [20], and this dependence provides valuable insight into the nature of defects and traps within the device under test. Specifically, the inversion charge can follow the applied excitation only at sufficiently low frequencies, due to the limited thermal generation of carriers in the depletion region. Consequently, in the inversion regime, the capacitance behavior is primarily governed by the inability of the inversion charge to respond to high-frequency signals. However, this condition is strictly valid for MOS capacitors.

In MOSFETs, the situation differs because, in the inversion region, the channel is replenished with carriers from the Source and Drain. As a result, the capacitance in inversion does not exhibit significant variation between low and high frequency, rendering the low–high frequency method unsuitable for these devices [21]. Therefore, it becomes essential to conduct a precise analysis of the capacitance associated with MOSFETs. This can be achieved using numerical frameworks capable of characterizing the SiC/SiO_2 interface properties [22]-[26]. Capacitance measurements are typically

This article is an open access article under the terms and conditions of the Creative Commons Attribution (CC BY) license
(https://creativecommons.org/licenses/by/4.0)

performed at the Gate terminal, with the Drain connected and the Source terminal tied to reference [27]-[29].

In our previous works [25], [30]-[33], we explored non-standard C–V measurement approaches on commercially available planar SiC MOSFETs. In those studies, experimental data were obtained by applying a small-signal AC excitation at the Gate while maintaining a fixed DC bias at the Drain, with the Source grounded. The resulting capacitance revealed an anomalous peak in the inversion region, attributable to both the interface properties and the channel region.

In this work, we investigate the correlation between the capacitance peak observed in the non-classical C-V characteristics and the transconductance behavior of SiC MOSFETs. To this end, the C-V curves are analyzed under the described measurement configuration, while the derivative of the I_D-V_{GS} characteristics is evaluated to extract the device transconductance. The experimental findings are confirmed by numerical results obtained using the Sentaurus TCAD environment. The remainder of the paper is organized as follows: the experimental setup is described in the next section, while the TCAD numerical setup is discussed in a separate section. Finally, the main conclusions are summarized in the last section.

Experimental Analysis

Experimental results are obtained on two different 1.2 kV planar SiC MOSFETs commercially available using the setup shown in Fig. 1i. The presented curves are obtained by measuring the capacitance arising between Gate and Source terminals, while a DC bias is applied to Drain terminal, V_{DS}. The excitation consisted of a DC sweep from –10 V to +10 V with a superimposed small-signal AC component (Fig. 1ii) applied to the Gate of the device under test. A fixed DC bias (Fig. 1iii) was applied to the Drain, while the Source was grounded. The measured Gate capacitance with the Drain biased at fixed positive values is reported as a red line in Fig. 2 for the first device considered. The capacitance exhibits the classical behavior in accumulation and depletion. Conversely, in the inversion region, when $V_{DS}\neq0$ V, a sharp peak emerges. Capacitance obtained on the other device under test is reported in Fig.3 in red. In this plot, there a several capacitance curves obtained with increasing V_{DS}. These curves exhibit the same behavior found in Fig. 2. In the inversion region, capacitance shows an unexpected peak whose amplitude increases with higher V_{DS}. In previous studies, the peak profile was attributed to traps located in the channel region beneath the SiC/SiO_2 interface [22]. Since interface traps in the channel affect this region physical properties, they have considerable impact on I_D-V_{GS} characteristics. Hence for the devices under test, we also measured the transfer characteristics, with the aim of investigating the relation between the capacitance peak and the transconductance behavior. The derivative of the I_D-V_{GS} characteristics, i.e. the transconductance, for both the device under tests are reported in Fig. 2 and Fig. 3 as blue curves. Experiments show that the derivative of I_D-V_{GS} characteristics, obtained for the same V_{DS} imposed in the C-V measurements, shows a maximum at the same voltage where the capacitance peak occurs, for both studied devices.

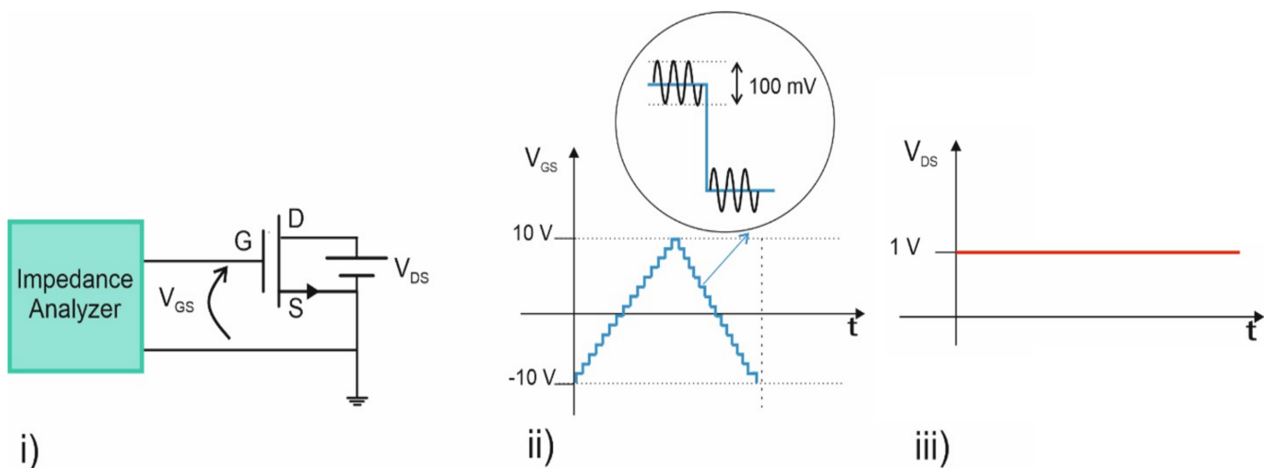
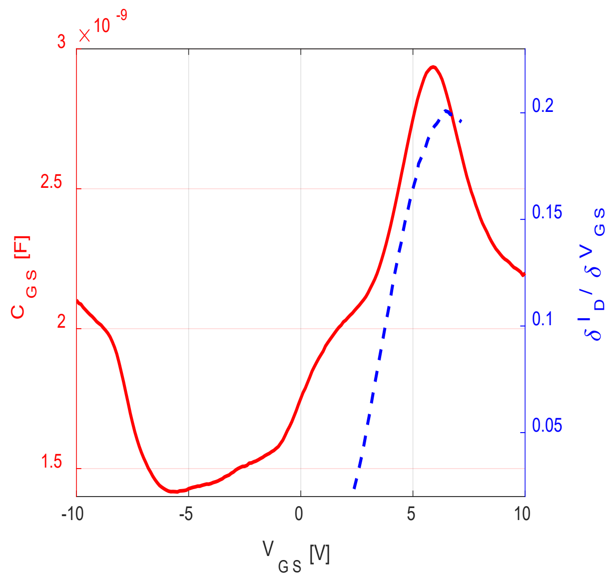


Fig. 1. i) Experimental setup; ii) applied Gate voltage; iii) applied Drain voltage.



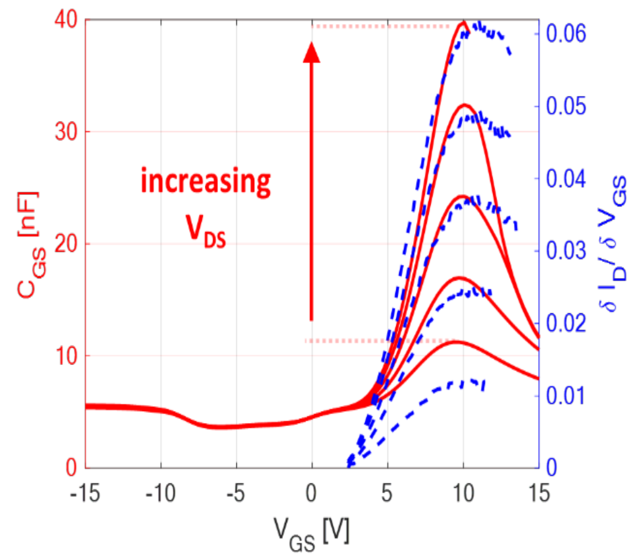


Fig. 2. Experimental C-V curves obtained from a commercial device, 1.2 kV SiC MOSFET, with positive V_{DS} (red line, left y-axis) and corresponding transconductance (blue line, right y-axis).

Fig. 3. Experimental C-V curves obtained from a commercial device, 1.2 kV SiC MOSFET, with positive V_{DS} (red lines, left y-axis) and corresponding transconductance (blue lines, right y-axis).

Numerical Analysis

The consistency of the experimental findings was further investigated through numerical simulations carried out within the Synopsys Sentaurus TCAD framework. The simulated device structure is depicted in Fig. 4, where the geometrical layout and material parameters were carefully defined to reproduce the actual device under test. In particular, the channel region was modeled by incorporating reduced carrier mobility and defect-related effects, thus reflecting the physical non-idealities typically observed in this region. To investigate the capacitive response, an AC small-signal analysis was performed under various biasing conditions, with a DC potential applied to the Drain terminal while the Gate voltage was swept across the operating range. This approach enabled the extraction of capacitance characteristics, which are strongly influenced by the transport properties of the channel. The resulting C-V curves are reported in Fig. 5 as red traces for different channel doping values. The numerical current-voltage curves were also obtained in the same circumstances. The obtained derivative of the numerical I_D-V_{GS} characteristics is also shown in Fig. 5 in blue. Observing curves in Fig. 5, it is possible to see that the capacitance and transconductance peaks occur at the same voltage. These results demonstrate excellent agreement with the experimental measurements. In particular, the capacitance peak (blue traces), obtained for different sets of channel parameters, appears at the same bias voltage at which the corresponding transconductance (red traces) exhibits its maximum value. Simulation findings indicate that the C_{GS} peak coincides with the g_m maximum in terms of both peak value and corresponding voltage, revealing a strong relation of both parameters in accordance with [34].

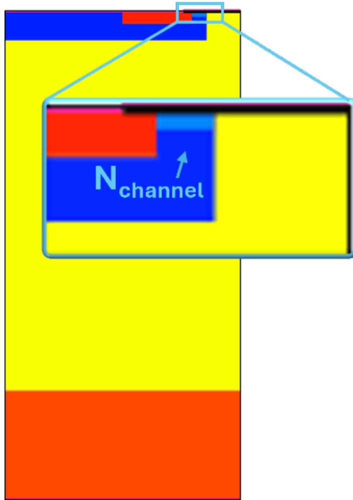


Fig. 4. Sketch of the TCAD structure. The structure is not to scale.

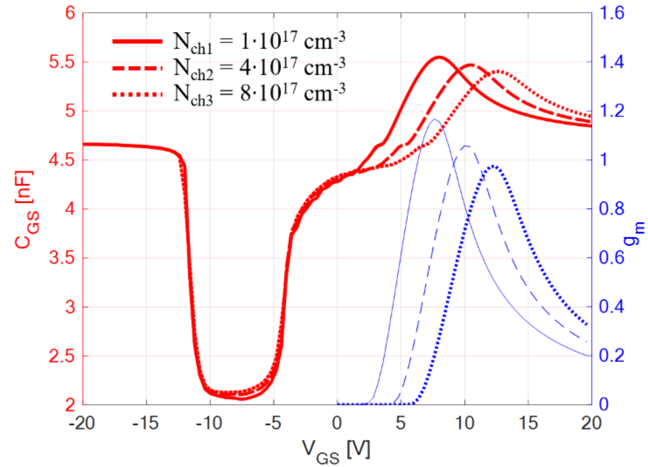


Fig. 5. Numerical C-V curves obtained with a positive V_{DS} (red curves, left y-axis) and corresponding transconductance (blue lines, right y-axis) from structure of Fig. 4.

Conclusion

In this work, we performed non-classical C-V measurements on commercially available planar SiC MOSFETs. Experimental results were obtained by measuring the capacitance arising between Gate and Source terminals, while a fixed DC bias is applied to Drain terminal. The capacitance measured in this configuration showed a non-negligible peak. The arising peak appeared more prominent as the applied Drain voltage increases and its shape is related to the traps in the channel region under the SiC/SiO_2 interface. Since interface traps in the channel affect this region physical properties, they have considerable impact on I_D-V_{GS} characteristics. Hence for the devices under test, transfer characteristics were also measured, with the aim of investigating the relation between the capacitance peak and the transconductance behavior. Experiments showed that the derivative of I_D-V_{GS} characteristics, obtained for the same V_{DS} imposed in the C-V measurements, exhibits a maximum at the same voltage where the capacitance peak occurs, for both studied devices. In order to better understand experimental outcomes, a numerical analysis was performed in Sentaurus TCAD environment. Numerical curves presented exhibited the same experimental behavior: the capacitance peak obtained for different channel properties occurs at the same voltage where the transconductance reaches its maximum. This correlation highlights the direct link between the channel transport properties and the observed capacitance behavior, confirming that the adopted characterization technique is directly related to transconductance and it could be able to give information about channel properties.

References

[1] B. J. Baliga, Fundamentals of power semiconductor devices, Springer Science & Business Media, (2010).

[2] C. Raynaud, et al., Comparison of trapping–detrapping properties of mobile charge in alkali contaminated metal-oxide-silicon carbide structures, Applied physics letters 66, no. 18: 2340-2342, (1995).

[3] D. Peters et al., Investigation of threshold voltage stability of SiC MOSFETs, ISPSD, (2018).

[4] V. V. Afanasev, et al., Intrinsic SiC/SiO2 interface states, physica status solidi (a) 162, no. 1: 321-337, (1997).

[5] Lancellotti, L., Lisi, N., Veneri, P. D., Bobeico, E., Matacena, I., & Guerriero, P. (2019, July). Graphene-on-Silicon solar cells with graphite contacts. In 2019 International Conference on Clean Electrical Power (ICCEP) (pp. 199-203). IEEE.

[6] Gobbo, C., Di Palma, V., Trifiletti, V., Malerba, C., Valentini, M., Matacena, I., ... & Tseberlidis, G. (2023). Effect of the ZnSnO/AZO interface on the charge extraction in Cd-free kesterite solar cells. Energies, 16(10), 4137.

[7] Sonnet, A. M., Hinkle, C. L., Heh, D., Bersuker, G., & Vogel, E. M. (2010). Impact of semiconductor and interface-state capacitance on metal/high-k/GaAs capacitance–voltage characteristics. *IEEE transactions on electron devices*, *57*(10), 2599-2606.

[8] Lancellotti, L., Bobeico, E., Della Noce, M., Veneri, P. D., & Matacena, I. (2018, June). Work function determination of transparent contact for a: Si/c-Si heterojunction solar cells. In 2018 IEEE International Conference on Environment and Electrical Engineering and 2018 IEEE Industrial and Commercial Power Systems Europe (EEEIC/I&CPS Europe) (pp. 1-5). IEEE.

[9] Matacena, I., Guerriero, P., Lancellotti, L., Alfano, B., De Maria, A., La Ferrara, V., ... & Daliento, S. (2023). Impedance spectroscopy analysis of perovskite solar cell stability. Energies, 16(13), 4951.

[10] Westerhoff, U., Kurbach, K., Lienesch, F., & Kurrat, M. (2016). Analysis of lithium-ion battery models based on electrochemical impedance spectroscopy. Energy Technology, 4(12), 1620-1630.

[11] Matacena, I., Lancellotti, L., Daliento, S., Alfano, B., De Maria, A., La Ferrara, V., ... & Guerriero, P. (2023). Impedance Spectroscopy of Perovskite Solar Cells With SnO 2 Embedding Graphene Nanoplatelets. IEEE Journal of Photovoltaics.

[12] Turut, A. (2020). On current-voltage and capacitance-voltage characteristics of metal-semiconductor contacts. Turkish Journal of Physics, 44(4), 302-347.

[13] Matacena, I., et al. "Capacitance–Voltage Investigation of Encapsulated Graphene/Silicon Solar Cells." *IEEE Transactions on Electron Devices* (2023).

[14] Gaberšček, M. (2022). Impedance spectroscopy of battery cells: Theory versus experiment. Current Opinion in Electrochemistry, 32, 100917.

[15] Chang, Yao-Wen, et al. "Charge-based capacitance measurement for bias-dependent capacitance." *IEEE Electron Device Letters* 27.5 (2006): 390-392.

[16] Almora, Osbel, et al. "On Mott-Schottky analysis interpretation of capacitance measurements in organometal perovskite solar cells." *Applied Physics Letters* 109.17 (2016).

[17] Gobbo, Carla, et al. "Effect of the ZnSnO/AZO interface on the charge extraction in Cd-free kesterite solar cells." *Energies* 16.10 (2023): 4137.

[18] Matacena, Ilaria, et al. "Forward bias capacitance investigation as a powerful tool to monitor graphene/silicon interfaces." *Solar Energy* 226 (2021): 1-8.

[19] Heerens, W-C. "Application of capacitance techniques in sensor design." *Journal of physics E: Scientific instruments* 19.11 (1986): 897.

[20] Schroder, D.K. Semiconductor Material and Device Characterization, 3rd ed.; Wiley: Hoboken, NJ, USA, 2006.

[21] Hu, Chenming Calvin. "Modern Semiconductor Devices for Integrated Circuits." Part I: Electrons and holes in a semiconductor (2011).

[22] I. Matacena, L. Maresca, M. Riccio, A. Irace, G. Breglio, S. Daliento, & A. Castellazzi, (2022). SiC MOSFET CV Characteristics with Positive Biased Drain. In Materials Science Forum (Vol. 1062, pp. 653-657). Trans Tech Publications Ltd.

[23] L. Maresca et al. Influence of the SiC/SiO 2 SiC MOSFET Interface Traps Distribution on C–V Measurements Evaluated by TCAD Simulations. IEEE Journal of Emerging and Selected Topics in Power Electronics 9.2 (2019): 2171-2179.

[24] Matacena, I., Maresca, L., Riccio, M., Irace, A., Breglio, G., & Daliento, S. (2022, June). Experimental Analysis of CV and IV Curves Hysteresis in SiC MOSFETs. In *Materials Science Forum* (Vol. 1062, pp. 669-675). Trans Tech Publications Ltd.

[25] Matacena, Ilaria, et al. "SiC MOSFET CV Curves Analysis with Floating Drain Configuration." Materials Science Forum. Vol. 1062. Trans Tech Publications Ltd, 2022.

[26] Matacena, Ilaria, et al. "Evaluation of Interface Traps Type, Energy Level and Density of SiC MOSFETs by Means of CV Curves TCAD Simulations." Materials Science Forum. Vol. 1004. Trans Tech Publications Ltd, 2020.

[27] Wei, Jiaxing, et al. "Interfacial damage extraction method for SiC power MOSFETs based on CV characteristics." 2017 29th International Symposium on Power Semiconductor Devices and IC's (ISPSD). IEEE, 2017.

[28] Tsuji, Katsuhiro, et al. "Measurement of MOSFET CV curve variation using CBCM method." 2009 IEEE International Conference on Microelectronic Test Structures. IEEE, 2009.

[29] Jouha, Wadia, et al. "Physical study of SiC power MOSFETs towards HTRB stress based on CV characteristics." IEEE Transactions on Device and Materials Reliability 20.3 (2020): 506-511.

[30] Matacena, Ilaria, et al. "SiC MOSFETs Capacitance study." *e-Prime-Advances in Electrical Engineering, Electronics and Energy* (2023): 100251.

[31] Matacena, I., Maresca, L., Riccio, M., Irace, A., Breglio, G., Castellazzi, A., & Daliento, S. (2023, July). SiC MOSFETs Biased CV Curves: A Temperature Investigation. In *Materials Science Forum* (Vol. 1091, pp. 31-36). Trans Tech Publications Ltd.

[32] Matacena, I., Maresca, L., Riccio, M., Irace, A., Breglio, G., & Daliento, S. (2024). Frequency Investigation of SiC MOSFETs CV Curves with Biased Drain. Solid State Phenomena, 360, 145-149.

[33] Matacena, I., Maresca, L., Riccio, M., Irace, A., Breglio, G., Castellazzi, A., & Daliento, S. (2022, July). SiC/SiO 2 interface traps effect on SiC MOSFETs Gate capacitance with biased Drain. In *2022 IEEE International Symposium on the Physical and Failure Analysis of Integrated Circuits (IPFA)* (pp. 1-5). IEEE.

[34] I. Matacena, A. Irace, S. Daliento and L. Maresca, "Investigation on Gate Capacitance Peak in SiC MOSFETs With Biased Drain," in *IEEE Transactions on Electron Devices*, doi: 10.1109/TED.2025.3638294.