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Insight into Bias-Temperature Instability of SiC MOSFETs Using Charge Pumping and Triple-Sense Threshold Measurements

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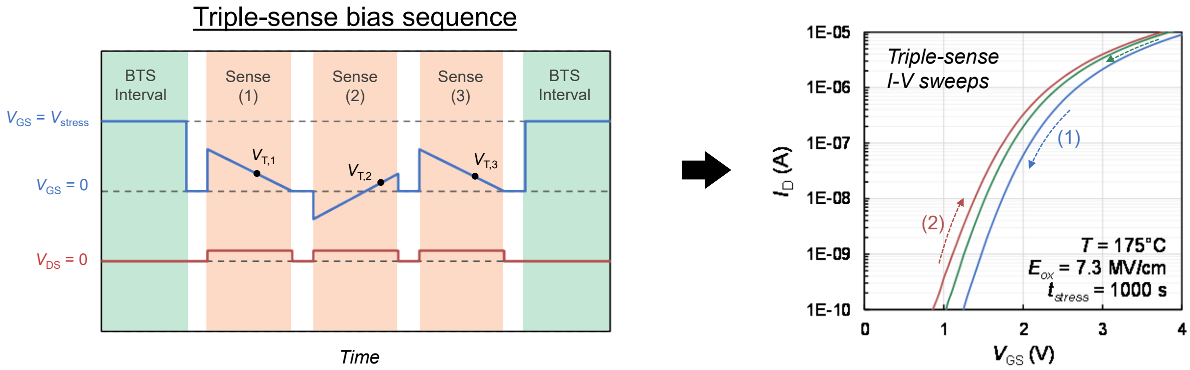
Abstract. Bias-temperature instability (BTI) is one of the primary sources of parameter drift in silicon and SiC MOSFETs and consequently can determine device lifetime. Most studies of BTI in SiC MOSFETs have characterized the threshold voltage (V_T) but not the interface trap density (N_{it}), leaving uncertainty about the relative contributions of carrier capture and trap creation to the V_T shift. In this study, to lend insight into the physical mechanisms responsible for BTI in SiC MOSFETs, we measure N_{it} during positive bias-temperature stress (BTS) using the charge pumping (CP) technique. We also characterize the shift in V_T and hysteresis using the triple-sense method [1], [2] for comparison with the N_{it} changes to evaluate whether the changes in N_{it} are responsible for the V_T and/or hysteresis changes, and demonstrate the utility of the technique for reliable characterization of V_T and hysteresis in SiC MOSFETs.

Introduction

In SiC MOSFETs, the V_T shift with an applied gate bias consists of two components: (i) a fast, reversible hysteresis wherein V_T rapidly shifts back or forth by a finite amount in response to a negative or positive gate bias, and (ii) a quasi-permanent shift of the hysteresis envelope itself with prolonged gate bias [3], [4]. The hysteresis is believed to result from the capture of electrons or holes in interface and border traps. When a sufficiently positive voltage is applied to the gate to form an inversion channel, electrons which accumulate at the interface are captured by these traps and the negative trapped charge shifts V_T positively. Conversely, when a sufficiently negative voltage is applied to the gate to accumulate holes at the oxide-semiconductor interface, the positively charged holes become trapped and shift V_T negatively. For interface traps, the capture rate during inversion and accumulation is very fast compared to emission, so V_T responds rapidly to the change in gate bias, resulting in the observed hysteresis. On the other hand, the physical mechanism responsible for the quasi-permanent V_T shift component is less clear. Generally, the candidate mechanisms are either carrier capture (particularly in border traps), or the creation of new interface traps which can then become charged and contribute to the V_T shift [5]. Many studies have been published which carefully characterize and model the V_T shift according to one mechanism or the other [6], but there is a lack of reports directly measuring the trap density to help confirm or rule out the role of interface trap generation in the V_T shift.

Charge pumping (CP) has been demonstrated to be an effective and versatile technique for measuring N_{it} for both silicon [7] and SiC [8], [9] MOSFETs. Advantages of this technique are that it can be used on a fully fabricated MOSFET (as long as the source and body contact are separated) undergoing the same process conditions as a production MOSFET and containing a p-type body, and it measures N_{it} across most of the semiconductor bandgap, including both donor and acceptor traps on each side of the bandgap, and only excluding traps very close to the band edges. This makes the technique especially useful for measuring the density of traps that affect V_T, which are located deeper than the Fermi level position when the gate is biased near V_T.



(a) (b)

Fig. 1. (a) Bias sequence of the triple-sense method. (b) I_D-V_{GS} curves corresponding to the three V_{GS} of the triple-sense method after a cumulative stress time of 1000 s.

For the purpose of this study, it is also necessary to compare the N_{it} measured by CP with the V_T and the hysteresis as a function of BTS duration. Since the V_T shift for SiC MOSFETs consists of the two components mentioned above, it is critical to have a proper V_T measurement technique to capture the full V_T behavior during BTS, or at least a conditioning step to establish a repeatable MOS interface charge state after each BTS interval. The triple-sense method has been demonstrated to be an optimal method for this purpose [1], [2]. As the name implies, the method uses three gate voltage (V_{GS}) sweeps after each bias stress interval to obtain three V_T sense measurements. A diagram of the bias sequence and the corresponding I_D-V_{GS} curves for the triple-sense method are shown in Fig. 1. In the case of a positive gate bias stress, the first sweep is a down-sweep starting from inversion with minimal delay time after the stress interval to minimize V_T relaxation due to electron emission from the interface/border traps, the second sweep is an up-sweep starting from accumulation in order to rapidly charge the interface positively by hole capture, and the third sweep is final down-sweep starting from inversion to negatively charge the interface again. $V_{T,1}$ obtained from the first sweep thus represents the combined effects of the negative trapped charge that exists during channel inversion and any additional time-dependent electron trapping during the bias stress interval preceding the first sweep, and $V_{T,2}$ and $V_{T,3}$ represent the lower and upper ends of the quasi-permanent hysteresis envelope, respectively, after resetting the interface charge condition with the accumulation bias at the beginning of the second V_{GS} sweep. Therefore, by using three V_{GS} sweeps and corresponding V_T measurements, the triple-sense method can capture all aspects of V_T shift during BTS.

The purpose of this study is to provide insight into the physical mechanisms responsible for the quasi-permanent V_T shift in SiC MOSFETs during BTS. Specifically, the goal is to clarify whether interface traps are generated during BTS and, if so, whether they are responsible for the observed V_T shift. To accomplish this, CP is used to measure N_{it}, and the triple sense method is used to characterize the quasi-permanent V_T shift and hysteresis, after each BTS interval. Finally the magnitudes of the V_T and hysteresis shifts are compared with the N_{it} changes to evaluate whether they are caused by the N_{it} changes.

Experimental Details

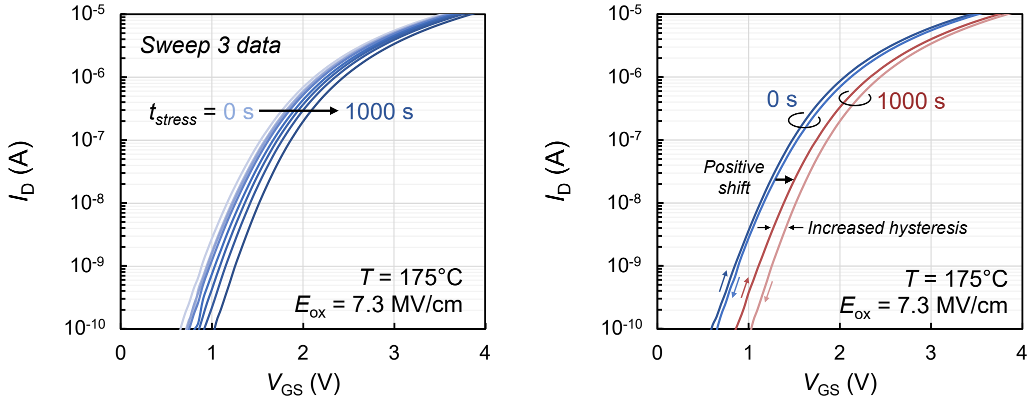
The devices studied are lateral test MOSFETs fabricated on 4° off-axis 4H-SiC epitaxial wafers, with an implanted acceptor concentration of 2×10^{17} cm^{-3} in the channel, a thermal gate oxide formed on the Si face followed by NO annealing, and a channel length and width of 2 μm and 200 μm, respectively. For the BTS, the device temperature was set to 175°C, and a gate voltage well beyond the recommended operating voltage was applied in order to accelerate the V_T shift, which corresponds to an oxide electric field of 7.3 MV/cm. At the same time, this bias is low enough to avoid the onset of additional degradation mechanisms such as impact ionization in the oxide which occur at even higher electric fields [9], [10]. For the triple-sense sequence, V_{GS} was swept down from

15 V to 0 V for the first and third sweep, and swept up from -8 V to 4 V for the second sweep. After each triple-sense sequence the CP sweep is performed using the constant-amplitude method, with a gate pulse amplitude of 15 V, a rise/fall time of 1 µs, and a high/low time of 10 µs.

Results and Discussion

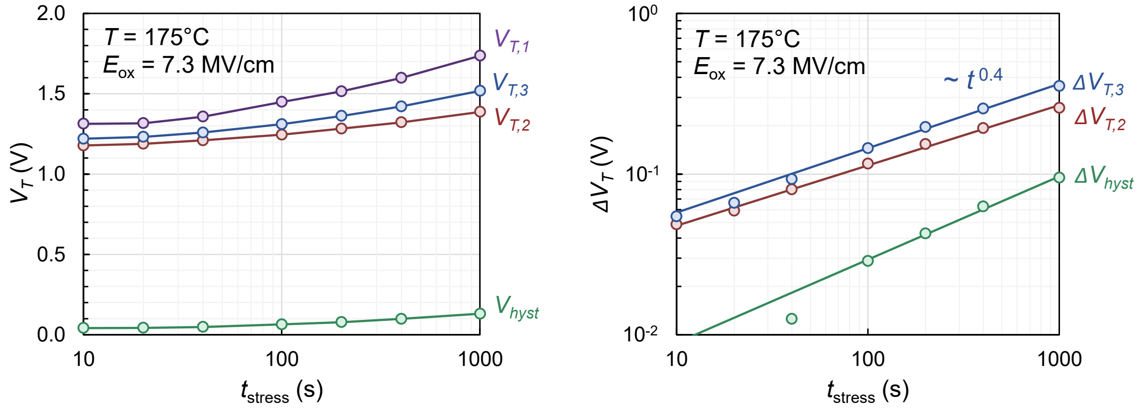
Fig. 2 shows the I_D-V_{GS} characteristics resulting from the triple-sense measurements throughout the BTS experiment. The I_D-V_{GS} curve shifts toward more positive voltages with increasing gate stress time (t_{stress}), and this is accompanied by an increase in the hysteresis between sweep #2 and sweep #3. The increase in hysteresis suggests that an increase in interface and/or border trap density is taking place during the BTS.

By choosing a reference current level to define V_T, each V_T from the triple-sense method can be plotted versus t_{stress} to evaluate the V_T shift and calculate the hysteresis. Fig. 3(a) shows each V_T and the calculated hysteresis (V_{hyst}) versus t_{stress} using a reference current of 10 nA. From this plot the full



(a) (b)

Fig. 2. (a) Triple-sense sweep #3 for each BTS interval from 0 s to 1000 s of cumulative stress time. (b) Sweep #2 and #3 before and after the entire BTS duration, from which both the quasi-permanent V_T and hysteresis can be seen to have increased.



(a) (b)

Fig. 3. (a) Each V_T of the triple-sense method versus stress time using a reference current of 10 nA, and the calculated hysteresis from the difference of $V_{T,2}$ and $V_{T,3}$. (b) The quasi-permanent V_T and hysteresis shifts (referred to the initial values before stress) as a function of stress time. The shifts can be fit to a power law, as is routinely done for BTI measurements.

V_T behavior can be seen as it evolves during the BTS. $V_{T,1}$ is highest value as it contains the maximum contribution of electron trapping effects on V_T with minimal relaxation after each stress interval. $V_{T,2}$ is the lowest value since it results from the up-sweep starting in accumulation which conditions the interface to a positive charge state. $V_{T,3}$ lies between $V_{T,1}$ and $V_{T,2}$ since it results from a down-sweep from inversion which conditions the interface to a negative charge state but comes after the accumulation conditioning of the up-sweep which effectively resets the interface condition after the preceding stress interval. The difference between $V_{T,1}$ and $V_{T,3}$ can then be attributed to any charge trapping occurring during the bias stress interval which responds quickly enough to be eliminated during the accumulation conditioning of the up-sweep; i.e., by recombination during hole capture. $V_{T,2}$ and $V_{T,3}$ together then form the hysteresis envelope, and the shift that each experiences in common can be attributed to the charge trapping or trap generation occurring during the bias stress interval which is too slow to respond or be eliminated during the accumulation conditioning. For this reason, this shift is labelled “quasi-permanent,” and it is the V_T shift that is most relevant during typical MOSFET operation in switching applications.

Fig. 3(b) shows the quasi-permanent shift of $V_{T,2}$ and $V_{T,3}$ over time, as well as the change in hysteresis. Most of the shift is common between $V_{T,2}$ and $V_{T,3}$, but there is also a small increase in the hysteresis as the two V_T values slowly diverge with time. Since the triple-sense sweep and timing parameters are constant along the BTS duration, any change in hysteresis should be related to a change in trap density. This is where CP measurements can provide additional insight by characterizing N_{it} during BTS as well.

The change in N_{it} as a function of t_{stress} measured by CP is shown in Fig. 4. The CP measurements confirm that additional interface traps are indeed generated during the BTS, which is consistent with the observed increase in hysteresis from the triple-sense measurements. The N_{it} change is quite small compared to the typical values measured for SiC MOS devices [8], [9], [11], which is also consistent with the fact that the hysteresis change is small relative to the quasi-permanent V_T shift.

To characterize the change in N_{it} further, the rise and fall times of the charge pumping gate pulse were varied in order to modulate the upper and lower bounds of the energy window of interface traps measured within the SiC bandgap and thus extract the interface trap density energy distribution (D_{it}) close to the valence band edge (E_V) and close to the conduction band edge (E_C) [9]. Since this procedure is more time intensive, it was performed once before the BTS experiment and once after the total 1000 s duration, to compare the D_{it} profile before and after stress. Furthermore, to extend the energy range of the D_{it} distribution that could be extracted, the procedure was repeated at two measurement temperatures: 25°C and 125°C.

The resulting D_{it} profile on each side of the bandgap before and after the BTS is shown in Fig. 5. The baseline D_{it} distribution is consistent with previous observations for Si-face SiC MOSFETs [12], [13], [14], with a uniform and relatively low D_{it} near E_V, and an exponential increase near E_C. After

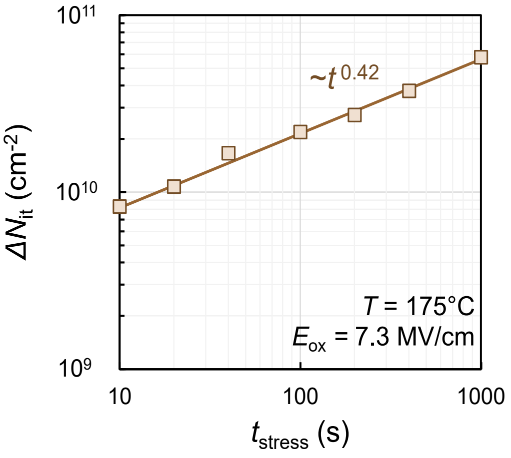
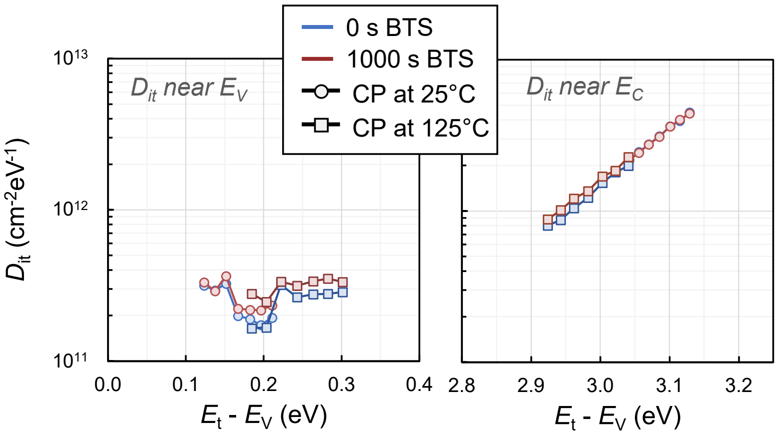


Fig. 4. The change in interface trap density as a function of bias stress time, which also follows a power law similar to the V_T shift.



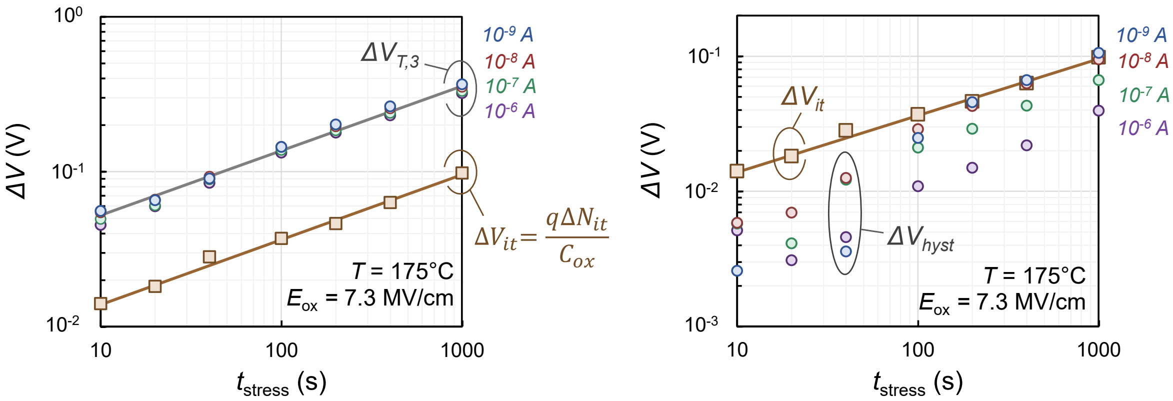
(a) (b)

Fig. 5. The extracted D_{it} profile before and after 1000 s of positive bias-temperature stress (a) in the lower half of the bandgap near the valence band edge and (b) in the upper half of the bandgap near the conduction band edge, obtained by modulating the rise and fall times of the gate voltage pulse during charge pumping.

the BTS, D_{it} increases a small amount evenly on both sides of the bandgap, which means both acceptor and donor interface traps are generated during the BTS.

With both V_T and N_{it} having been measured as a function of stress time, it is now of interest to compare these quantities to evaluate their correlation. To make a quantitative comparison, the quantity $V_{it} = qN_{it}/C_{ox}$ was calculated, where q is the elementary charge and C_{ox} is the specific oxide capacitance of the MOSFET. This quantity represents the total expected gate voltage shift between accumulation and inversion due to the interface trap density measured by CP. In other words, it is the expected hysteresis based on the measured N_{it} value.

Fig. 6(a) shows the change in $V_{T,3}$ and the change in V_{it} plotted together versus t_{stress} for comparison. In the plot, $\Delta V_{T,3}$ is plotted for four different choices of reference current used to extract V_T, which is seen to have minimal impact on the extracted $\Delta V_{T,3}$. The magnitude of $\Delta V_{T,3}$ is about 3× greater than ΔV_{it}, indicating that the V_T shift is caused primarily by factors other than the creation of interface traps, such as electron capture in border traps within the oxide.



(a) (b)

Fig. 6. The change in V_{it} plotted versus stress time alongside (a) the change in $V_{T,2}$ and (b) the change in hysteresis, for comparison of the interface trap density changes measured by CP with the quasi-permanent V_T and hysteresis changes measured with the triple-sense method. $\Delta V_{T,2}$ and ΔV_{hyst} are each plotted for four different choices of reference current used to extract V_T.

In Fig. 6(b), the change in hysteresis and the change in V_{it} are plotted together versus t_{stress} for comparison. The choice of reference current used to measure V_T is seen to have a significant impact on the ΔV_{hyst} extracted. This can be interpreted as a result of the different amounts of band bending which occur depending on the current level used, which changes the energy range of the interface trap distribution causing the hysteresis. For the lower current levels, ΔV_{it} and ΔV_{hyst} converge with increasing time, indicating that the generated interface traps measured by CP are responsible for the increase in hysteresis during the BTS.

Summary

In summary, using CP measurements and the triple-sense method, we have been able to deduce certain facts about the physical mechanisms responsible for BTI in SiC MOSFETs. First, CP measurements revealed that interface traps are generated during positive BTS. Second, the quasi-permanent V_T shift during sBTS was significantly greater than the voltage shift caused by the generated N_{it}, which allows us to conclude that the V_T shift is not primarily caused by interface trap creation, but by other effects such as charge capture by border traps. Lastly, the hysteresis envelope widened during the BTS, and the magnitude of the change was equal to the voltage shift due to the generated N_{it}, from which we can conclude that the generated interface traps are responsible for the increase in hysteresis. These insights into the physical mechanisms responsible for BTI are valuable for enabling the modeling and prediction of BTI related degradation and parameter shifts in SiC MOSFETs.

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