Key Engineering Materials
ISSN: 1662-9795, Vol. 1057, pp 43-47
doi:10.4028/p-3xeuTP

Submitted: 2025-09-11
Revised: 2025-12-09
Accepted: 2026-03-16
Online: 2026-05-21

Experimental Analysis of 4H-SiC CMOS NOT Logic Gate Down to 100K

Luigi Di Benedetto[1,a*], Nicola Rinaldi[1,b], Mathias Rommel[2,c], Alexander May[2,d], Leander Baier[2,e], Rosalba Liguori[1,f], Alfredo Rubino[1,g] and Gian Domenico Licciardo[1,h]

[1]Department of Industrial Engineering, University of Salerno, Via Giovanni Paolo II, 132, Fisciano, Italy

[2]Fraunhofer Institute for Integrated Systems and Device Technology, IISB, Schottkystraße 10, Erlangen, Germany

[a]ldibenedetto@unisa.it, [b]nrinaldi@unisa.it, [c]mathias.rommel@iisb.fraunhofer.de, [d]alexander.may@iisb.fraunhofer, [e]leander.baier@iisb.fraunhofer.de, [f]rliguori@unisa.it, [g]arubino@unisa.it, [h]gdlicciardo@unisa.it

Keywords: cryogenic temperatures, NOT logic gate, 4H-SiC lateral CMOS technology.

Abstract. In this paper, the electrical characterizations of a 4H-SiC CMOS NOT logic gate are performed in the temperature range from 300K down to 100K and the results are analyzed. The integrated circuit is fabricated with the Fraunhofer IISB 4H-SiC 2μm CMOS technology and the lateral NMOSFET and PMOSFET have channel form factor of 6/6 and 44/6, respectively. The circuit is supplied with a 20V. The curves show a reduction of the threshold voltage from 8.96V to 6.85V reducing the temperature from 300K to 100K and an ever-widening region in the High side (NMOSFET in saturation and PMOSFET in triode regime) compared to the Low side (NMOSFET in triode and PMOSFET in saturation regime). However, the noise margins are still wide enough for practical applications, making the circuit still useful. The behavior can be ascribed to a reduction of the conductivity of the PMOSFET with the decreasing of the temperature. Finally, analysis also focuses on the power dissipation during the transition of the output voltage from high (low) to low (high).

Introduction

Nowadays, 4H-Silicon Carbide semiconductor devices are largely used in power electronics or for high-temperatures applications [1]. Its widespread availability permitted the fabrication of high-quality substrates together with the improvements of the oxidation and of the ion implantation processes provided the basis for the development of new technologies, like 4H-SiC Complementary Metal Oxide Semiconductor, CMOS [2]. Indeed, 4H-SiC CMOS Integrated Circuits have been demonstrated to operate up to 873K [3] or to allow integration of other devices, like diodes [3] or UV [4] sensors, opening new application fields. On the other hand, electronics for space explorations needs good radiation hardness, reducing the shielded package, and capability to operate at temperatures lower than 150K. Moreover, the possibility of a single device to operate from 800K down to 100K with such huge temperature range is interesting both for scientific and for industrial purposes. Actually, only a few papers showed the operability of 4H-SiC devices at cryogenic temperatures from single vertical diodes [5] to power MOSFETs [6] as well as about lateral 4H-SiC MOSFETs [7-8]. However, there are lacks of information about the understanding of 4H-SiC device performances at low temperatures, like the effects of the incomplete ionization of Aluminum or of the interface trap density [9], and experimental results needs for an in-depth analysis.

In this context, our paper shows the electrical performance of a 4H-SiC CMOS NOT logic gate, which is the core circuit for digital electronics. It has been measured in the temperature range from 300K down to 100K with the aim to analyze and understand the limits of 4H-SiC CMOS technology at cryogenic temperatures.

Fabrication Process and Experimental Set-Up

The Fraunhofer IISB 4H-SiC 2μm CMOS technology [2] is used to fabricate the NOT logic gate, where the channel width of the NMOSFET, M_N, and PMOSFET, M_P, are 6μm and 44μm, respectively, whereas the channel length is even to 6μm for both devices. In Fig. 1 a simplified cross-section of the device structures is reported. On a 4H-SiC n-type 350 μm 4° off-axis (0001) substrate, a n-type epitaxial layer is grown with doping concentration of 10^{15} cm^{-3} and thickness of 10μm. Selective doping regions are made through ion implantations of Aluminum and Nitrogen dopant atoms, respectively, for p-type and n-type regions and doping concentrations of $5{\cdot}10^{19}$ cm^{-3}5, 10^{17} cm^{-3}, 10^{16} cm^{-3} are for high doping regions, p-type and n-type wells. After ion implantation, thermal activation annealing at 1973K for 30 minutes is made. Then, thermal gate oxide of 55nm-thick is grown and post-annealed at 1573K in NO ambient and covered with n-type high doped poly-silicon. The resulting gate capacitance, C_{ox}, is equal to 62.8nF/cm^2. Silicide of Ti/Al and NiAl are formed on p^+ and n^+-regions, respectively, and Ti/Pt is used as metal stack layers.

Measurement set-up consists of a HP 4145A for the electrical characterization and of a closed cycle cryo-system attoDRY800xs [10] and the temperature is monitored with a Cernox RTDs temperature sensor [11]. The samples are bonded on special PCB and positioned on the sample holder in order to cool down from 300K to 100K with a temperature step of 25K.

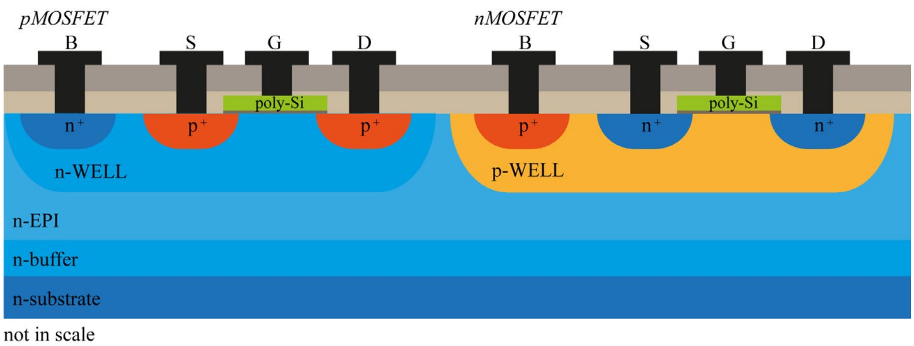

Fig. 1. A cross-section view of the 4H-SiC CMOS device structures.

Experimental Measurements and Discussion of the Analysis

In Fig.2 V_{IN}-V_{OUT} characteristics are shown with a supply voltage, V_{DD}, of 20V and by varying the temperature from 100K to 300K with a step of 25K. At 300K the CMOS NOT has a threshold voltage, V_M, of 8.96V and, hence, is not fully complementary, i.e., $V_M \neq V_{DD}/2$, because NMOSFET is more conductive than PMOSFET.

Observing the curves, the reduction of the temperature modifies the transfer-characteristics both shifting toward lower V_{IN} and decreasing the gain in the transition region. Indeed, in Fig.3 we report V_M as function of the temperature and it changes from 8.96V at r.t. to 8.53V at 200K and to 6.85V at 100K, which is a reduction of –23.55% respect to r.t. It is worth to note that at 100K the value of V_M is still valid as NOT logic gate. Further, the high output voltage, V_{OH}, is 19.98V from 300K to 150K, but decreases to 19.95V at 125K and to 19.64V at 100K, whereas the low output voltage, V_{OL}, is nearly 0V. On the other hand, the variations of the V_M and of the gain cause a significative reduction of V_{IL} and V_{IH} values: from 300K to 100K, V_{IH} decreases from 9.89V to 7.17V and V_{IL} from 8.18V to 5.5V. In Tab.1 the main parameters of the NOT logic gate are reported for different temperatures.

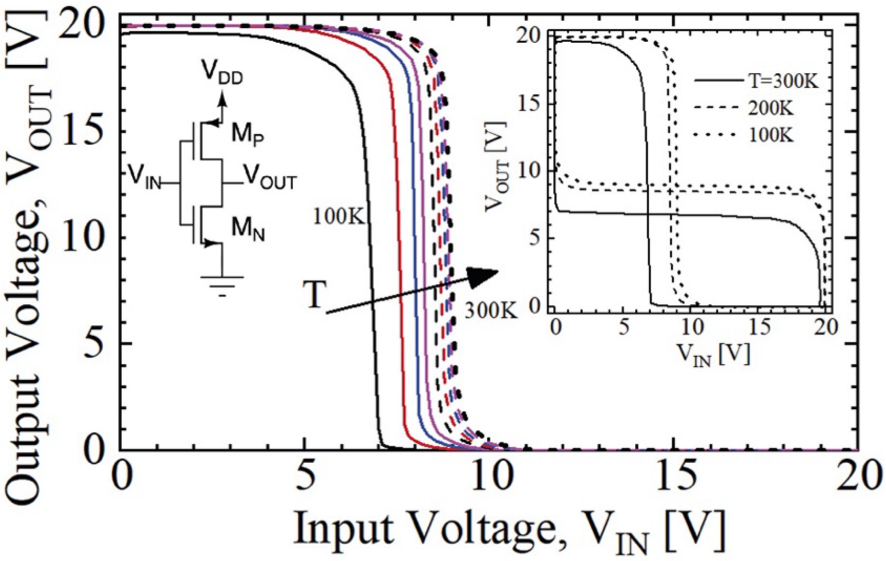

Fig. 2. V_{IN}-V_{OUT} characteristics from 100K to 300K with a T-step of 25K. The inset shows Voltage Transfer Characteristics for the estimation of the Noise Margin and the NOT logic gate

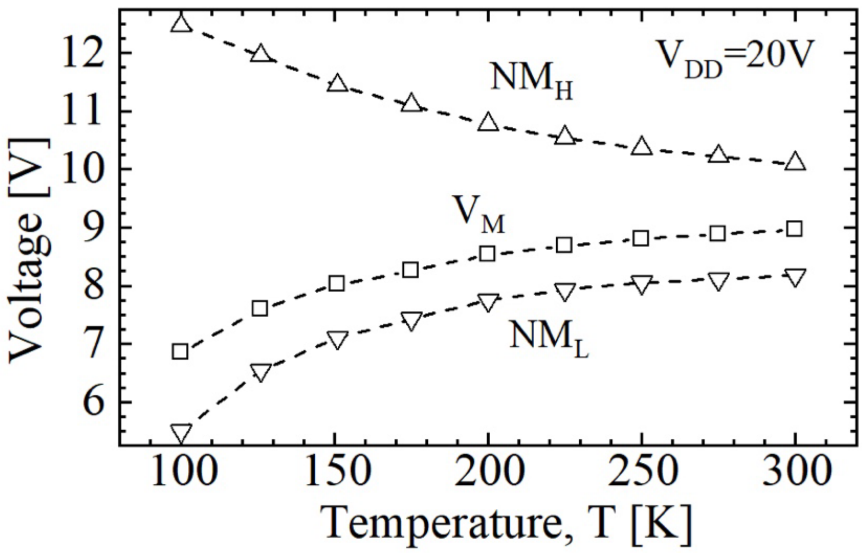

Fig. 3. Threshold voltage, V_M, and High and Low Noise Margin, NM_H and NM_L, as function of the temperature measured at V_{DD}=20V.

Table 1. Parameter of the Voltage-Transfer Characteristic of the 4H-SiC CMOS NOT logic gate as function of the temperature at V_{DD}=20V.

T [K]	V_{IL} [V]	V_{IH} [V]	V_{OL} [V]	V_{OH} [V]	V_M [V]	NM_L [V]	NM_H [V]
100	5.5	7.17	~0	19.64	6.85	5.5	12.47
150	7.11	8.54	~0	19.96	8.02	7.11	11.44
200	7.75	9.21	~0	19.98	8.53	7.75	10.77
250	8.06	9.62	~0	19.98	8.81	8.06	10.22
300	8.18	9.89	~0	19.98	8.96	8.18	10.09

Moreover, in the inset of Fig.2 the area related to the High Noise Margin, NM_H, increases compared to that of Low Noise Margin, NM_L, and in Fig.3 their values are reported. They are defined as $NM_H = V_{OH} - V_{IH}$ and $NM_L = V_{IL} - V_{OL}$. At 300K NM_H and NM_L are worth, respectively, 10.09V and 8.18V and, then, they have different behaviour with the reduction of the temperature: indeed, NM_H increases to 10.77V at 200K and to 12.47V at 100K, whereas NM_L reduces to 7.75V at 200K and to 5.5V at 100K. In Tab.1 detailed results are also reported. In both cases, their values make still useful the circuit for practical applications.

The temperature behavior of the Voltage-Transfer characteristic of NOT logic gate can be ascribed to the reduction of the conductivity of the PMOSFET and to the still valid operation of the NMOSFET down to 100K. Indeed, in [7] 4H-SiC lateral PMOSFET diode-connect temperature sensors vary their characteristics around 175K due to a significative reduction of the field-effect channel mobility, $\mu_{CH,P}$: at a current of 1μA, $\mu_{CH,P}$ is equal to 5.59cm^2/V/s at T=300K and decreases to 0.2cm^2/V/s at 150K, and to 0.07cm^2/V/s at T=100K. Being $\mu_{CH,P}$ proportional to free/trapped carrier ratio, such reduction of $\mu_{CH,P}$ is related to the reduction of the free/trapped carriers ratio with the temperature, because the Fermi level moves toward the valence band [12]. On the other hand, NMOSFET field-effect channel mobility, $\mu_{CH,N}$, decreases from 4.25cm^2/V/s at 300K to 2.9cm^2/V/s at 150K, but then increases to 3.38cm^2/V/s at 100K at a current of 1μA [8].

Finally, Static power dissipation is analyzed through the supply current, I_{DD}, that is normalized with that at r.t., $I_{DD,300K}$, and it is reported as function of V_{IN} in Fig. 4. I_{DD} reduces with the temperature and at 200K is one order lower than 300K until to have more than two orders of magnitude at 100K. This advantageous reduction of the power dissipation is expected when electronic circuits operate at cryogenic temperatures [13].

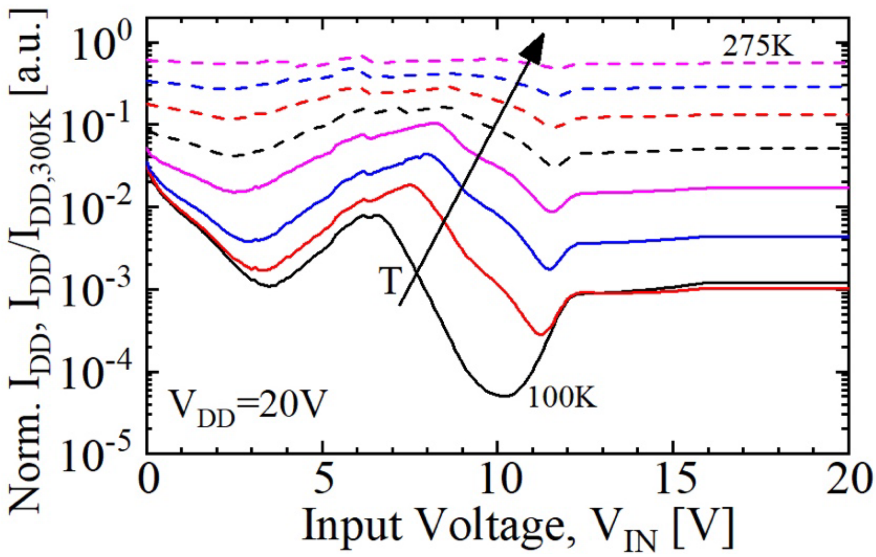

Fig. 4. Normalized supply currents, I_{DD} / $I_{DD,300K}$, respect to 300K as function of the input voltage for temperatures from 100K to 275K with a T-step of 25K and measured at V_{DD}=20V.

Summary

In this paper the voltage transfer characteristics of 4H-SiC CMOS NOT logic gates are measured from r.t. down to 100K showing the operability of the circuit in cryogenic temperature range. Indeed, although a reduction of the threshold voltage and of the low noise margin is evident, the values are still valid for its functionality as logic gate. Also, the expected reduction of the supply current during the transition from high (low) to low (high) output values is confirmed. The worsening of the static characteristic is mainly ascribed to the reduction of the field-effect channel mobility of PMOSFET. To have a complete understanding of the 4H-SiC CMOS NOT logic gate, dynamic characterizations are necessary as well as a long-term performance need to be addressed.

References

[1] P. G. Neudeck, D. J. Spry, L. Chen, N. F. Prokop, and M. J. Krasowski, Demonstration of 4h-sic digital integrated circuits above 800°C, IEEE Electron Device Letters, 38 (2017) 8, 1082–1085.

[2] "Fraunhofer Institute for Integrated Systems and Device Technology (IISB)," https://www.iisb.fraunhofer.de/.

[3] J. Mo, J. Li, Y. Zhang, J. Romijn, A. May, T. Erlbacher, and S. Vollebregt, A highly linear temperature sensor operating up to 600° C in a 4H-SiC CMOS technology. IEEE Electron Device Letters, 44 (2023) 6, 995-998.

[4] L. Di Benedetto, G.D. Licciardo, T. Erlbacher, A.J. Bauer, and A. Rubino, A 4H-SiC UV phototransistor with excellent optical gain based on controlled potential barrier, IEEE Transactions on Electron Devices, 67 (2019) 1, 154-159.

[5] C. D. Matthus, L. Di Benedetto, M. Kocher, A. J. Bauer, G. D. Licciardo, A. Rubino, and T. Erlbacher, Feasibility of 4H-SiC p-i-n Diode for Sensitive Temperature Measurements Between 20.5 K and 802 K, IEEE Sensors Journal 19 (2019) 8, 2871-2878.

[6] Y. Wei, M.M. Hossain, and H. A. Mantooth. Comparisons and evaluations of silicon and wide band gap devices at cryogenic temperature, IEEE Transactions on Industry Applications 59 (2022) 2, 1982-1994.

[7] N. Rinaldi, M. Rommel, A. May, R. Liguori, A. Rubino, G.D. Licciardo, and L. Di Benedetto, Analysis of a 4H-SiC lateral PMOSFET temperature sensor between 14K-482K. IEEE Sensors Letters, 9 (2025) 3, 2501504.

[8] N. Rinaldi, M. Rommel, A. May, R. Liguori, A. Rubino, G. D. Licciardo, L. Di Benedetto, A 4H-SiC NMOSFET-based temperature sensor operating between 14K and 481K, IEEE Electron Device Letters, 45 (2024) 11.

[9] L. Di Benedetto, N. Rinaldi, G.D. Licciardo, R. Liguori, A. Rubino, A. May, and M. Rommel, Performance and Understanding of 4H-SiC Electron Devices at Low Temperature Range. 2024 IEEE International Semiconductor Conference (2023) 23-28.

[10] Information on https://www.attocube.com.

[11] Information on https://www.lakeshore.com.

[12] X. Chi, K. Tachiki, K. Mikami, M. Kaneko, and T. Kimoto, Different temperature dependence of mobility in n-and p-channel 4H-SiC MOSFETs. Japanese Journal of Applied Physics, 62 (2023), 110906.

[13] R. M. Fox, and R.C. JAEGER, MOSFET behavior and circuit considerations for analog applications at 77 K. IEEE Transactions on electron Devices, 34 (1987) 1, 114-123.